Chapter 2

Theory of P–N Junction Diode

CHAPTER HIGHLIGHTS

- *Introduction*
- *Biasing of p-n Junction Diode*
- *V-I Characteristics of p-n Junction Diode*
- *Breakdown in PN Junction Diodes*
- *PN Junction Capacitances*
- *The Potential Variation within a Graded Semiconductor*
- *Effect of Temperature on PN Junction*
- *Application of PN Diode*
- *Zener Diode*
- *Varactor Diode*
- *Tunnel Diode*
- *Schottky Diode*
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Introduction

In a piece of semiconductor material, if donor impurities are introduced into one side and acceptors into the other side of a single crystal of semiconductor, a P–N junction is formed. The plane dividing into the two halves or zones is called P–N junction shown in below figure.

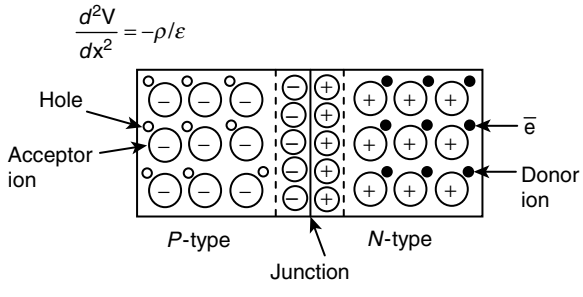
The donor ion is represented by a plus sign because, after this impurity atom 'donates' an electron, it becomes a positive ion. The acceptor ion is indicated by a minus sign because, after this atom 'accepts' an electron, it becomes a negative ion.

The *N*-type material has high concentration of free electrons, whereas *P*-type material has high concentration of holes. At the junction, the free electrons to diffuse over to the *p*-side and holes to the *n*-side, this process is called diffusion.

The general shape of the charge density depends upon how the diode is doped. The region of the junction is depleted of immobile charges, and it is called the depletion region, the space-charge region, or the transition region.

The space-charge density (ρ) is zero at the junction. It is positive to the right (*n*-side) and negative to the left (*p*-side) of the junction.

The field intensity curve is proportional to the integral of the charge density curve. This is known as Poisson's equation.



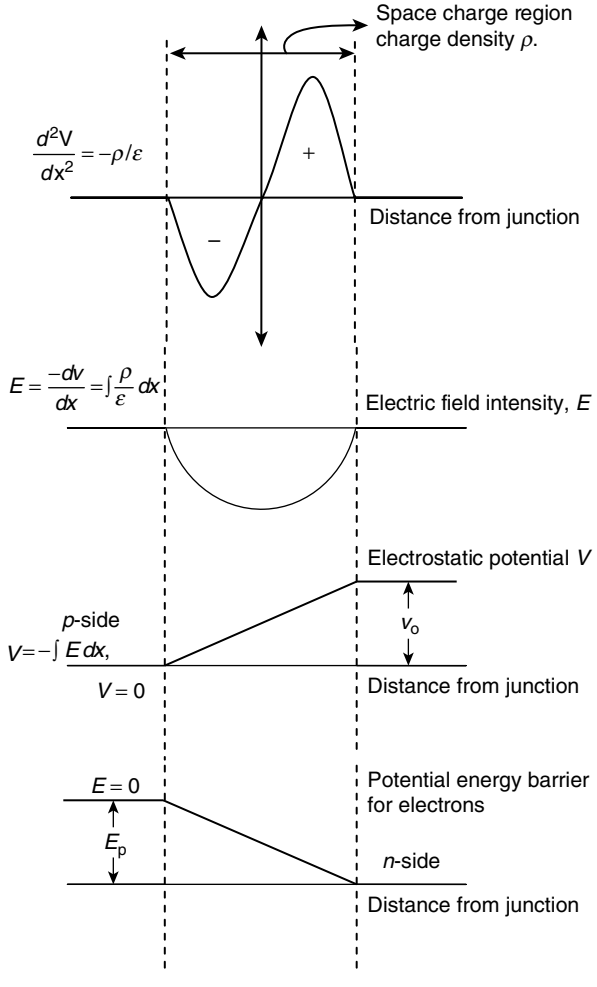


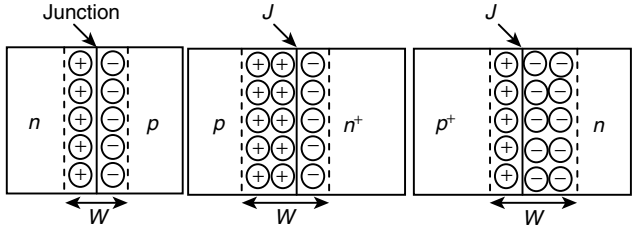
Figure 1 A schematic diagram of a P–N junction including the charge density, electric field intensity, and potential energy barriers at the junction

The barrier potential of P–N junction mainly depends on the following factors:

1. The type of semiconductor used
2. The concentration of impurity
3. The temperature

Effect of Doping on Depletion Region

The width of the depletion region depends on the amount of doping on *n*-side and *p*-side.



(i) Both sides equally doped (*p-n* diode) ($W_n = W_p$)

(ii) n^+p diode ($W_n << W_p$) $W \approx W_P$

(iii) p^+n diode ($W_n >> W_p$) $W \approx W_n$

($W = W_n + W_P$)

The depletion region penetrates more into the lightly doped side.

The relation between the impurity concentration and depletion width is

$$W_p . N_A = W_n . N_D$$

Biasing of P–N Junction Diode

Applying external dc Voltage to any electronic device is called biasing.

Forward Biasing of P–N Junction Diode

When the P–N junction is forward biased as long as the applied voltage is less than the barrier potential, there cannot be any conduction.

When the applied voltage becomes more than the barrier potential, the negative terminal of the battery repels electrons and positive terminal repels holes. Thus, the applied voltage overcomes the barrier potential and hence reduces the width of depletion region.

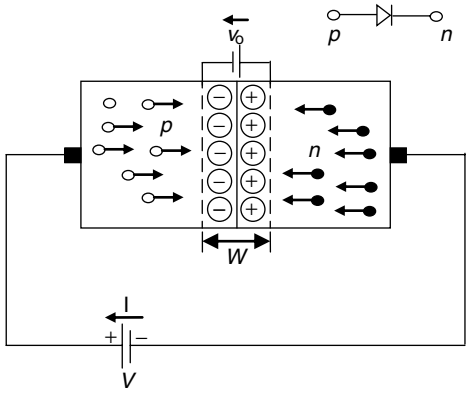


Figure 2 P–N junction under forward bias

Reverse Biasing

If *p*-side of a P–N junction is connected to the negative terminal, and the *n*-side is connected to the positive terminal of a battery, since the holes in the *p*-region are attracted towards the negative terminal, and the electrons in the *n*-region are attracted towards the positive terminal. There can be no diffusion of charge carriers through the junction, and hence, there is no conduction.

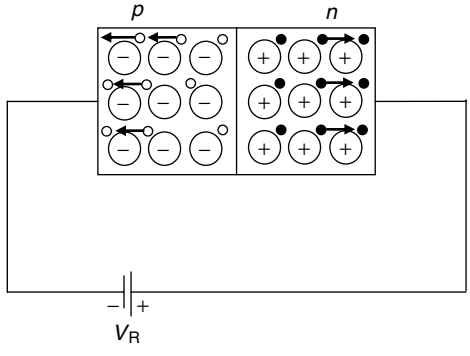


Figure 3 P–N junction under reverse bias

The applied reverse bias voltage established an electric field in the same direction as the field due to the barrier potential with the result the width of the depletion region increases, and the junction offers high resistance.

A small reverse current of the order of μA or nA flows through the reverse-biased P–N junction. This is due to the applied voltage acts as forward bias for the minority charge carriers. This current gets stabilized to a steady magnitude and is quite independent of the bias voltage and this is also called as reverse saturate current (I_s or I_o).

The reverse saturation current is temperature-dependent, and it is almost doubles for every 10°C rise of temperature.

$$\therefore I_{o2} = I_{o1} . 2^{(T_2 - T_1)/10} \text{ Amps}$$

Electrons forming covalent bonds of the semiconductor atoms in the *P*- and *N*-type regions may absorbs sufficient energy form heat and light to cause breaking of some covalent bonds. Hence, $\bar{e}$ -hole pairs are continually produced in the both regions. Under the reverse bias condition, the thermally generated electrons in the *N*-region attracts towards the '+ve' terminal and holes towards '-ve' terminal of the battery. The magnitude of reverse saturation current mainly depends upon junction temperature because the major source of minority carriers is thermally broken covalent bonds.

Energy Band Structure of an Open-Circuited P–N Junction

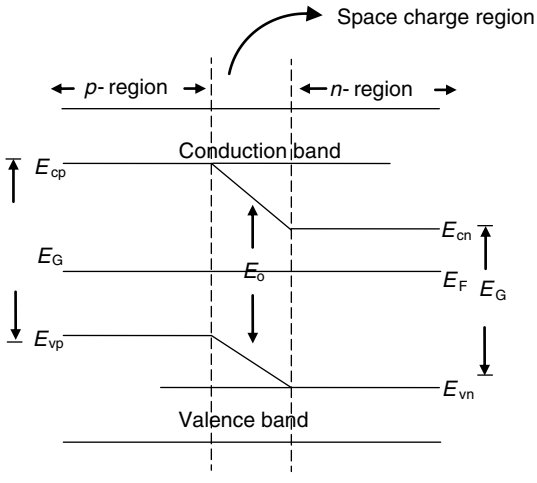


Figure 4 Energy band structure

The energy band structure of a P–N junction is shown above figure, where the fermi level E_F is closer to the conduction band E_{cn}. In *N*-type material, and it is closer to the valence band E_{vp} in the *P*-type material.

The total shift in the energy level E_o is given by

$$E_o = E_{cp} - E_{cn} = E_{vp} - E_{vn}.$$

This energy E_o(in eV) is potential energy of the electrons at the P–N junction, and it is equal to qv_o (in *V*).

Where $V_o \rightarrow$ contact potential (in volts)

(or)

Contact difference of potential

(or)

The barrier potential

Contact Potential V_o

$$\text{Energy band gap } E_G = KT\ln \frac{N_c.N_v}{n_i^2} \text{ eV}$$

$$E_o = KT \ln\left[\frac{N_A N_D}{n_i^2}\right]\text{eV}$$

We know $E_o = q\,V_o$

$$\therefore \text{ Contact potential } V_o = \frac{KT}{q}.ln\left[\frac{N_A.N_D}{n_i^2}\right] \text{volts}$$

$$\boxed{\therefore V_o = V_T.ln\left[\frac{N_A N_D}{n_i^2}\right]\text{v}}$$

The alternative expression for E_o is as follows: $n_n = N_D$ $n_n.p_n = n_i^2$ For *N*-type materials

$$p_n = \frac{ni^2}{N_D}$$

and $n_p.p_p = n_i^2$ at $p_p = N_A$ for *p*-type

$$\therefore\ n_p = \frac{n_i^2}{N_A}$$

$$\therefore E_o = KT \ln\left[\frac{P_{Po}}{p_{no}}\right] = KT \ln\left[\frac{n_{no}}{n_{po}}\right]$$

Diode Current Equation

$$\boxed{\therefore I = I_0\left[e^{V_d/\eta V_T} - 1\right] \text{ Amp}}$$

Where v = external voltage applied to the diode, η = constant, 1 for Ge and 2 for si

$$V_T = \frac{KT}{q} = \frac{T}{11{,}600}V$$

$I_o \Rightarrow$ reverse saturation current. It is represented by $I_o = \text{A.q}$

$$\left[\frac{D_P}{L_P.N_D} + \frac{D_n}{L_n.N_A}\right] n_i^2$$

NOTE

When the diode is reverse biased, its current equation may be obtained by reverse the sign of the applied voltage v, (−ive). Then, the diode current with reverse bias is $I = I_o$ $\left[e^{-Vd/\eta V_T} - 1\right]$ Amp.

Solved Examples

Example 1

A silicon diode has a forward current of 750 mA and a reverse saturation current of 50 nA at room temperature. Then, the applied forward bias voltage is

(A) 0.75 V. (B) 0.86 V.
(C) 0.36 V. (D) 0.97 V.

Solution

We know $I = I_o\left[e^{V_d/\eta V_T} - 1\right]$.

From the given data

$$I = 750 \text{ mA}$$

$$I_o = 50 \times 10^{-9} \text{ A}$$

$$V_T = 0.026 \text{ V}$$

$$15 \times 10^6 = [e^{\text{Vd}/2 \times 0.026} - 1]$$

$$(19.23)v_d = \ln [15 \times 10^6]$$

$$V_d = 0.86 \text{ volts}$$

V–I Characteristics of P–N Junction Diode

Forward-Biased P–N Junction

As the applied voltage is increased beyond cut in voltage, the junction readily conducts, and the forward current. It rapidly rises with further increase in v_f. These are shown in the below figure.

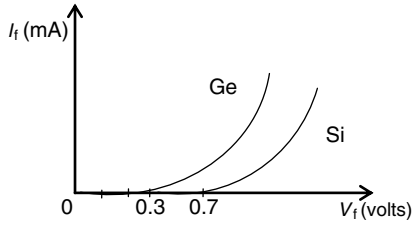


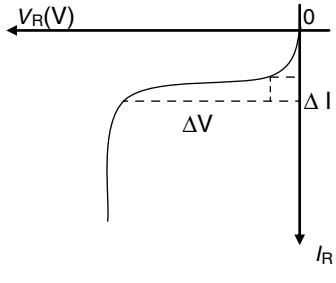
Figure 5 V–I characteristics of P–N diode

Forward resistance of the junction diode is

$$R_f = \frac{\Delta V_f}{\Delta I_f}\Omega \Rightarrow R_f \Rightarrow \text{is small}$$

Reverse-Biased P–N Junction

When P–N junction is reverse biased, the depletion region widens, and as a result, the junction offers very high resistance.



Breakdown in P–N Junction Diodes

The junction breakdown is due to the following two factors. They are as follows:

(i) Zener effect.
(ii) Avalanche effect.

Avalanche Effect

As the reverse voltage increases, the minority charge carriers acquires more kinetic energy, so its drift velocity increases.

They acquire sufficient energy, from the applied potential to produce new carriers by removing valance electrons from their bonds.

These new carriers will in turn collide with other atoms and will increase the number of electrons and holes available for conduction. Thus, charge carriers increase at a very rapid, and at breakdown voltage, the minority carrier current rises rapidly, causing the breakdown of the junction. This phenomenon is formed as avalanche effect.

It is a positive temperature coefficient.

Zener Effect

Practical diodes are heavily doped, the depletion layer is very thin, and hence, the potential gradient is quite high. Increase in reverse bias increases the potential gradient, even if the initially available carriers do not acquire sufficient energy to disrupt bonds, it is possible to initiate breakdown by a direct rupture of the bonds because of the existence of strong electric field. This phenomenon is known as Zener effect.

The Zener effect is in diodes with breakdown voltages below about 6 V, and the operating voltages in avalanche breakdown are from several volts to several 100 volts with power rates up to 50 W.

$$(V_A > 6\text{ V})$$

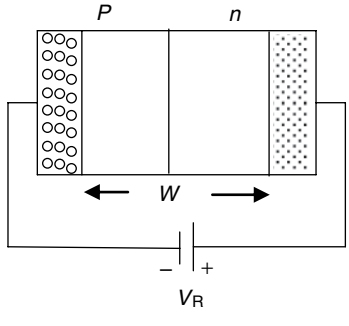
It has a negative temperature coefficient.

P–N Junction Capacitances

In a P–N junction, there is a depletion region in between *P*-type and *N*-type semiconductor, the depletion region is totally devoid of charge carriers, and hence, it acts as a dielectric in between two oppositely charged surfaces. A practical junction diode possesses two types of capacitances:

Transition or Space Charge or Depletion Capacitance (CT)

Under reverse-biased condition, the majority carriers move away from the junction, thereby uncovering more immobile charges. Hence, the width of the space charge layer at the junction increases with reverse voltage.



$$\Rightarrow C_T = \frac{\in A}{W}$$

Where $A \rightarrow$ surface area of the junction
$W \rightarrow$ width of the depletion layer

$$W = \sqrt{\frac{2\varepsilon_s}{q}\left[\frac{1}{N_A} + \frac{1}{N_D}\right]V_j}$$

Diffusion Capacitance (C_D)

When a P–N junction is forward biased, the capacitance of the junction is much larger than its transition capacitance.

Diffusion capacitance may be defined as the rate of change of charge with voltage.

$$C_D = \frac{dQ}{dV}$$

$$i = \frac{dq}{dt} \Rightarrow dQ = \tau.dI$$

$$C_D = \tau.\frac{dI}{dv}$$

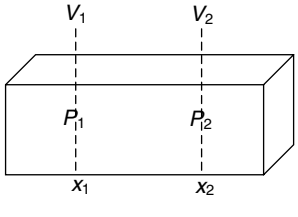
We know $I_D \simeq I_o \cdot e^{\left(\frac{Vd}{\eta V_T}\right)}$

$$\frac{dI}{dV} = \frac{I}{\eta V_T} = g$$

$$\therefore C_D = \frac{\tau I}{\eta V_T} \text{ or } C_D = \tau g$$

Where $g = 1/r = \dfrac{I_f}{\eta V_T}$

The Potential Variation Within a Graded Semiconductor

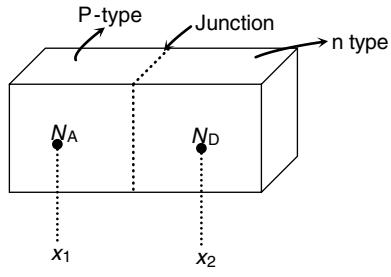


A graded semiconductor is one whose doping is non-uniform. Assume the specimen is open circuited, so the total current must be zero. At $x = x_1$, the hole concentration is P_1 and at $x = x_2$, the hole concentration is P_2. There exists an electric field which opposes the movement of holes. The electric potential is given by

$$V_{21} = V_2 - V_1 = V_T \ln \frac{P_1}{P_2}$$

$$P_1 = P_2 e^{V_{21}/V_T}$$

An Open-Circuited Step-Graded Junction



Assume a P–N junction, where the *P*-type is doped with a constant concentration N_A and the *N*-type is doped with constant concentration N_D. The contact difference potential V_o is given by

$$V_o = V_{21} = V_T \ln\left(\frac{P_{po}}{P_{no}}\right)$$

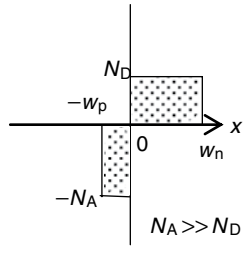
$$V_o = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right) V$$

Step-graded Junction

Consider a junction in which there is an abrupt change from acceptor ions on one side to donor ions on the other side. A step-graded junction is also formed between emitter and base of an integrated transition.

$$W_P.N_A = W_n.N_D$$

$$W \alpha V_j^{1/2}$$



Linearly Graded Junction

A second form of junction is obtained by drawing a single crystal from a melt of Ge whose type is changed during process by adding first *P*-type and *N*-type impurities. A linearly graded junction is also formed between the collector and base of an integrated transistor. For such a junction, the charge density varies gradually. However, ***W*** varies as $V_j^{1/3}$.

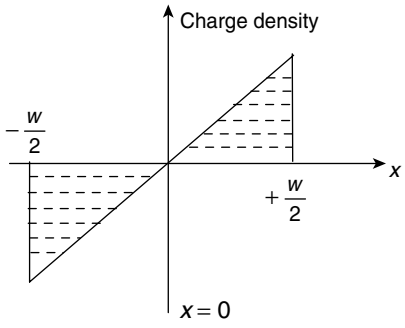


Figure 6 The charge density variation vs. distance at a linearly graded P–N junction

Effect of Temperature on P–N Junction

The rise in temperature increases the generation of electron – hole pairs in semiconductors and increases their conductivity. That is, current through the P–N junction diode increases with temperature.

$$I = I_o \left(e^{V_d/\eta V_T} - 1\right)$$

The reverse saturation current I_o of diode approximately doubles for every 10°c rise in temperature.

$$\therefore I_{o2} = I_{o1}\left(2^{(T_2 - T_1)/10}\right)$$

Hence, if the temperature is increased at fixed voltage, the current I increases. To bring the current I to its original value (i.e., constant), the voltage V is to be reduced.

$$\Rightarrow \frac{dv}{dT} \approx -2.3\,\text{mV/°c}$$

A Ge diode can be used up to a maximum of 75° C and a Si diode to maximum of 175°C.

Example 2

A Ge diode has a saturation current of 8 μA at room temperature. Then, the reverse saturation current at T = 400°k is

(A) 7.5 mA. (B) 8.42 mA.
(C) 8.192 mA. (D) 9.34 mA.

Solution

We know $I_{02} = I_{01}.\, 2^{(T_2 - T_1)/10}$

Given $I_{01} = 8\ \mu A$

$T_1 = 300°k$

$T_2 = 400°k$

then $I_{02} = 8 \times 10^{-6} \times 2^{100/10} = 8.192\ \text{mA}$

NOTE

The gold dopant, sometimes called a life time killer, it increases the recombination rate and removes the stored minority carries.

Application of P–N Diode

1. Rectifiers in DC power supplies.
2. Switching circuits.
3. Clamping and clipping circuits, used as wave shaping circuits used in computers, radar, radio and TV receivers.
4. Demodulation circuits.

The same P–N junction with different doping levels finds special applications as follows.

1. Zener diodes in voltage regulators.
2. Varactor diodes in tuning sections of radio and TV Receivers.
3. detectors (APD, PIN photo diode)
4. LED and LCD's in digital displays.
5. LASER diodes in optical communication.

Tunnel diodes used as a relaxation oscillators at microwave frequencies.

Zener Diode

When the reverse voltage reaches breakdown voltage in normal P–N diodes, the current through the junction and the power dissipation at the junction will be high such an operation is destructive and the diode gets damaged.

As diodes can be designed with adequate power dissipation capabilities to operate in the breakdown region, one such diode is known as zener diode. It is a heavily doped than the ordinary diode.

In forward bias, the operation of zener diode is the same as normal P–N diode.

While under reverse biased condition, breakdown of the junction occurs, it depends on the concentration of doping. If the diode is heavily doped, depletion layer will be very thin and breakdown occurs at lower reverse voltage and further breakdown voltage is sharp.

The sharp increasing current under breakdown conditions are due to the following mechanisms.

1. Zener breakdown
2. Avalanche breakdown

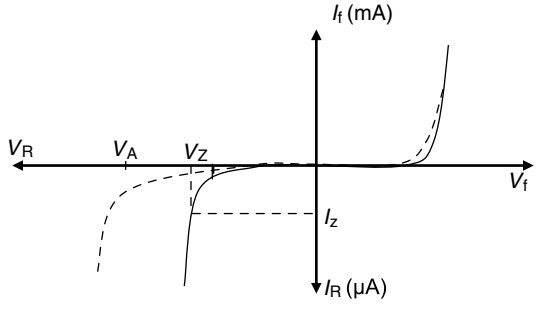
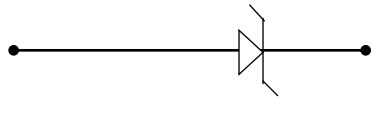


Figure 7 The *V–I* characteristics of an avalanche, or Zener diode

Symbol



Example 3

Consider an asymmetrical Si junction, with $N_A = 10^{19}$ cm^{-3} and $N_D = 10^{17}$ cm^{-3}. If the cross-sectional area of the junction is 10μm^2, determine its transition capacities with no applied bias. ($n_i = 1.45 \times 10^{10}$).

Solution

$$C_T = \frac{'\varepsilon' A}{W}$$

$$W = \sqrt{\frac{2\varepsilon_s}{q}\left[\frac{1}{N_A}+\frac{1}{N_D}\right].V_j}$$

$$v_j = V_o = V_T \ln\left[\frac{N_A.N_D}{n_i^2}\right] \text{ V}$$

$$V_j = 0.94 \text{ volts},.\ \varepsilon_s = 11.9\ \varepsilon_0^{si}$$

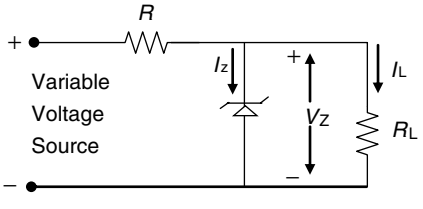
$$W = \sqrt{\frac{2\times11.9\times8.85\times10^{-12}}{1.6\times10^{-19}}\times\left[\frac{1}{10^{19}}+\frac{1}{10^{17}}\right].(0.94)\times10^{-6}}$$

$$W = 11.17\ \mu\text{m}$$

$$C_T = \frac{11.9\times8.85\times10^{-12}\times10\times10^{-12}}{11.17\times10^{-6}}$$

$$= 9.428 \times 10^{-17}\ \text{F}.$$

Zener Diode as a Voltage Regulator



A zener diode, under reverse bias breakdown condition, can be used to regulate the voltage across the load irrespective of the supply voltage or load current. The voltage across the zener diode remains constant even if current through it changes by large extent.

Zener breakdown occurs and current I_Z flows through it. A current I_L flows into the load R_L.

$$V_Z = I_L.R_L$$

$$V_Z = V_L$$

The current through R is, $I = I_Z + I_L$.

If the supply voltage now increases, more current is drawn from the supply. Since the zener diode is operating in the breakdown region, its current I_Z increases and I_L remains same (V_z = constant)

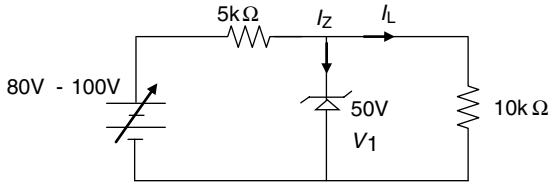
If P_Z denote the power rating of the zener diode.

$$\boldsymbol{P_Z = V_Z.I_{Z(max)}}, \text{ watts}$$

If the load resistance decreases, more current flows into the load; if the load resistance increases, the load current decreases. That is, the load is parallel to the zener diode operations with a constant breakdown voltage.

Example 4

For the circuit shown in figure, find the maximum and minimum values of zener diode current.



Solution

From the given data

$$V_Z = 50\ \text{V}, = V_L$$

$$\therefore I_L = \frac{50}{10}\text{mA} = 5\text{mA}$$

$$\text{If } V_{in} = 80\ \text{V}$$

$$I = \frac{80-50}{5}\text{mA} = 6\ \text{mA}$$

$$I = I_Z + I_L$$

$$\therefore I_{Z(min)} = I - I_L = (6-5)\text{mA} = 1\ \text{mA}$$

$$V_{in} = 100\ \text{V}.$$

$$I_{max} = \frac{100-50}{5}\text{mA} = 10\ \text{mA}$$

$$I_{max} = I_{Zmax} + I_L$$

$$I_{Z(max)} = (10-5)\text{mA} = 5\ \text{mA}$$

$\therefore$ The range of zener current is varies from 1 mA to 5 mA.

Example 5

Zener diode is _____ device.

(A) A non-linear (B) a Linear

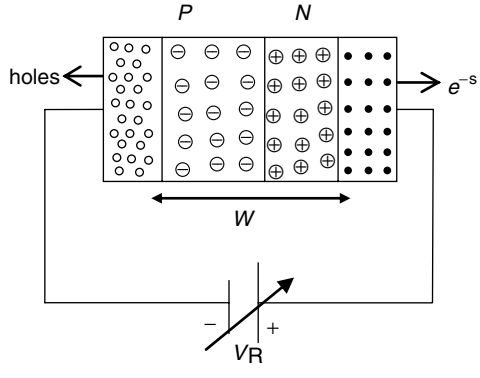
(C) an amplifier (D) None of the above

Solution: (A)

Varactor Diode

The varactor diode also called as a varicap or tunning or voltage variable capacitor diode, it is a lightly doped diode.

The diode is reverse-biased, a depletion region is formed, shown in below figure.



If the reverse bias voltage varies, the width of the depletion region also varies.

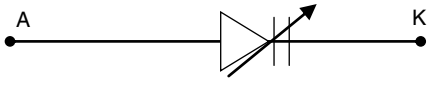
If V_R increases, the width of the depletion layer 'W' becomes wider.

$$V_R \propto W.$$

This depletion region is devoid of majority carriers and acts like an insulator preventing conduction between the N and P region of the diode, which separates the two plates of a capacitor.

$$C_T = \frac{\varepsilon A}{W} \text{ F}$$

The capacitance is inversely proportional to the distance between the plates (C_T a $1/W$)



Circuit symbol of varactor diode

Applications

1. Varactor diodes are used in FM radio and TV Receivers AFC circuits.
2. Self-adjusting bridge circuits and adjustable band pass filters.
3. Tuning circuits of LC resonant circuits in μw frequency multipliers and in very low noise μw parametric amplifiers.

Tunnel Diode

The tunnel or Esaki diode is a thin-junction diode which exhibits negative resistance under forward bias.

An ordinary P–N junction diode has an impurities concentration of $1:10^8$ atoms. In this, the amount of doping is 1 in 10^3 atoms.

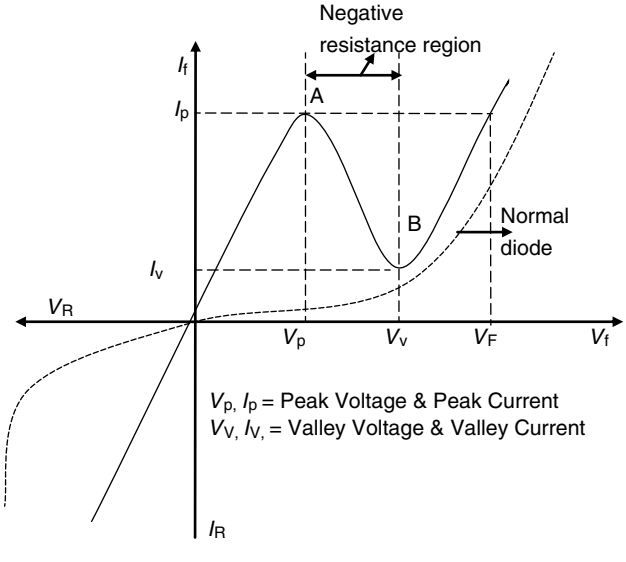


Figure 8 *V–I* characteristics of tunnel diode

Operation: When the semiconductor is very highly doped, the fermi level goes above the conduction band for *N*-type and below valance band for *P*-type material. These are called degenerate materials.

Under Forward Bias

Step 1: At zero bias there is no current flow.

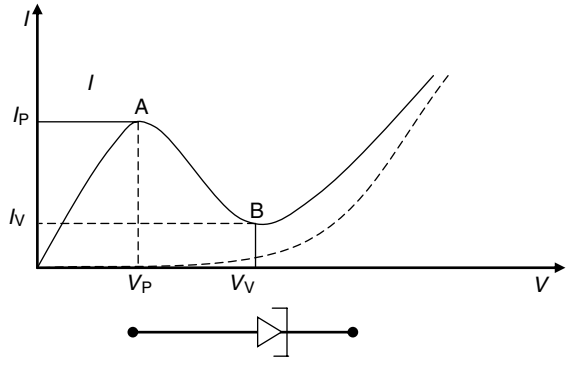
Step 2: A small forward bias is applied. The potential barrier is still very high with no noticeable injection and forward current through the junction. However, electrons in the conduction band of the *N*-region will tunnel to the empty states of the valance band in *P*-region. This will create forward bias tunnel current.

Step 3: With a large voltage, the energy of the majority of e in the *N*-region is equal to the empty states (holes) in the valance band of *P*-region. This will produce maximum tunnelling current.

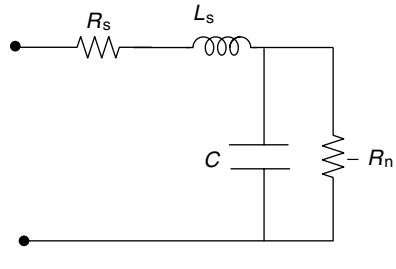
Step 4: As the forward bias continuous to increase, the number of e's in the *n*-side that are directly opposite to the empty states in the valance band (In terms of their energy) decrease. That is, decrease in the tunnelling current will start.

Step 5: As more forward voltage is applied, the tunnelling current drops to zero. However, the regular diode forward current due to electron – hole injection increases due to lower potential barrier.

Step 6: With further voltage increase, the tunnel diode *V–I*. characteristics is similar to that of a normal P–N diode.



(a) Symbol



(b) Tunnel diode circuit.

Applications

1. High-speed switch
2. High-frequency oscillator
3. The most commonly available tunnel diodes are made from Ge or GaAs.

NOTE

It is the difficult to have a high ratio of peak to valley current $\frac{I_p}{I_v}$ with Si.

Example 6

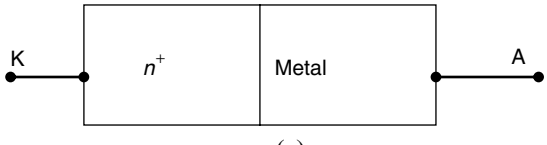
The reverse bias breakdown of high speed Si transistors is due to

(A) avalanche breakdown mechanism at both the junctions.
(B) zener breakdown mechanism at base-collector junction.
(C) zener breakdown mechanism at base-emitter junction.
(D) All the above

Solution: (C)

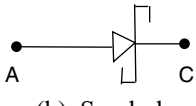
Schottky Diode

1. Schottky diodes are high current diodes used in high frequency and fast switches applications.
2. A Schottky diode is formed by joining a doped *N*-type with a metal such as gold silver or platinum.
3. It means that it has a metal-to-semiconductor junction rather than P–N junction.



(a)

Figure 9 Schottky diode structure

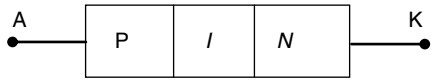


(b) Symbol

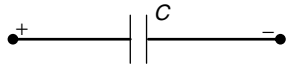
4. The forward voltage drop is 0.3 V.
5. There are only majority carriers with no reverse leakage current.
6. The metal conductor has many conduction band electrons and *N*-type is also heavily doped.
7. When forward bias applied, the *N*-type electrons move across to the metal region and rapidly loss energy. The process is very fast which makes Schottky diodes ideal for fast switches applications.
8. It is also called hot carrier diode.

Pin Diode

1. The PIN diode consists of heavily doped *P* and *N* regions, with are separated by intrinsic material.
2. In reverse bias, the PIN diode acts like a capacitance.
3. When forward bias applied, it acts like a current controlled variable resistance.



(a) PIN diode



(b) reverse biased

(c) forward biased

Example 7

Find the correct match between List-I and List-II.

List-I (Diode)	List-II (Application)
P. Varactor diode	1. Voltage reference
Q. PIN diode	2. High-frequency switch
R. Zener diode	3. Tuning circuits
S. Schottky diode	4.Current controlled attenuator

(A) P-4, Q-2, R-1, S-3
(B) P-2, Q-4, R-1, S-3
(C) P-3, Q-4, R-1, S-2
(D) P-1, Q-3, R-2, S-4

Solution

P-3, Q-4, R-1, S-2

Example 8

Match List-I with List-II.

List-I	List-II
P. Zener diode	1. High-speed switch
Q. Tunnel diode	2. Voltage stabilizer
R. PIN diode	3. Negative resistance
S. Si diode	4. Very low reverse saturation current.

Solution

P-2, Q-3, R-1, S-4

Example 9

The values of voltage (V_D) across a tunnel diode corresponding to peak and valley currents are V_P and V_V, respectively. The range of tunnel diode voltage V_D for which the slope of its and I–V_D characteristics is negative would be.

(A) $V_D < 0$ (B) $0 \le V_D < V_P$
(C) $V_P \le V_D < V_V$ (D) $V_D \ge V_V$

Solution: (C)

Example 10

A p^+n junction has a built-in potential of 0.8 V. The depletion layer width at a reverse bias of 1.2 V is 2 μm, for a reverse bias of 7.2 V, the depletion layer width will be.

(A) 4 μm. (B) 4.9 μm.
(C) 8 μm. (D) 12 μm.

Solution

We know

$$W \propto \sqrt{V_j}$$

V_j = junction potential = Built in potential + V_R

$$V_j = V_o + V_R$$

$$\frac{W_1}{W_2} = \sqrt{\frac{V_o + V_{R1}}{V_o + V_{R2}}}$$

$$\frac{2\mu m}{W_2} = \sqrt{\frac{0.8+1.2}{0.8+7.2}}$$

$$W_2 = 2\times10^{-6}\times 2 = 4\ \mu m$$

NOTES

Diodes and its normal operating region

1. P–N diode → Forward bias
2. Zener diode → Reverse bias
3. Avalanche diode → Reverse bias
4. Tunnel diode → Forward bias
5. PIN diode → Forward bias
6. Varactor diode → Reverse bias
7. Schottky diode → Forward bias

Example 11

A silicon diode has reverse saturation current of 2.5 μA at 300 K. Find forward voltage for a forward current of 10 mA.

Solution

$$I = I_0\left(e^{V/\eta V_T} - 1\right)$$

$$0.01 = 2.5\times10^{-6}\left(e^{V/2x\,0.026} - 1\right)$$

$$V = 0.43 \text{ volts.}$$

Example 12

Find the dynamic resistance of a P–N junction Ge diode at a forward current of 2 mA.

$$\text{Assume } \frac{KT}{q} = 25\,\text{mV}$$

Solution

$$r_d = \frac{\eta V_T}{I}$$

Let $\eta = 1$ $V_T = 25$ mV

$$r_d = \frac{0.025}{0.002} = 12.5\,\Omega$$

Example 13

Determine ac resistance for a germanium semiconductor diode having a forward bias of 200 mV and reverse. Saturation current of 1 μA at room temperature.

Solution

$$r_d = \frac{\eta V_T}{I_0\left(e^{V/\eta V_T}\right)} = \frac{0.026}{1\ x\ 10^{-6}\left(e^{0.20/.026}-1\right)} = 11.86\ \Omega$$

Example 14

Find the value of contact potential of an abrupt P–N junction at room temperature of intrinsic concentration $n_i = 1.5 \times 10^{16}/m^3$ with doping level of $N_D = N_A = 10^{21}/m^3$.

Solution

$$V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right) = \frac{T}{11,600}\ln\frac{\left(10^{21}\right)^2}{\left(1.5\times10^{16}\right)^2}$$

$$= \frac{300}{11,600}\ln\frac{\left(10^{21}\right)^2}{\left(1.5\times10^{16}\right)^2} = 0.5745\ \text{V}$$

Example 15

A germanium diode carries a current of 1 mA at room temperature when a forward bias of 0.15 V is applied. Estimate the reverse saturation current at room temperature.

Solution

The diode current, $I = I_0\left(e^{V/\eta V_T} - 1\right)$

$$I_0 = \frac{I}{\left(e^{V/\eta V_T} - 1\right)} = \frac{1\ x\ 10^{-3}}{\left(e^{0.15/0.026} - 1\right)} = 3.12\ \mu A$$

Example 16

Calculate the wavelength λ of an electron with kinetic energy of 300 eV. Mass of an electron = 9.108×10^{-31} kg, charge = 1.602×10^{-19} c. Plank's constant, $h = 6.626 \times 10^{-34}$ J-S

Solution

Energy associated with electron

$$= 300\ \text{eV} = 300 \times 1.602 \times 10^{-19}\ \text{J}$$

Velocity of electron $V = \sqrt{\frac{2E}{m}}$

$$= 10.273 \times 10^6\ \text{m/s}$$

$$\lambda = \frac{hv}{E} = 1.416 \times 10^{-10}\ m = 1.416\ A^0$$

Example 17

An *N*-type germanium crystal has a current density of 100 A/m^2. The crystal has a resistively of 0.5 Ω-m and electron mobility of 0.4m^2|vs. Calculate the drift velocity and the time taken by the electron to travel 10 μm in the crystal.

Solution

Electron drift velocity, $v = \mu \times E$

$$= \mu \times \frac{J}{\sigma} = \mu \times J \times \rho = 0.4 \times 100 \times 0.5 = 20 \text{ m/s}$$

Time taken by the electron to travel 10×10^{-6} m is crystal

$$= \frac{10 \times 10^{-6}}{20}$$

$$= 0.5 \times 10^{-6} \text{ second}$$

Example 18

A specimen of germanium at 300 K for which the density of carriers is 2.5×10^{13} cm^{-3}, is doped with impurity atom for 10^6 germanium atoms. All the impurity atoms may be assumed ionized. The resistivity of doped material is 0.039Ω cm. Carrier mobility for germanium at 300 K is 3,600 cm^2/V-S. For the doped material, find the electron and hole densities $q = 1.602 \times 10^{-19}$ C

Solution

Conductivity of doped material,

$$\sigma_n = \frac{1}{\rho} = \frac{1}{0.039} = 25.64 \ \Omega\text{–cm}$$

$$\sigma_n = nq\mu_n = N_D q \mu_n$$

$$N_D = \frac{\sigma_n}{q\mu_n} = \frac{25.64}{1.602 \times 10^{-19} \times 3600}$$

$$n_n = N_D = 4.45 \times 10^{16}/\text{cm}^3$$

$$P_n = \frac{n_i^2}{N_D} = \frac{\left(2.5 \times 10^{13}\right)^2}{4.45 \times 10^{16}} = 1.4 \times 10^{10}/\text{cm}^3$$

Example 19

In a *P*-type semiconductor, the Fermi level is 0.27 eV above the valence band at a room temperature of 300 K. Find the new position of the Fermi level at a temperature of 400 K.

Solution

$$E_F = E_v + KT \ln \frac{N_v}{N_A}$$

$$E_F - E_v = KT \ln \frac{N_v}{N_A}$$

At $T = 300$ K,

$$0.27 = k \times 300 \times \ln \frac{N_v}{N_A} \qquad \rightarrow (1)$$

at $T = 400$ K

$$E_{F1} - E_v = k \times 400 \times \ln \frac{N_v}{N_A} \qquad \rightarrow (2)$$

(2) ÷ (1) gives

$$E_{F1} - E_v = \frac{400}{300} \times 0.27 = 0.36 \text{ eV}$$

The new position of the Fermi level lies 0.36 eV above the valence band.

Example 20

Find the diffusion constant of holes and electrons for germanium at 300 K. The carrier mobilities in cm^2/v-s at 300 K for electrons and holes are 3,600 and 1,700, respectively. Density of carrier is 2.5×10^{13}/cm^3. Boltzmann constant $k = 1.38 \times 10^{-23}$ J/K, $q = 1.602 \times 10^{-19}$ C.

Solution

Diffusion constant for electrons

$$D_n = \mu_n \frac{KT}{q} = \frac{3600 \times 1.38 \times 10^{-23} \times 300}{1.602 \times 10^{-19}} = 93 \text{ cm}^2/\text{s}$$

Diffusion constant for holes $= \mu_p \frac{KT}{q}$

$$= \frac{1700 \times 1.38 \times 10^{-23} \times 300}{1.602 \times 10^{-19}} = 43.93 \text{ cm}^2/\text{s}.$$

Example 21

In an *N*-type semiconductor, the Fermi level is 0.24 eV below the conduction band at a room temperature of 300 K. If the temperature is increased to 350 K, determine the new position of the Fermi level

Solution

$$E_F = E_c - KT \ln \frac{N_c}{N_D}$$

$$E_c - E_F = KT \ln \frac{N_c}{N_D}$$

$$0.24 = 300 \times k \times \ln \frac{N_c}{N_D} \qquad \rightarrow (1)$$

At $T = 350$ K

$$E_c - E_F = 350 \times k \times \ln \frac{N_c}{N_D} \qquad \rightarrow (2)$$

(2) ÷ (1) gives

$$\frac{E_c - E_{F1}}{0.24} = \frac{350}{300}$$

$E_c - E_{F1} = \frac{350}{300} \times 0.24 = 0.28$ eV , that is, the new position of the fermi level lies 0.28 eV below the conduction band.

Example 22

Find the conductivity of intrinsic germanium at 300 K. If donor impurity is added to the extent of 1 impurity atom in 10^7 germanium atoms, find the conductivity. Given that n_i at 300 K is 2.5×10^{13} cm^{-3} and μ_n and μ_p in germanium are 3,800 and 1,800 cm^2/v-s, respectively.

Solution

$$\sigma_I = n_i q (\mu_n + \mu_p)$$

$$= 2.5 \times 10^{13} \times 1.6 \times 10^{-19} (3800 + 1800)$$

$$= 0.0224 \text{ (ohm–cm)}^{-1}$$

Concentration of donor atoms

$$= \frac{4.4 \times 10^{22}}{10^7} = 4.4 \times 10^{15}/\text{cm}^3$$

Concentration of electrons

$$n = N_D = 4.4 \times 10^{15}/\text{cm}^3$$

Concentration of holes,

$$p = \frac{n_i^2}{N_D} = 1.42 \times 10^{11} \text{ holes} | \text{cm}^3$$

Conductivity in N-type semiconductor

$$\sigma_n = q\, N_D \mu_n = 2.68 \text{ (ohm – cm)}^{-1}$$

Example 23

A potential difference of 10 V is applied longitudinally to a rectangular specimen of intrinsic germanium of length 25 mm, width 4 mm, and thickness 1.5 mm. Determine at room temperature

(i) electron and hole drift velocities

(ii) the conductivity of intrinsic germanium if intrinsic carrier density is $2.5 \times 10^{10}/\text{ m}^3$ and

(iii) the total current

Given $q = 1.6 \times 10^{-19}$ C,

$\mu_n = 0.38 \text{ m}^2/\text{V–s}$,

$\mu_h = 0.18 \text{ m}^2/\text{V–s}$

Solution

Applied electric field $E = \frac{V}{l} = \frac{10}{0.025}$

(i) electron drift velocity, $V_e = \mu_n \times E$

$= 0.38 \times 400 = 152$ m/s

Hole drift velocity, $V_h = \mu_p \times E$

$= 0.18 \times 400 = 72$ m/s.

(ii) Intrinsic conductivity of G_e

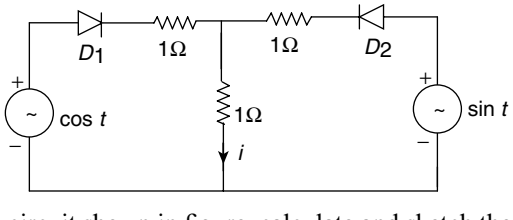
$$\sigma_I = n_i q \left(\mu_n + \mu_p\right) = 2.24 \left(\text{ohm} - \text{cm}\right)^{-1}.$$

(iii) Total current, $I = \sigma_I$ EA

$= 2.24 \times 400 \times 4 \times 10^{-3} \times 1.5 \times 10^{-3}$

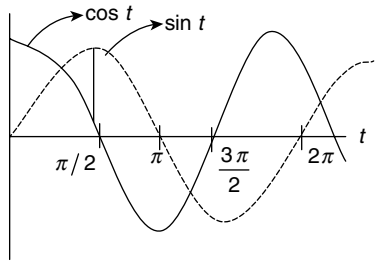
$= 5.376$ mA.

Example 24



In the circuit shown in figure, calculate and sketch the wave form of current i over one period of the input voltages. Assume the diodes to be ideal.

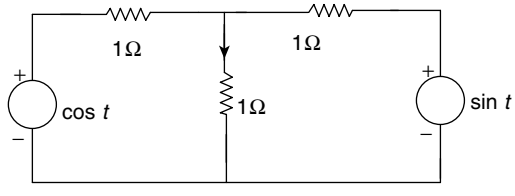
Solution



The two input voltages are shown in figure.

For $0 \le t \le \pi / 2$

Both diodes D_1 and D_2 are forward biased and are, therefore, conducting because both sin$t$ and cos$t$ are positive. The circuit is given in the figure.



By KCL at node A,

$$\frac{V_A - \cos t}{1} + \frac{V_A - \sin t}{1} + \frac{V_A}{1} = 0$$

$$3V_A = \cos t + \sin t \Rightarrow V_A = \frac{\cos t + \sin t}{3}$$

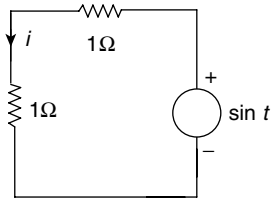
$$I = \frac{\cos t + \sin t}{3} = \frac{V_A}{1}$$

For $\pi / 2 \le t \le \pi$

During this period, only sin$t$ is positive so only diode D_2 is forward biased and conducts. The circuit is given in the figure.

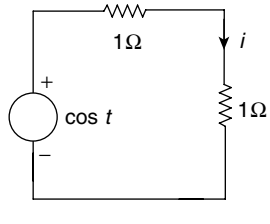
$$i = \frac{\sin t}{2}$$

For $\pi \le t \le \frac{3\pi}{2}$



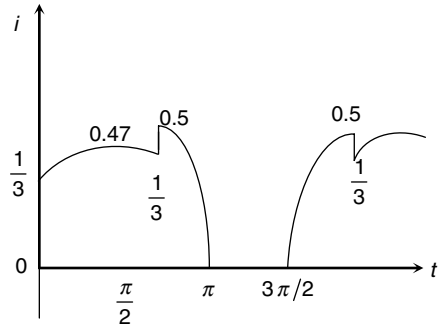
For this period, both cos$t$ and sin$t$ are negative, so both the diodes are reverse biased and do not conduct, so $i = 0$.

For $\frac{3\pi}{2} \le t \le 2\pi$



During this period, only cos*t* is positive, so only diode D_1 is forward biased and conducts. The circuit is shown in figure.

The current $i = \frac{\cos t}{2}$ wave form of the output current I, as calculated above is drawn in the figure.



Example 25

A silicon sample is doped 10^{17} As atoms / cm^3. What is the equilibrium hole concentration P_0 at 300 K? Where is E_F relative to E_i?

Solution

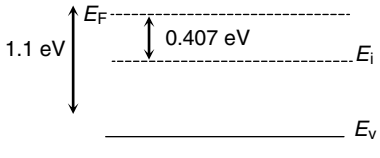
Since $N_D >> n_i$, we can approximate

$$n_0 = N_D \text{ and}$$

$$P_0 = \frac{n_i^2}{n_0} = \frac{2.25 \times 10^{20}}{10^{17}} = 2.25 \times 10^3/\text{cm}^3$$

$$E_F - E_i = KT \ln \frac{n_0}{n_i}$$

$$= 0.025 \ln \frac{10^{17}}{1.5 \times 10^{10}} = 0.407 \text{ eV}.$$



Example 26

A P$^+$n junction has a built in potential of 0.8 V. The depletion layer width at a reverse bias of 1.5 V is 3 μm. For a reverse bias of 7.5 V, the depletion layer width is

Solution

Junction potential = built in potential + reverse bias voltage

$$V_j = V_0 + V_R$$

Now for abrupt P–N junction depletion width

$$W \propto V_j^{1/2}$$

$$W = kV_j^{1/2}$$

$$3 \times 10^{-6} = K(2.3)^{1/2}$$

$$X = K(8.3)^{1/2}$$

$$\frac{3\times10^{-6}}{X} = \left(\frac{2.3}{8.3}\right)^{1/2} \quad \frac{X}{3\times10^{-6}} = \left(\frac{8.3}{2.3}\right)^{1/2}$$

$$X = 5.6 \text{ μm}$$

Example 27

In a sample of GaAs at $T = 150$ K, $n_0 = 6\ p_0$ and $N_a = 0$. The value of n_0 is

Solution

$$KT = 0.0259\left(\frac{150}{300}\right) = 0.01295$$

For GaAs at 300 K

$$N_C = 4.7 \times 10^{17}/\text{cm}^3$$

$$N_V = 7 \times 10^{18}/\text{cm}^3,\ E_g = 1.42 \text{ eV}$$

$$n_i^2 = N_C N_V \left(\frac{150}{300}\right)^3 e^{\frac{-1.42}{0.01295}}$$

$$n_i^2 = 4.7 \times 10^{17} \times 7 \times 10^8 \times \left(\frac{1}{2}\right)^3 e^{-1.42/0.01295}$$

$$= 4.7 \times 10^{17} \times 7 \times 10^8 \times 0.125 \times e^{-1.42/0.01295}$$

$$= 4.7 \times 10^{17} \times 7 \times 10^8 \times 0.125 \times 2.39 \times 10^{-48}$$

$$= 9.828 \times 10^{-13}$$

$$n_i = 9.91 \times 10^{-7}/\text{cm}^3$$

$$n_i^2 = n_0 p_0 = \frac{n_0^2}{6}$$

$$n_0^2 = 6n_i^2 = 5.8968 \times 10^{-12}$$

$$n_0 = 2.42 \times 10^{-6}/\text{cm}^3$$

Example 28

If the current flowing through a P–N junction diode increases 10 times what is the increase in diode voltage? Assume forward-biased Si diode operating at room temperature

Solution

$$I = I_0\left(e^{V_1/\eta V_T} - 1\right)$$

$$I = I_0\left(e^{V_2/\eta V_T} - 1\right)$$

$$10 = e^{V_2 - V_1/2\times26}$$

$$2.302 = \frac{V_2 - V_1}{2\times26}$$

$$V_2 - V_1 = 119.7 \text{ mV}$$

Example 29

An npn transistor under forward active mode of operation is biased at $I_C = 2$ mA and has a total emitter base capacitance of C_k of 20pF and base transit time of t_F of 200 psec. Under this condition, the depletion capacitance of emitter base junction is

Solution

It is the diffusion capacitance
i.e., given

$$C_\mu = 20\text{pF}$$

$$C_\mu = \frac{\tau I_c}{\eta V}, \eta = 1$$

$$C_\mu = \frac{200\times10^{-12}\times2\times10^{-3}}{26\times10^{-3}} = 15\text{pF}$$

Depletion capacitance = 20 – 15 = 5pF

Example 30

For an abrupt P–N junction, the doping concentrations on p side and *n*-side are $10 \times 10^{15}/\text{cm}^3$ and $2 \times 10^{15}/\text{cm}^3$. The P–N junction is reverse-biased and total depletion width is 5 µm. The depletion width on *p*-side is

Solution

$$N_A = 10\times10^{15}/\text{cm}^3$$

$$N_D = 2\times10^{15}/\text{cm}^3$$

$$W_T = 5\ \mu\text{m}$$

$$W_p N_A = w_N N_D \quad W_T = W_P + W_N$$

$$W_P = (W_T - W_P)\frac{N_D}{N_A}$$

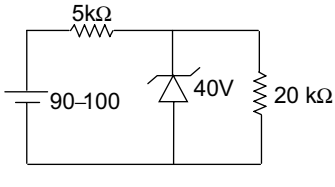
$$W_P\left(1+\frac{N_D}{N_A}\right) = W_T\frac{N_D}{N_A}$$

$$W_P = \frac{W_T N_D}{N_A + N_D}$$

$$= \frac{5\mu\text{m}\times2\times10^{15}}{12\times10^{15}} = 8.3\times10^{-7} = .83\ \mu\text{m}.$$

Example 31

The maximum value of Zener current.



Solution

$$I_R = \frac{100-40}{5\text{k}\Omega} = 12\text{mA}$$

$$I_L = \frac{40}{20\text{k}\Omega} = 2\text{mA}$$

Current through Zener diode = 10 mA.

Example 32

An unregulated supply 50 V varies between 30 V and 50 V and it is desired to use the Zener shunt regulator so that output will be held between 7.4 V and 7.6 V as load changes from 200 mA to 25 mA. The minimum permissible value of series resistance

Solution

$$I_{z\min} = 10\%\text{ of } I_L\max = \frac{10}{100}\times200 = 20\text{mA}$$

$$R_S = \frac{V_{S\min} - V_{R\min}}{I_{Z\min} + I_{L\max}} = \frac{30-7.4}{(20+200)\times10^{-3}}$$

$$= 102.72\Omega.$$

Example 33

A p^+n junction has a built in potential of .8 v. The depletion layer width at a reverse bias of 2.4 v is 3 µm. For a reverse bias of 8 v, the depletion layer width is

Solution

Junction potential = built in potential + reverse bias voltage

$$V_j = V_o + V_R$$

for abrupt junction depletion width $w \propto V_j^{1/2}$

$$w = V_j^{1/2}$$

$$3\ \mu\text{m} = k(.8+2.4)^{1/2}$$

$$\text{Also, } X = k(.8+8)^{1/2}$$

$$\frac{X}{3} = \left(\frac{8.8}{3.2}\right)^{1/2}$$

$$\frac{X}{3} = (2.75)^{1/2}$$

$$X = 4.974\ \mu\text{m}.$$

EXERCISES

Practice Problems I

Direction for questions 1 to 25: Select the correct alternative from the given choices.

1. Calculate built-in potential of a Ge P–N junction if *p*-side is doped with 5×10^{16} acceptors/cm^3 and *n*-side with 5×10^{14} donors/cm^3.

(A) 0.612 volts (B) 0.696 volts
(C) 0.276 volts (D) 0.236 volts

2. The resistivities of the two sides of an abrupt silicon P–N junction are 9.6Ω cm on *p*-side and 100 Ωcm on *n*-side. Find contact potential.

(A) 0.5 volts (B) 0.6 volts
(C) 0.55 volts (D) 0.65 volts

3. What is the ratio of currents for a forward bias of 0.1 volt to the current for the same magnitude of reverse bias of silicon P–N junction?
(A) –6.841 (B) –64.81
(C) +6.841 (D) +64.81

4. What is the change in voltage at 300°K for a 10-fold increase in current for a Si diode operating in the conducting region?
(A) 0.24 volts (B) 0.36 volts
(C) 0.48 volts (D) 0.12 volts

5. For a silicon diode operating under conducting region at room temperature, if the voltage is increased by 0.24 volts, then the current flowing through it increases by _____ number of times.
(A) 10 (B) 20 (C) 50 (D) 100

6. What increase in temperature would result in a reverse saturation current, which is 50 times its value of room temperature?
(A) 40°C (B) 50°C (C) 56°C (D) 46°C

7. A silicon diode operates at a forward voltage of 0.7 volts. Calculate the factor by which the current will be multiplied when the temperature is decreased from 25°C to −55°C.
(A) 0.9 (B) 0.6 (C) 0.3 (D) 0.554

8. An ideal silicon P–N junction has a reverse saturation current of 0.1 μA at a temperature of 125°C. The dynamic resistance for 0.8 volts forward bias at 105°C is _____
(A) 1.2 Ω (B) 12.2 Ω
(C) 24 Ω (D) 1.8 Ω

9. For an alloy Si P–N junction with $N_A << N_D$, calculate depletion layer capacitance (C_T), if the resistivity of P-material is 4Ω-cm, the barrier height, V_o is 0.3 volts, applied reverse voltage is 4 volts and the cross-sectional area is circular of 50 mils in diameter.
(A) 100pF (B) 10pF (C) 1nF (D) 10nF

10. For a Si P^+N junction, $N_D = 10^{15}$ per cm^3 and $V_o = 0.5$ volts. If the applied reverse voltage is 10 volts. Find the value of electric field at the junction.
(A) −5.62 kV/cm (B) −56.81 kV/cm
(C) −5.62 kV/m (D) −56.24 kV/m

11. For a silicon P–N diode, $N_D = 10^{15}$ atoms per $cm^3 << N_A$ and the built-in potential of 0.5 volts. If the applied reverse voltage is 10 volts, find the transition capacitance per square mil.
(A) 0.02 pF/mil^2 (B) 0.2 pF/mil^2
(C) 2.84 nF/mil^2 (D) 2.84 pF/mil^2

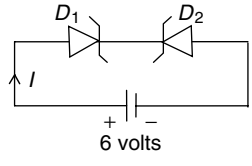
12. Find the magnitude of the electric field at the centre of depletion region of Si P–N junction with $N_A = N_D = 10^{21}$ atoms per m^3 and built-in potential of 0.6 volts.
(A) 94.8 kV/m (B) 94.8 MV/m
(C) 9.48 kV/cm (D) 9.48 MV/m

13. For a silicon P–N junction with $N_A = N_D = 10^{21}$ atoms per m^3 and $n_i = 9.8 \times 10^{15}$ atoms per m^3. Calculate transition capacitance, if the area is 1 mm^2 and the junction is reverse biased with 10 volts.
(A) 10pF (B) 20pF (C) 8pF (D) 12pF

14. The zero barrier height of an alloy Si P–N^+ junction is 0.6 volts, and acceptor concentration is 5×10^{16} atoms per cm^3. If the cross-sectional area of 1mm^2, then the space charge capacitance for an applied reverse voltage of 5.6 volts is _____
(A) 0.26 nF (B) 0.20 nF
(C) 0.50 nF (D) 0.90 nF

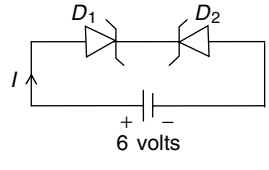
15. For a silicon P^+N Junction, if the diffusion capacitance is 1 nF and diffusion length is 2.6 μm, then the current flowing through the junction is _____.
(A) 1 mA (B) 2 mA
(C) 10 mA (D) 0.01 mA

16.



Assume silicon diodes with reverse saturation current of 10 nA and Zener breakdown voltage of 10 volts. Voltage across diode P_2 is _____
(A) 6 volts (B) 10 volts
(C) 5.96 volts (D) 5.3 volts

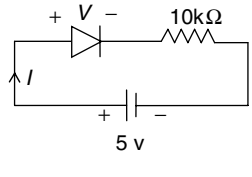
17.



Assume silicon diodes with $I_D = 10$ nA and $V_z = 5$ volts. Then, the current flowing in the circuit 'I' as shown is _____
(A) 2.25 mA (B) 10 nA
(C) 2.25Amp (D) Cannot be determined

18. The zero voltage barrier height of an alloy silicon PN^+ junction is 0.6 volts given $N_A = 5 \times 10^{16}$ atoms per cm^3. Calculate the width of depletion layer for an applied reverse voltage of 5.6 volts.
(A) 0.5 μm (B) 0.4 μm
(C) 4 μm (D) 40 μm

19.



The V–I characteristics of the diode is given as

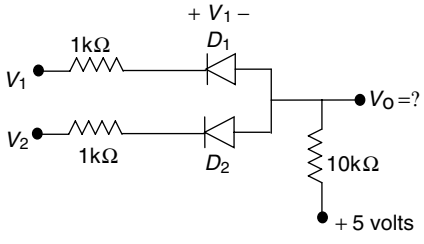
$$I = +0.2\sqrt{V-1} \text{ for } V \geq 1$$

$$= 0 \text{ for } V < 1$$

Calculate the current 'I'

(A) 1 mA (B) 0.1 mA
(C) 0.24 Amp (D) 0.5 Amp

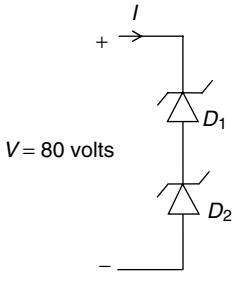
20.



Assume Ideal diodes ($Vr = 0$, $R_f = 0$ and $R_r = \infty$)
If V_1 = 5 volts and V_2 = 0 volts, calculate the voltage drop across D_1 (Polarity is as shown)

(A) 5 volts (B) 0 volts
(C) 0.45 volts (D) 4.5 volts

Direction for questions 21 and 22:



Assume breakdown voltage of each diode is 100 volts.

If the reverse saturation currents of the diodes, D_1 and D_2 are 1 μA and 2 μA, respectively.

21. Calculate the value of I shown

(A) 1 μA (B) 2 μA (C) 3 μA (D) Zero

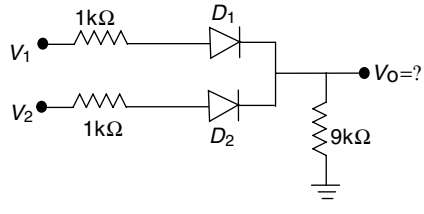
22. Voltage across diode D_1 is (from 'p' to 'n' side)

(A) –36.04 volts (B) 36.04 volts
(C) 79.96 volts (D) –79.96 volts

23. Calculate the doping concentration required for P-type Germanium to have breakdown voltage of 10 volts. Assume breakdown occurs in Germanium at a field intensity of 2×10^7v/m

(A) 10^{16} acceptors/cm^3
(B) 1.78×10^{16} acceptors/cm^3
(C) 3.12×10^{15} acceptors/cm^3
(D) 0.196×10^{15} acceptors/cm^3

24.



Assume the drop across conducting diode is 0.7 volts. If V_1 = 10 volts and V_2 = 5 volts, then V_0 is _____

(A) 8.0 volts (B) 9 volts
(C) 8.3 volts (D) 7.8 volts

25. The zero voltage barrier height of an alloy silicon P$^+$N junction is 0.6 volts, given $N_D = 5 \times 10^{16}$ per cm^3. Calculate the width of depletion layer for an applied forward voltage of 0.5 volts.

(A) 2 nm (B) 51.52 nm
(C) 2 μm (D) 1.5 μm

Practice Problems 2

Direction for questions 1 to 17: Select the correct alternative from the given choices.

1. For what voltage, will the reverse current in a P–N junction silicon diode reach 95% of its saturation value at room temperature?

(A) −0.260 volts (B) −0.156 volts
(C) +0.260 volts (D) +0.156 volts

2. If the reverse saturation current in a silicon P–N junction is 1nAmp. Find the applied voltage for a forward current of 0.5 μA

(A) 0.39 volts (B) 0.25 volts
(C) 0.32 volts (D) 0.42 volts

3. A silicon diode at room temperature conducts 5 mA at 0.7 volts. If the voltage increases to 0.8 volts, the diode current is _____

(A) 43.12 mA (B) 34.21 mA
(C) 21.34 mA (D) 12.43 mA

4. Calculate the factor by which the reverse saturation current of a Germanium diode is multiplied, when the temperature is increased from 25 to 100°C.

(A) 90 (B) 181 (C) 120 (D) 150

5. An ideal Ge diode at room temperature has a static resistance of 4.57Ω at a point, where I = 43.8 mA. Find the dynamic resistance for a forward bias of 0.1 volts.

(A) 28Ω (B) 56Ω (C) 280Ω (D) 560Ω

6. Find the resistivity of the P-type material in a Si P–N junction, where cross-sectional area is circular and of 40 miles in diameter and the transition capacitance is 61 pF, The given barrier height is 0.35 volts and the applied reverse voltage is 5 volts.

(A) 4Ω-cm (B) 3.5Ω-cm
(C) 3Ω-cm (D) 4.5Ω-cm

7. The transition capacitance of an abrupt P–N junction is 10pF at 4 volts. Find the decrease in capacitance for a 0.5 volt increase in bias.

(A) 0.91 pF (B) 9.428 pF
(C) 10 pF (D) 0.57 pF

8. Calculate the width of depletion region of a P–N junction under open circuit, when doped equally on both sides with 10^{21} atoms/m^3. Assume built in potential of 0.2 v and $\varepsilon_r = 10$.
(A) 66 μm (B) 66 nm
(C) 6.6 nm (D) 0.66 μm

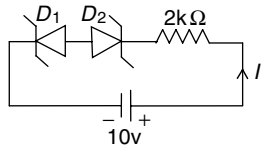
9. Static and dynamic resistances of a P–N junction Germanium diode, if the temperature is 300°K and $I_o = 1$ μA, for an applied FB of 0.2 volts.
(A) 91.324 Ω, 11.872 Ω
(B) 11.36 Ω, 88 Ω
(C) 11.36 Ω, 44 Ω
(D) 44 Ω, 11.36 Ω

10. The diffusion capacitance of a silicon diode with $N_A >> N_D$, when carrying a current of 1 mA, is _____. Assume diffusion length of holes is 0.026 cm.
(A) 0.65 μF (B) 1 μF
(C) 6.5 μF (D) 8.5 μF

11. Zener breakdown occurs in a Ge at a field intensity of 2×10^7 v/m. Find Zener breakdown voltage, V_z, for pure Ge.
(A) 2.3 kV (B) 23 volts
(C) 14.166 kvolts (D) 230 volts

12. Calculate the Zener breakdown voltage of *P*-type Ge with doping concentration of 1 in 10^8 Ge atoms. Assume Breakdown occurs in Ge at a field intensity of 2×10^7v/m.
(A) 162 volts (B) 188 volts
(C) 132 volts (D) 138 volts

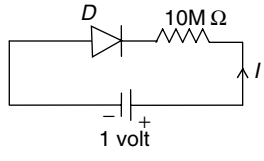
13. If the diode breakdown voltage is 7 volts and its reverse saturation current is 10 nA, then (i) the current '*I*' shown is _____. Assume $V_D = 0.7$ volts under Forward Bias.



(A) 1.2 mA (B) 1.5 mA
(C) 2 mA (D) 1.15 mA

14. If the breakdown voltage of diode is 15 volts, then the value of *I* shown is _____
(A) 1.15 mA (B) '0'(zero) mA
(C) 10 nA (D) 20 nA

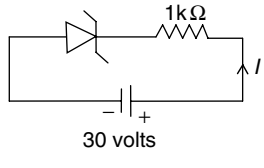
15. If the reverse saturation current of diode is 30 nA, then voltage across the diode is _____



(A) 0.3 volts (B) 0.7 volts
(C) zero (D) Cannot be determined

16. Calculate the barrier capacitance of a Germanium P–N junction, where area is 0.5 mm × 0.5 mm and space change thickness is 3×10^{-4} cm.
(A) 12 pF (B) 16 pF (C) 10pF (D) 8 pF

17.



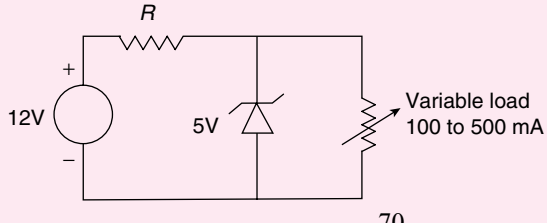
If the diode has reverse saturation current of 10 nA and breakdown voltage of 10 volts, then the current *I* as shown in the circuit is _____
(A) 10 nA (B) zero
(C) 20 mA (D) 30 mA

Previous Years' Questions

1. In an abrupt P–N junction, the doping concentration's on the *p*-side and *n*-side are $N_A = 9 \times 10^6/\text{cm}^3$ and $N_D = 1 \times 10^6/\text{cm}^3$ respectively. The P–N junction is reverse biased, and the total depletion width is 3 μm. The depletion width on the *p*-side is **[2004]**
(A) 2.7 μm (B) 0.3 μm
(C) 2.25 μm (D) 0.75 μm

2. Consider an abrupt junction. Let V_{bi} be the built -in potential of this junction and V_R be the applied reverse bias. If the junction capacitance (C_j) is 1 pF for $V_{bi} + V_R = 1$ V, then for $V_{bi} + V_R = 4$ V, C_j will be **[2004]**
(A) 4pF (B) 2 pF
(C) 025 pF (D) 0.5 pF

3. In the voltage regulator shown below, the load current can vary from 100 mA to 500 mA. Assuming that the Zener diode is ideal (i.e., the Zener knee current is negligibly small and Zener resistance is zero in the breakdown region), the value of *R* is **[2004]**



(A) 7 Ω (2) 70 Ω (C) $\frac{70}{3}\Omega$ (D) 14 Ω

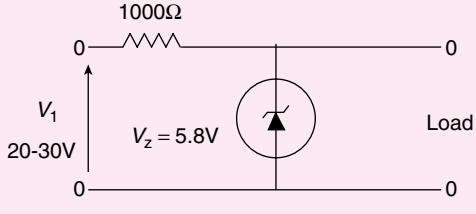
4. A silicon P–N junction at a temperature of 20°C has a reverse saturation current of 10 pico Amperes (pA). The reverse saturation current at 40°C for the same bias is approximately. **[2005]**

(A) 30 pA (B) 40 pA (C) 50 pA (D) 60 pA

5. A silicon P–N junction diode under reverse bias has depletion region of width 10 μm. The relative permittivity of silicon, $\varepsilon_r = 11.7$ and the permittivity of free space $\varepsilon_0 = 8.85 \times 10^{-12}$F/m. The depletion capacitance of the diode per square meter is **[2005]**

(A) 100 μF (B) 10 μF
(C) 1 μF (D) 20 μF

6. The Zener diode in the regulator circuit shown in figure has a Zener voltage of 5.8 volts and a Zener knee current of 0.5 mA. The maximum load current drawn from this circuit ensuring proper functioning over the input voltage range between 20 and 30 volts is, **[2005]**

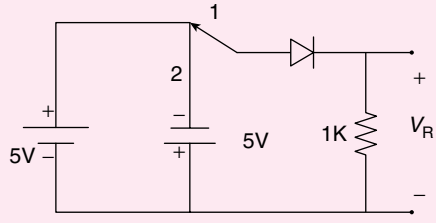


(A) 23.7 mA (B) 14.2 mA
(C) 13.7 mA (D) 24.2 mA

7. The values of voltage (V_D) across a tunnel diode corresponding to peak and valley currents, are V_P and V_V, respectively. The range of tunnel diode voltage V_D for which the slope of its I–V_D characteristic is negative would be **[2006]**

(A) $V_D < 0$ (B) $0 \le V_D < V_P$
(C) $V_P \le V_D < V_V$ (D) $V_D \ge V_V$

8. In the circuit shown below, the switch was connected to position 1 at $t < 0$ and at $t = 0$, it is changed to position 2. Assume that the diode has zero voltage drop and a storage time t_s. For $0 < t \le t_s$, V_R is given by (all in volts) **[2006]**



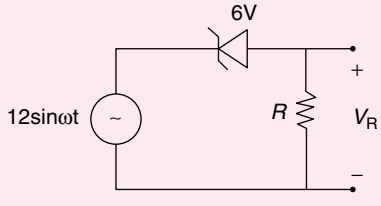
(A) $V_R = -5$ (B) $V_R = +5$
(C) $0 \le V_R < 5$ (D) $-5 < V_R < 0$

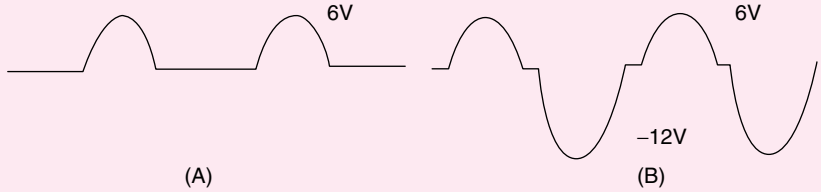
9. Find the correct match between Group 1 and Group 2. **[2006]**

Group I		Group II	
(E)	Varactor diode	(1)	Voltage reference
(F)	PIN diode	(2)	High-frequency switch
(G)	Zener diode	(3)	Tuned circuits
(H)	Schottky diode	(4)	Current-controlled attenuator

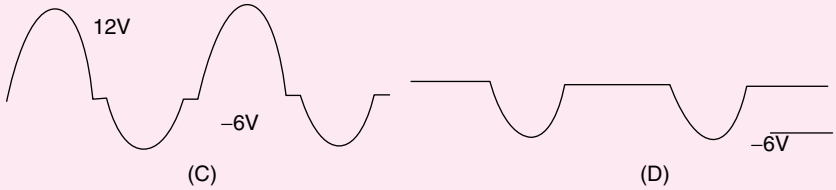
(A) E – 4, F – 2, G – 1, H – 3
(B) E – 2, F – 4, G – 1, H – 3
(C) E – 3, F – 4, G – 1, H – 2
(D) E – 1, F – 3, G – 2, H – 4

10. For the circuit shown below, assume that the Zener diode is ideal with a breakdown voltage of 6 volts. The wave form observed across R is: **[2006]**





(A) (B)

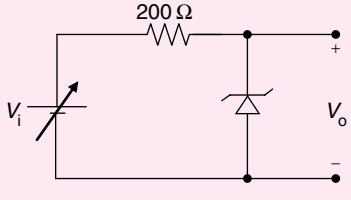


(C) (D)

11. In a P^+n junction diode under reverse bias, the magnitude of electric field is maximum at **[2007]**
(A) The edge of the depletion region on the *p*-side
(B) The edge of the depletion region on the *n*-side
(C) The P^+ n junction
(D) The centre of the depletion region on the *n*-side

12. A P^+n junction has a built in potential of 0.8 V. the depletion layer width at a reverse bias of 1.2 V is 2 μm. for a reverse bias of 7.2 V, the depletion layer width will be: **[2007]**
(A) 4 μm (B) 4.9 μm
(C) 8 μm (D) 12 μm

13. For the Zener diode shown in the figure, the Zener voltage at knee is 7 V, the knee current is negligible and the Zener dynamic resistance is 10 Ω. If the input voltage (V_i) range is from 10 to 16 V, the output voltage (V_0) ranges from **[2007]**



(A) 7.00 to 7.29 V (B) 7.14 to 7.29 V
(C) 7.14 to 7.43 V (D) 7.29 to 7.43 V

14. Which of the following is NOT associated with a P–N junction? **[2008]**
(A) Junction capacitance
(B) Charge storage capacitance
(C) Depletion capacitance
(D) Channel length modulation

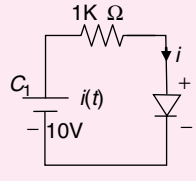
15. Consider the following assertions
S_1: For Zener effect to occur, a very abrupt junction is required
S_2: For quantum tunnelling to occur, a very narrow energy barrier is required
Which of the following is correct? **[2008]**
(A) Only S_2 is true.
(B) S_1 and S_2 are both true but S_2 is not a reason for S_1.
(C) S_1 and S_2 are both true and S_2 is a reason for S_1.
(D) Both S_1 and S_2 are false.

16. Compared to a P–N junction with $N_A = N_D = 10^{14}/cm^3$, which one of the following statements is TRUE for a P–N junction with $N_A = N_D = 10^{20}/cm^3$? **[2010]**
(A) Reverse breakdown voltage is lower and depletion capacitance is lower
(B) Reverse breakdown voltage is higher and depletion capacitance is lower
(C) Reverse breakdown voltage is lower and depletion capacitance is higher
(D) Reverse breakdown voltage is higher and depletion capacitance is higher

17. A silicon P–N junction is forward biased with a constant current at room temperature. When the temperature is increased by 10°C, the forward bias voltage across the P–N junction **[2011]**
(A) increases by 60 mV (B) decreases by 60 mV
(C) increases by 25 mV (D) decreases by 25 mV

18. A Zener diode, when used in voltage stabilization circuits, is biased in **[2011]**
(A) reverse-biased region below the breakdown voltage
(B) reverse breakdown region
(C) forward-biased region
(D) forward-biased constant current mode

19. The *I–V* characteristic of the diode in the circuit given below are

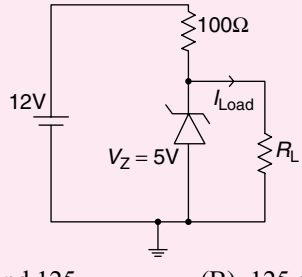


$$I = \begin{cases} \dfrac{V-0.7}{500}\text{A}, & V \geq 0.7\text{V} \\ 0\text{A}, & V < 0.7\text{V} \end{cases}$$

the current in the circuit is **[2012]**
(A) 10 mA (B) 9.3 mA
(C) 6.67 mA (D) 6.2 mA

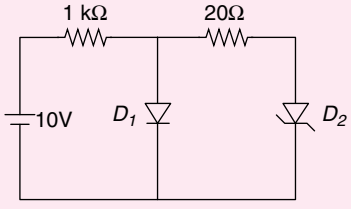
20. In a forward biased P–N junction diode, the sequence of events that best describes the mechanism of current flow is **[2013]**
(A) injection, and subsequent diffusion and recombination of minority carriers
(B) injection, and subsequent drift and generation of minority carriers
(C) extraction, and subsequent diffusion and generation of minority carriers.
(D) extraction, and subsequent drift and recombinations of minority carriers.

21. In the circuit shown below, the knee current of the ideal Zener diode is 10 mA. To maintain 5 V across R_L, the minimum value of R_L in Ω and the minimum power rating of the Zener diode in mW, respectively, are **[2013]**



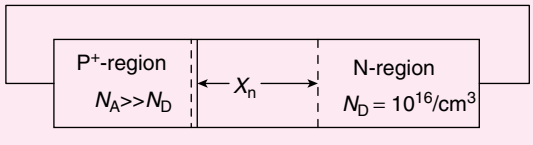
(A) 125 and 125 (B) 125 and 250
(C) 250 and 125 (D) 250 and 250

22. In the figure, assume that the forward voltage drops of the P–N diode D_1 and Schottky diode D_2 are 0.7 V and 0.3 V, respectively. If ON denotes conducting state of the diode and OFF denotes non-conducting state of the diode, then in the circuit **[2014]**



(A) both D_1 and D_2 are ON
(B) D_1 is ON and D_2 is OFF
(C) both D_1 and D_2 are OFF
(D) D_1 is OFF and D_2 is ON

23. Consider an abrupt P–N junction (at T = 300 K) shown in the figure. The depletion region width X_n on the n-side of the junction is 0.2 µm and the permittivity of silicon (ε_{si}) is 1.044×10^{-12} F/cm. At the junction, the approximate value of the peak electric field (in kV/cm) is _____. **[2014]**



24. When a silicon diode having a doping concentration of $N_A = 9 \times 10^{16}$ cm^{-3} on p-side and $N_D = 1 \times 10^{16}$ cm^{-3} on n-side is reverse biased, the total depletion width is found to be 3 µm. Given that the permittivity of silicon is 1.04×10^{-12} F/cm, the depletion width on the p-side and maximum electric field in the depletion region, respectively, are **[2014]**

(A) 2.7 µm and 2.3×10^5 V/cm
(B) 0.3 µm and 4.15×10^5 V/cm
(C) 0.3 µm and 0.42×10^5 V/cm
(D) 2.1 µm and 0.42×10^5 V/cm

25. A thin P-type silicon sample is uniformly illuminated with light which generates excess carriers. The recombination rate is directly proportional to **[2014]**

(A) the minority carrier mobility
(B) the minority carrier combination lifetime
(C) the majority carrier concentration
(D) the excess minority carrier concentration

26. The donor and accepter impurities in an abrupt junction silicon diode are 1×10^{16} cm^{-3} and 5×10^{18} cm^{-3}, respectively. Assume that the intrinsic carrier concentration in silicon $n_i = 1.5 \times 10^{10}$ cm^{-3} at 300 K, $\frac{kT}{q} = 26\text{mV}$ and the permittivity of silicon $\varepsilon_{si} = 1.04 \times 10^{-12}$ F/cm. The built-in potential and depletion width of the diode under thermal equilibrium conditions, respectively, are **[2014]**

(A) 0.7 V and 1×10^{-4} cm
(B) 0.86 V and 1×10^{-4} cm
(C) 0.7 V and 3.3×10^{-5} cm
(D) 0.86 V and 3.3×10^{-5} cm

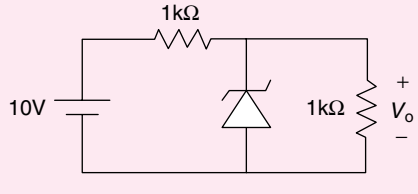
27. Consider two BJTs biased at the same collector current with area $A_1 = 0.2\ \mu m \times 0.2\ \mu m$ and $A_2 = 300\ \mu m \times 300\ \mu m$. Assuming that all other device parameters are identical, kT/q = 26 mV, the intrinsic carrier concentration is 1×10^{10} cm^{-3}, and $q = 1.6 \times 10^{-19}$ C, the difference between the base-emitter voltages (in mV) of the two BJTs (i.e., $V_{BE1} - V_{BE2}$) is _____ **[2014]**

28. A region of negative differential resistance is observed in the current voltage characteristics of a silicon PN junction if **[2015]**

(A) both the P region and the N region are heavily doped
(B) the N region is heavily doped compared to the P region
(C) the P region is heavily doped compared to the N region
(D) an intrinsic silicon region is inserted between the P region and the N region

29. A silicon sample is uniformly doped with donor-type impurities with a concentration of 10^{16}/cm^3. The electron and hole mobilities in the sample are 1200 cm^2/V-s and 400 cm^2/V-s, respectively. Assume complete ionization of impurities. The charge of an electron is 1.6×10^{-19} C. The resistivity of the sample (in Ω-cm) is _____. **[2015]**

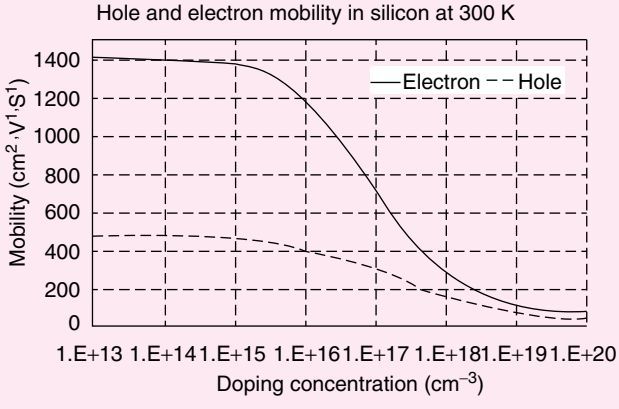
30. In the circuit shown below, the Zener diode is ideal and the Zener voltage is 6 V. The output voltage V_o (in Volts) is _____. **[2015]**



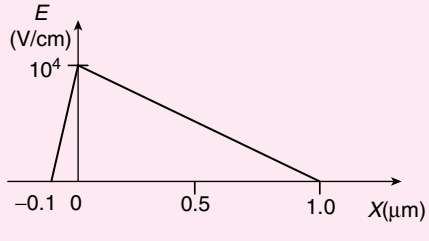
31. For a silicon diode with long P and N regions, the acceptor and donor impurity concentrations are 1×10^{17} cm^{-3} and 1×10^{15} cm^{-3}, respectively. The lifetimes of electrons in P region and holes in N region are both 100 µs. The electron and hole diffusion coefficients are 49 cm^2/s and 36 cm^2/s, respectively. Assume kT/q = 26 mV, the intrinsic carrier concentration is 1×10^{10} cm^{-3}, and $q = 1.6 \times 10^{-19}$ C. When a forward voltage of 208 mV is applied across the diode, the hole current density (in nA//cm^2) injected from P region to N region is _____. **[2015]**

32. An *n*-type silicon sample is uniformly illuminated with light which generates 10^{20} electron-hole pairs per cm^3 per second. The minority carrier lifetime in the sample is 1 μs. In the steady state, the hole concentration in the sample is approximately 10^x, where x is an integer. The value of x is _____. **[2015]**

33. A piece of silicon is doped uniformly with phosphorous with a doping concentration of $10^{16}/cm^3$. The expected value of mobility versus doping concentration for silicon assuming full-dopant ionization is shown below. The charge of an electron is 1.6×10^{-19} C. The conductivity (in S cm^{-1}) of the silicon sample at 300 K is _____. **[2015]**



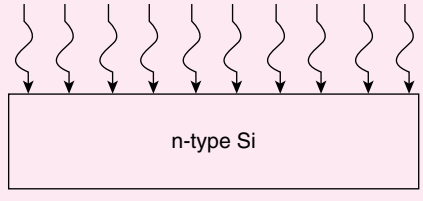
34. The electric field profile in the depletion region of a *p-n* junction in equilibrium is shown in the figure. Which one of the following statements is NOT TRUE? **[2015]**



(A) The left side of the junction is *n* type and the right side is *p* type
(B) Both *n*-type and *p*-type depletion regions are uniformly doped
(C) The potential difference across the depletion region is 700 mV
(D) If the *p*-type region has a doping concentration of 10^{15} cm^{-3}, then the doping concentration in the *n*-type region will be 10^{16} cm^{-3}

35. Consider a silicon p-n junction with a uniform acceptor doping concentration of 10^{17} cm^{-3} on the p side and a uniform donor doping concentration of 10^{16} cm^{-3} on the n-side. No external voltage is applied to the diode Given: kT/q = 26 mV, $n_i = 1.5 \times 10^{10}$ cm^{-3}, $\varepsilon_{si} = 12\varepsilon_0$, $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm, an and $q = 1.6 \times 10^{-19}$ C. The charge per unit junction area (nC cm^{-2}) in the depletion region on the p-side is _____. **[2016]**

36. Consider a silicon sample at T = 300K, with a uniform donor density $N_d = 5 \times 10^{16}$ cm^{-3}, illuminated uniformly such that the optical generation rate is $G_{opt} = 1.5 \times 10^{20}$ $cm^{-3}s^{-1}$ throughout the sample. The incident radiation is turned off at t = 0. Assume low level injuection to be valid and ignore surface effects. The carrier lifetimes are $\tau_{po} = 0.1$ μs and $\tau_{no} = 0.5$μs.

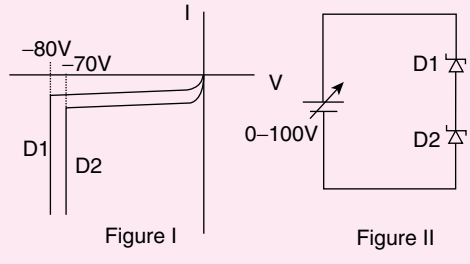


The hole concentration at $t = 0$ and the hole concentration at $t = 0.3$μs, respectively, are **[2016]**
(A) $1.5 \times 10^{13} cm^{-3}$ and 7.47×10^{11} cm^{-3}
(B) 1.5×10^{13} cm^{-3} and 8.23×10^{11} cm^{-3}
(C) 7.5×10^{13} cm^{-34} and 3.73×10^{11} cm^{-3}
(D) 7.5×10^{13} cm^{-3} and 4.12×10^{11} cm^{-3}

37. Consider avalanche breakdown in a silicon P + n junction. The n–region is uniformly doped with a donor density N_D. Assume that breakdown occurs when the magnitude of the electric field at any point in the device becomes equal to the critical field E_{crit}. Assume E_{crit} to be independent of N_D. If the built in voltage of the P^+ n junction is much smaller than the breakdown voltage V_{BR}, The relationship between V_{BR} and N_D is given by **[2016]**

(A) $V_{BR} \times \sqrt{N_D}$ = constant
(B) $N_D \times \sqrt{V_{BR}}$ = constant
(C) $N_D \times V_{BR}$ = constant
(D) $\frac{N_D}{V_{BR}}$ = constant

38. The *I* – V characteristics of the zener diodes D1 and D2 are shown in figure I. These diodes are used in the circuit given in figure II. If the supply voltge is varied from 0 to 100 V, then breakdown occurs in **[2016]**



(A) D1 only
(B) D2 only
(C) Both D1 and D2
(D) None of D1 and D2

Answer Keys

Exercises

Practice Problems 1

1. C	**2.** A	**3.** A	**4.** D	**5.** D	**6.** C	**7.** D	**8.** B	**9.** A	**10.** B
11. A	**12.** C	**13.** B	**14.** A	**15.** C	**16.** C	**17.** C	**18.** B	**19.** C	**20.** D
21. A	**22.** C	**23.** B	**24.** C	**25.** B					

Practice Problems 2

1. B	**2.** C	**3.** B	**4.** B	**5.** A	**6.** B	**7.** D	**8.** D	**9.** A	**10.** B
11. A	**12.** B	**13.** D	**14.** C	**15.** B	**16.** A	**17.** C			

Previous Years' Questions

1. B	**2.** D	**3.** D	**4.** B	**5.** B	**6.** A	**7.** C	**8.** A	**9.** C	**10.** B
11. C	**12.** A	**13.** C	**14.** D	**15.** A	**16.** C	**17.** D	**18.** B	**19.** D	**20.** A
21. B	**22.** D	**23.** 30 to 32		**24.** B	**25.** D	**26.** D	**27.** 380 to 382		**28.** A
29. 0.50 to 0.54		**30.** 5	**31.** 28 to 30		**32.** 14	**33.** 1.8 to 2.0		**34.** C	
35. $-48.36 nC/cm^2$		**36.** A	**37.** C	**38.** A					