Logic Gates

2

Introduction

- Logic gates are most fundamental digital circuit that can be constructed from diodes, transistors and resistors connected in such a way that the circuit output is the result of a basic logic operation performed on the inputs.
- The Boolean '0' and '1' represents the "logic level".

Logic 0	Logic 1
False	True
OFF	ON
Low	High
No	Yes
Open switch	Closed switch

- A "Truth table" is a means of describing how a logic circuits output depends on the logic levels present at circuits input.

Note:

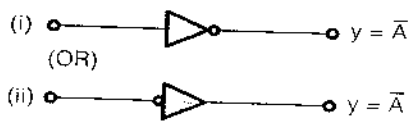
The number of input combinations will equals to '2^N' for an "N-input" truth table.

- The logic Gates can be classified as
  - (a) **Basic Gate:** NOT, AND, OR.
  - (b) **Universal Gate:** NAND, NOR.
  - (c) **Special Purpose Gates:** EX-OR and EX-NOR. They are used in arithmetic circuit, comparators, code conversion, parity generators and parity checkers etc.

NOT Gate

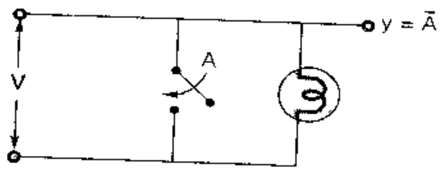
It is also referred as "inversion" or "complementation".

Symbol and Truth Table

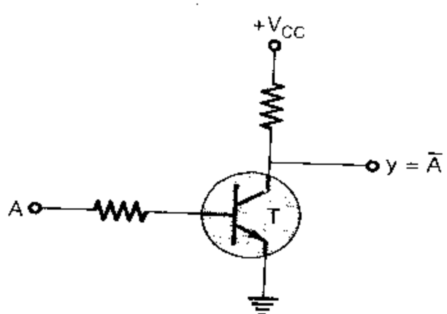


Input	Output
A	y = $\bar{A}$
0	1
1	0

Switching Circuit

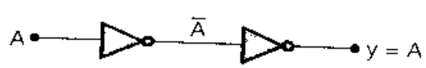


Transistor Circuit

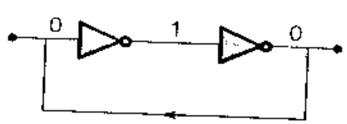


A	T	y
0	OFF	$+V_{CC} \approx 1$
1	0	Ground ≈ 0

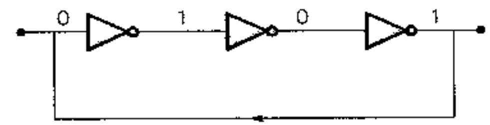
- When even number of NOT Gates are connected in series then it acts like Buffer Circuit.



- When even number of NOT Gates are connected with feedback then it acts like a "Bistable multivibrator". It is also a basic memory element.



When odd number of NOT Gates are connected with feedback, then it acts like an astable multivibrator (AMV) or square-wave generator or clock generator or ring oscillator.



All inverter take some time to get the response 'Y', this time is called propagation delay time (t_{pd}).

For an Astable Multivibrator (AMV)

Time period of Square Wave Generated by AMV:

$$T = 2nt_{pd}$$

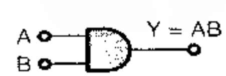
where n = Number of inverters (NOT Gates)

t_{pd} = Propagation delay time of each inverter

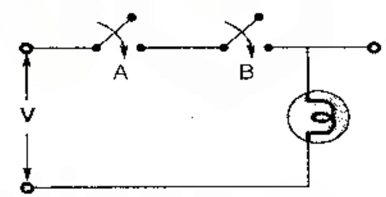
T = Time period of a square wave generated by AMV or Ring oscillator

AND Gate

Symbol, Truth Table and Switching Circuit



Inputs		Output
A	B	Y = AB
0	0	0
0	1	0
1	0	0
1	1	1



Note: ....

In AND operation

- ENABLE INPUT ⇒ Logic '1'
- DISABLE INPUT ⇒ Logic '0'

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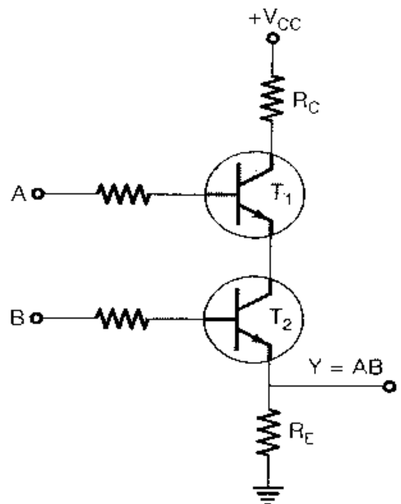
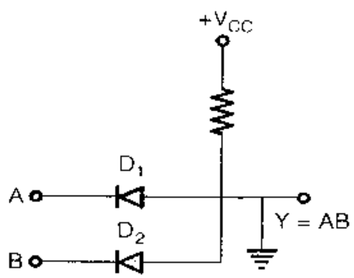
Transistor circuit:



A	B	T_1	T_2	Y
0	0	OFF	OFF	0
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	ON	1

Diode circuit diagram:



A	B	D_1	D_2	Y
0	0	ON	ON	0
0	1	ON	OFF	0
1	0	OFF	ON	0
1	1	OFF	OFF	1

Remember: ....

- In AND gate operation, any unused inputs (Floating inputs) may be connected as:
  Logic'1'for TTL circuit
  Logic'0'for ECL circuit
- AND gate is also known as detector logic

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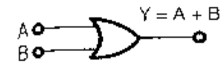
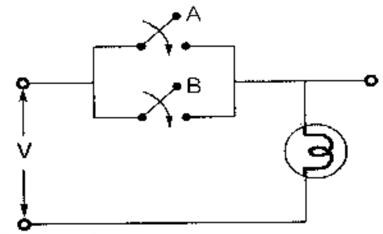
OR Gate

Symbol, Truth Table and Switching Circuit



Inputs		Output
A	B	Y = A + B
0	0	0
0	1	1
1	0	1
1	1	1



Remember: ....

In OR operation

- ENABLE INPUT ⇒ Logic'0'
- DISABLE INPUT ⇒ Logic'1'

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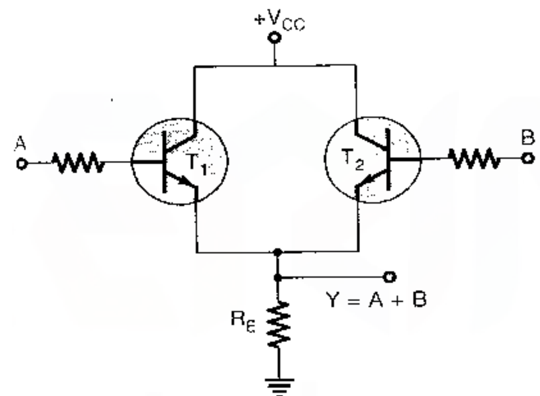
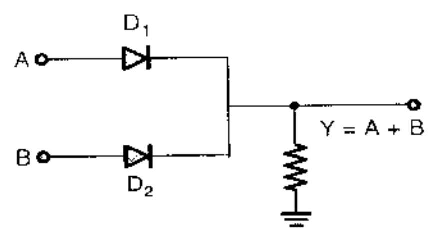
Transistor Circuit



A	B	T_1	T_2	Y
0	0	OFF	OFF	0
0	1	OFF	ON	1
1	0	ON	OFF	1
1	1	ON	ON	1

Diode Circuit Diagram

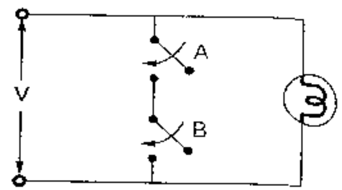


A	B	D_1	D_2	Y
0	0	ON	ON	1
0	1	ON	OFF	1
1	0	OFF	ON	1
1	1	OFF	OFF	0

NAND Gate

Symbol, Truth Table and Switching Circuit

Inputs		Output
A	B	Y = $\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

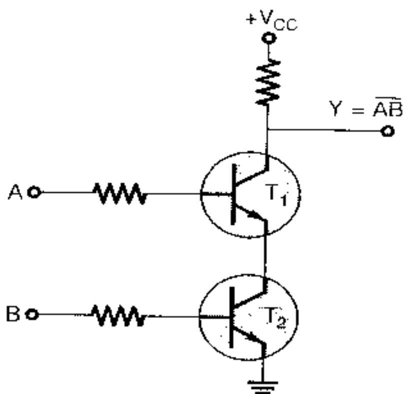


Remember: ....

In NAND operation

- ENABLE INPUT ⇒ Logic'1'
- DISABLE INPUT ⇒ Logic'0'

Transistor Circuit

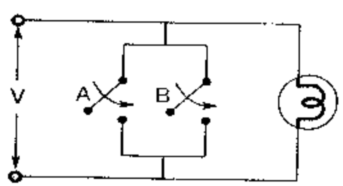


A	B	T_1	T_2	Y
0	0	OFF	OFF	1
0	1	OFF	ON	1
1	0	ON	OFF	1
1	1	ON	ON	0

NOR Gate

Symbol, Truth Table and Switching Circuit

Inputs		Output
A	B	Y = $\overline{(A + B)}$
0	0	1
0	1	0
1	0	0
1	1	0

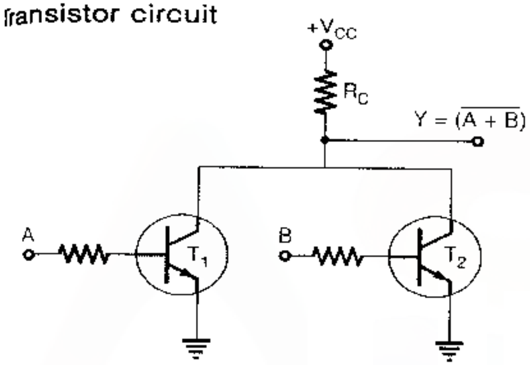


Remember: ....

In NOR operation

- ENABLE INPUT ⇒ Logic'0'
- DISABLE INPUT ⇒ Logic'1'

Transistor circuit



A	B	T_1	T_2	Y
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	ON	0

EXOR Gate

It is also called "stair case switch".

Symbol and Truth Table

Inputs		Output
A	B	Y = A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

❑ Boolean function of 2-input EXOR operation

$$Y = A \oplus B = \bar{A}B + A\bar{B}$$

Remember: ....

- It acts as "odd number of 1's detector in the input".
- It is mostly used in "parity generation and detection".
- When both the inputs are same, then output becomes LOW or Logic'0'.
- When both the inputs are different, then output becomes HIGH or Logic'1'.
- In EXOR operation
  - (i) For BUFFER CIRCUIT ⇒ Logic'0'
  - (ii) For INVERSION CIRCUIT ⇒ Logic'1'

Note: ....

$$\boxed{\begin{array}{ll} A \oplus A = 0, & A \oplus 0 = A \\ A \oplus \overline{A} = 1, & A \oplus 1 = \overline{A} \end{array}}$$

- $A \oplus A \oplus A \oplus$.........upto n terms = 0, when n = even
  = A, when n = odd

....

EXNOR Gate

- It acts as "even number of 1's detector".
- It is also called "Gate of equivalence" or "coincidence logic".

Symbol and Truth Table

Inputs		Output
A	B	Y = A ε B
0	0	1
0	1	0
1	0	0
1	1	1

❑ Boolean function of 2-input EXNOR operation

$$\boxed{Y = A \odot B = \overline{A \oplus B} = \overline{(\overline{A}B + A\overline{B})} = AB + \overline{A}\,\overline{B}}$$

Remember: ....

- When both the inputs are same, then output becomes HIGH or Logic '1'.
- When both the inputs are different, then output becomes LOW or Logic '0'.
- In EXNOR operation
  (i) For BUFFER CIRCUIT ⇒ Logic '1'
  (ii) For INVERSION CIRCUIT ⇒ Logic '0'

....

Note: ....

$$\boxed{\begin{array}{ll} A \odot A = 1, & A \odot 1 = A \\ A \odot \overline{A} = 0, & A \odot 0 = \overline{A} \end{array}}$$

- $A \odot A \odot A \odot$ .... upto n terms = 1, when n = even
  = A, when n = odd
- $\boxed{\begin{array}{l} \overline{A} \oplus B = A \odot B \text{ and } A \oplus \overline{B} = A \odot B \\ \overline{A} \odot B = A \oplus B \text{ and } A \odot \overline{B} = A \oplus B \end{array}}$

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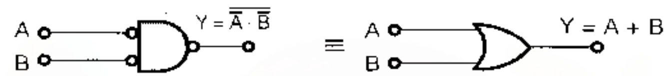
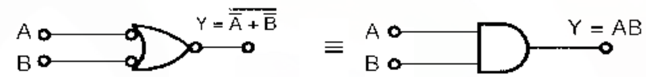
Alternative Symbols of Gates

Bubbled – OR gate ≡ NAND gate

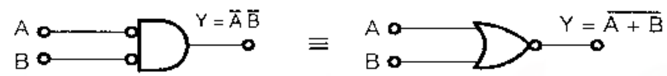
Bubbled – NAND gate ≡ OR gate



Bubble – NOR gate ≡ AND gate



Bubbled – AND gate ≡ NOR gate



NAND and NOR Gate as Universal Gate

Logic gates	No. of NAND gate required	No. of NOR gate required
NOT	1	1
AND	2	3
OR	3	2
EX-OR	4	5
EX-NOR	5	4