Sequential circuit • INTRODUCTION of Sequential circuit --In sequention logic circuit the opp is depent on upon the present i/p as well as the past I/p and output. O/P-> I/p. combinational arcuit Memory element Sequential cincuit Synchronous Asynchronous sequential cut sequentias unt chang in i/p cignals change En Yp cignals can Can effect memory elements effect memory elements at any only upon activation of your Instant of time. These are fuster Lignars than cynchronous CKt. Pp VP Combi-Combinah ع onal TUKE CKt CLOCK -> Memor element - Delay (Clock sequention unt) > The storage elements (memory) used in clocked sequential > flip flop is a one bit memory cell which stores the 1-bit signar data (logic 'o'ore logic 1').

classmate Data Paga 114_ > In cynchronous sequential circuit, memory elements are clocked flip-flop and generally edge triggerred, > In Asynchronous requestion circuit, memory elema ents are unclocked flip-flop/time delay eliments which are generally level triggered. -> flip-flop circuit is also known as bistable multivibrator or latch because it has two stable state (1 state, O state). +ve edge -ve edge clock. CLOCK · Storrage Elements = ~ Latebes . ---- (SR latch , D latch) - flipflops. -> (SR, JK, D, T). " A storage Eliments in a digital circuit can mainmantain a binary state indefinitely as long as power is delerere to the circuit, until directed by an i/p signal to switch states. Do D Bistuble element

LASSMACE. Page 115 Latchesla Storage elements that are operate with signay levels are rufferend to as "Latches" (Latches are level sensitive) CLOCK -> Latches are used in aunchronous sequential incuit for storing binary information and for the design. · Flip-Acpo storage elements that are controlled by a clock transition are the flop. +ve edge curck 1 11 11 (415 p-Plop are edge sensitive) edge adia > SR-Latch (set - Reset Latch) (1) <u>SR Latch wing NOR gate</u> 2 Q 8 (next state) S (legic dragmam) Function table. Symbol -R 2 03 03 8 S No change 0 0 0 T 1 0 0 0 σ undefined state or forbidden state.

CLASSMAN Deta. Poge 116 (11) SR-Latch wing NAND gates -5 3 B (logic diagream) Function table -2 R 03 0 > forebidden state 0 Ø 1 0 1 0 ** . 0 0 1 1 > NO champe 1 Opposite of function fable of SR latch ming NOR gate. . Symbol -8 S R B uning (ontro) inpute (11) SR-Latch (a) using NOR gates AND 3 n En -Q NOR AND

	5 D					Page III C		
	Opercation -							
	When En=	0 (8	23.	oill re	mains	In previous state)		
	En=1	WS		B No-	(hang	٤		
				0	1	-		
	Cymbol-			Line	eline	-> for hidden state.		
	\$	Q B		isting)				
	₽ <u></u> ₽	Sint-		1	- 420.22 - 1 2 2-			
	(b) wing NAND gate -							
	SDo			- &				
	R-D-	R	\geq	- 8	6			
6. 9. a.e.	Operation- When En=	o, (0	१४छ	temo	u'ns i°	n previous state)		
	Ene	1 VUS	B	B	ā			
11		C	0			> No - change		
				0	0	<u> </u>		
						> forbidden stat		
	Supmbel - En-	S 8 -	- ¹⁹ 15 - 1	×	(

Pege 118 • D-Latch (Transparent Latch) -= (Delay Latch) (S) D or B \$ En -03 (B) 5-> To tumore undefine state we use D-Latch Eunction_table-En 03 D 03 Previous state 0 х 0 1 0 D ۱ Symbol -D 3 0 En · D-latch with preset & clean T/p's -- lasynchronous 1/23 pro (active low i/p) D 03 0 to (active low i/p) Pr=0 → 0 =1 (cet state) CI=0 -> O = 0 (rent state) in the god of

Page 119 0 pr =0 0 2) -Q=1 0=0 D. En 8=1 $\Theta = 0$ b $Q\overline{u}=0$ auguchnomous i/p because - will - Copenation of the i/pA not depend on the i/p of D & En) aug · ELip- Flop ---There are '4'- types of flip-flop -(1) S-R - flip flop. (11) J-K-flip flop. (11) D - flip flop. (IV) T - lip Hop. * Clock tresponse in Latch -(1) response to positive level. (1) response to negative sevel. *. clock thespone in flip - flop --() Positive edge tresponse. 01) negetive edge tresponse

Jassmate Data Paga 120 · SR-Slip-flop = 8 S S 3 CIK-05 R ō R -ve edge SR-FF. the edge SR-FF 5-2 8 CIK - 5 R Truth Table / Function Table . CK R 03 B S X D Х NO change NO Change D 1 0 \uparrow 0 -1 0 1 1 0 1 0 1 Forhidden State 1 1 1 Characteristic table. Next.S Pos Om R 8m+1 5 0 0 0 0 ۱ 0 0 0 1 0 0 1 1 forbidden state. 0 ۱ 1 01 01 0 1 1 0 0 DJ ١ 1 1 forhidden state. 1 1 1

classmate Date_ - ---Page 121 Charactenistic equation -Onti = S+ On R Kmap SR om 01 11 10 X Q 0 0 1 1) Ix 0 T 1 Excitation table -Om Om+1 R S 0 0 Х O -١ 0 Ø 1 . 0 0 1 X 0 · J-K - flip-flop == 0, 1 3 1 uk-CIK 8 0 K ž ter edge #JK-FF -ov edge JK-FF. Logic Diagram. のうつ J b CUK -8=1 K-I

1	in state					Ç	Data Paga 122
	functi	on tuble	_	-	1		
	[LIK]	JK	o a	-		11	
	0	XX	No-tham	-	1997 - 19	7 1903	
	\uparrow	0 0	No-chan		1.10		
	9	0 1	6 1	8			
		1 0	1 0				
		1 1	previous	state com	priment.	1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1	
				-	<u>v.</u>	2.12	
	Charco	utenistic	table -	-		4	
	Om	1	K	Bn+1		a di a	
	0	0	0	0			
	0	D	1	C		0.55	
	0	1	0	1			
	σ	100	10 100 100	14			
	81	0	0	Ĵ		7.	
)	٥	1	Ø			
	1	1	0)			
	J	1		0	PERCENT F		
		$a_{1} = 0,$		ati <u>on -</u> nJ	-		
			Sy har	and the	Sapar St.		
	Kma	p1	6	3. THE			. 1
		and	5 00) (1	10	~	
		0	0 0		DI	-	
		· ī	D	0 0		•	
	Excitation	on tak	re-	1			1
			Onti	IIK	T - Maria		
		0	0	0 X		1	
		0	1	IX			· · · · · · · · · · · · · · · · · · ·
		1	0	XII			

Page 123 · D-Fuip-flop == D 0 03 D cik-CIK-0 03 negative edge)-FF positive edge D-FF logic Diagram -D 00 1)0-CHAK 03 Function Tuble -. \$ CIK By Bn+1 D No change X 0 0 0 1 1 0 1 Characteristic Table -Ł Characteristic equation -On+1 on D 0 0 O 1 l On+= D. 0 0 0 1 1 Excitation Table anti D Bn 0 0 0 9) 0 0 1 0

classmate Dete 124 • T-FF (Toggle FF) --3 T 3 T CIK CIK-B 03 negative edge T-EE. Positive edge T-FF logte d'agram -2 8 CIK a Function table onti CIK T On_ No change (37) X 0 D T No change (om) to. previous tos tate compliment (30) 1 Characteric be Jable. Bm+1 Characterichic equation -Om T 0 0 D のカキノ= ろカナ + あカナ= のかモナ ١ 1 0 1 0 1 0 (1)0 0 $\widehat{\mathbf{H}}$ 0 Exuitation Table -Bn Om+1 T 0 0 0 1 0 0 t ۱ 0 1

JASSMACE. · Conversion of this Hops --> characteristic table of travined FF. -> Excitation table of existing FE. · Function Table of all FFS --S R Bn+1 10n+1 D Brit Bnt T K Sm Sn On D Sn 0_1 0. Sm I · Excitation table of all the FF3 -A ALL Som Sm+1 R T D K X Ð X X l X × X) (Example - 1) SR-FF to JK-FF: Required - FF Existing-FF Bin R J Sm+1 S K X X XO X Ĩ

classmate Page 12.6 S JK 00 R 0) NKOO 10 11 01 11 10 0 0 D On 1 T 0 X 8 X 0 0 1 X 0 X D 0 ١ S= Onj R=ByK. Block Diagrom Or 5 · On CIK R On - On Example - 2 SR to D-FF : D Bn Bm+1 R S 0 0 0 0 X 1 ۱ 0 1 0 0 0 D 1 ۱ X D 1 5 Do On P On 0 1 0 R 0 1 0 D 0 lx 0 R=D S = @00 D Block Diagram S D Bri CIK Bn

Page 127 1-1-1 Example - 3 JK-FF to SR-FFO Bn K S R On+ S X 0 0 0 0 0 X 0 1 0 0 0 X 01 ١ 1 D 0 X x 1 1 X 0 0 X Ø 1 0 D ۱ × 0 1 0 1 D × 1 0 1 1 X X 1 X t 1 m K -----8n/5800 01 SROO 11 10 10 01 11 Br X X X X D TX 1 O 0 0 : 0 D x X x × 1 K=R J= 5 4.1 Block Diagram 5 Br - 4 5 CIK-Ð om K R Example - 9 J-FE to D-FF ? D Omti T Bm D 0 Omo (ī 0 6 0 0 0 1 1 ۱ 1 0 $T = \overline{B_n} D + \overline{B_n} \overline{D}$ 0 1 D 1 1 1 (8n⊕D 0 -

C1455204524 128 Block Diagram -D. Bn T On CK-OTC · On DI Om T . Bn Bn UK-· RACE AROUND CONDITION ? -> It occurs in level thiggered JK-flip flop. function table -0 Ŧ CIK (OT) Onti K J ā En K om 0 0 0 0 ۱ 1 Race arround 0 1 By condition (Timing Diagram -Next page CAR

classmate Page 129 Apd << Tak -> the level trigand. CIK + riggered y Tork K J=1 K=t 1 Byti fale atount Condition. i.e when J=K=1 and too << Terk the state of the flip-flop will oscillates between 'o' &' and at the end of the clock ptu pulse, the FE state is uncertain, • This phenomenem & called Race around condition". Avoid race around condition --> Master-Slave level truggered JK-FF. z > tpd> Tax. Masker-Slave JK-FF -== Master Slave \$ Js as B Bn JM J 0,m Bs an KS KM. K-DO aK

classmate 130 Operation = (1) CLK=1, Master is in operating mode store is in off mode (017) retains previous state. (LK=0, Master is in off mode (00 retaining. (1)pruvious mon state; slave is in operating mode. (-veedge triggerud)-Logic diagram = 8n=0 8n=1 K CIK=0 (-ve edge truggered FF) When CLK= 0, then slove to active & and we get result So, It is -ve edge triggered FF. · Master-salare D Flip-Flop -= (OR) D-FF (OR) Edge truggered)-FF. problem with D-Latch = Eunction Table-3 D Bn B D CIK (017) 0 0 En 1

classmate Date _____ Page __1 3] ____ > +ev level +riggened cik. CIK 2 D output cambe o'or 1? 05 Mastik slave D.F.F = DM D latch Conasten) D. DS D lateh B (Slave) En En CIK = 0 TIK Operation -> cik=1 (logic-1 level). - the external data Dip is transfettred to the master. But slave is disabled (: cik = 0) because its enable i/p is =0 -> when clk=0, the master latch is disable, and the slave latch is anable (at =1) and its output of Is equal to the master output y. 4 behaviour of the master-slove FF dist dictates that -(3) The o/p may change only once. (b) a change in the o/p is truggered by the negative edge of the clock. (c) the change may occur only during the clark's -re level

132 Internal logic diagram Master -> D-L SR-Latch & Slave atch) 0, En B CIK ve edge triggered D-FF) ŝ . . ż

classmite 132 · COUNTER: 4 countere is requential logic citauit capabel to counting the number of clock pulses arriving at its clock 1/p OT "A counter is a set of FF whose states changes in response to cloux pulses applied at the 1/p to the counter? -> A counter consured to as a frequency divider. -> with n-FFs maximum possible states in the counter is 2m N S 2 n -> np. of FFS. N > no. of states. > modules of the Counter. Ex: m=2 -> NX9 -> Mod 4 Counter. m=3 ~~ N 523 ~ N 8 ~ mod 5 counter I) Mod 6 counter, EX: MOD 16 counter, find n=9 here. $28 N \leq 16 \qquad m = 4$ N\$24 Ex: MOD 6 counter, find n= 9 here, NS23 n=3 (minimum).

decompte. Page 134 > +/ (Divide by N Counter) \rightarrow Mod 'N' £ counter ex: -1/6 f Mod'6 ModM MOJ N 111 ₽/mn MOJMH ex: 4/80 FMOD10 [MOD 8] • Types of counter = Depending on the clock pulse applied counters of two type: > A cynchronous Counter.or (ripple Counter). Lynchtonous_counter. \rightarrow BI 82 Oru J2 03, JI B, Jo 8,0 100 ō, Ko ā K2 (Asynchronous counter) CIK TZ BJ 73 83 TI B. 1 a 8, B CLK (Synchronous Counter)

Page 135 Lynchnonous counter. · Asynchitonous counter > In this type of counter FFs are In this type of counterconner - tion blod counter there is no connected in such a way that connection b/w the o/p of the Up of 1st FE drives the clock for the 2nd FF, the op of 1st FE & Clock i/p of next the 2nd will be the clock of 3nd FF and so on. FF and so on. > All the FFS are not clocked > All the FFS are clocked simultanearly. simultanearly. > Design ale Implementation -> Design and Implementation ic very cimple even for becomes complex as the no. of states increases. more no. of the states -> Low speed. -> High speed = · A cynchronous / Ripple Counteres --> 2-bit counter -> mp. of FFS = 2 n=2 -> 2n= 4 -> MOD - 4 counter. (0, 1, 2, 3) counting requence 6-1,2,3 (up-counter) counting requence 3,2,1,6 (Down - counter) > JK-FF and T-FF are use of Ast Asynchromous counter. On+1 Bnti K On 0 6 Om D O Bn D) Bn Toggle state

CLASSMALE

D Papa _136_ JK-FF T-FF 1 3 S 1 2 5 B megetive_edge truggened. CIK -ve edge miggened CIK er (CP) 1 J 3 3 8 3 CIK possitive èdge triggened +ve edge truggeried CHK ore (cp) Nigelive edge IK flip flop 3 > pivide by 2 counter CUK 3 8=17 K CLK 0 0 0 -27-7 0 1 B ١ 0 = \$/2 Truth Table ULK 8 B frag divider initial O 0-1 04 13 1 J 1 0-2 J 3 1 1 0 1 bit counter up down orc counting counting MOD-2 counter.

classmate Page 137 • 2-bit Up counter using negative-edge träggered JK-FF: $n=2, N=2^2=4$ no. of FFs MOD - 4 counter 00 OTC 01) D Divide by 9 counter. J. 8 81 KO B 8 MSB CIK 1SB 0,-B, Do CIK Bo 0 1 1 D 0 ۱ 0 1 0 1 0 0 1 ۱ 0 0 1 0 0 (Lep counting down counding Timing Diagram 3 + += y-CLK l 0,0 0 ٥ ١ 0 0 ←27. 1 B 0 0 1 . 0 1 σ AT. Divide by 4-counter.

821 - 138 · 2 Lit bown - Counter using -ve edge truggened T-Fr: T. D. T, 0, 0.1 0, CLV 0,0 . O Dio 0.1 ¢ 1 1 a (bown - counting) Jruth tuble ā, Du 0,0. CLK D. 1 . V V (Down counting)

dissuite Page 139 · 2-bit Up-counter using the edge - triggered J-FF -= T₀ -7, FFO OSD FFIBI CLK CIK 030 0 D Bo.0 8,0 Truth Table = B1 O.D CLK Bi D up counting MOD-4 Up-counter pivide by 4 counter. 8. $\frac{f/z}{f/z} CLK frequency f = 1 MHZ, using 2-bit counter$ What is 0/p frequency = $<math>\rightarrow f = \frac{1}{2^2} = 1 MHZ.$

Scanned by CamScanner

classmate 140 · 2-bit Down counter wing the edge-miggened JK-EE 1. J. 00 J 81 8, B K CIK CLK 1 0 So. 0 01) ١ 1 S, 1 0 0 0 l Truth Fable = 80 Sp BI CLK So 9 J 0 0 D 1 1 ۱ 17 0 0 I 1 0 0 1 2) 1 0 1 3 0 l 1 0 0 4 1 \$5 1 D Ď Down counter (Mo) -4 counter) 00 01 10 11 Note: $m=2 \rightarrow 2^{m}=4$ >2--3-Up-lount m=3 -> 2" = 3 -er. 1) 10 01 $n=4\rightarrow 2^{n}=16$ 00 23->2->1. 20 Down-count N = 16 er. n-bit counter on MOD-N counter. max no. of states 612 Divide by N counter . = 4/N Scanned by CamScanner

chesnute Dete 141 51-1 Note: ()-ve Edge truggere FF → 8 as clk → Up counter. $(1) - ve_{12} \longrightarrow y \rightarrow B y y \rightarrow Down counter.$ 11 1) -> B 11 1 -> Down 1 (11) +ve " (N) tre " " $\rightarrow \overline{\mathcal{B}}$ " $\rightarrow UP$ " • 3 bit <u>Ripple Counter</u> = (up counter) OR MOD 8 - Ripple Counter (0, 1, 2, 3, 9, 5, 6) TT, sit1 1-172 1 . 82 To 8,0 Ø. ã CLK T=1 CLK -T-> 1 YO to= \$12 0 10 11 0 1 0 1 Bo $f_1 = f_4$ 110 0 0 1 0 11 0 OSI -41 f= fx 10 0 1 -Bz 0 0 0 1 1 8T Truth Table 31 Øp Bo elk On By Do QU. ١ 0 0 0 07 1 1 O l 0 0 1 2 0 0) 1 D $\rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 6$ 1 3 1 0 0 0 1 4 0 0 0 ۱ ١ 0 5 1 1 0 0 1 0 1 6 0 1 0 0 0 0 1. 0 1 1

dissente Da's 142-N=16=29→3 (Pown Asynchronous counter) $\frac{1}{1-k_{0}} = \frac{1}{8_{0}} = \frac{1}{1} = \frac{1}{8_{1}} = \frac{1}{12} = \frac{1}{8_{2}} = \frac{1}{1} = \frac{1}{8_{3}} = \frac{1}{1} = \frac$ CLK CLK_ 1 10 1 10 1 10 10 10 10 10 10 10 00 0 BD 0 1 81 110 01 0 100111001110 0 a la -4T . è B 10 112000011111200 U BL 11 OO -8T-4 91 B, 9-833 1110000 0 0 0 1 0 167 BEDROX i.e

classnate

Pager 14.3

	Truch 7	able (Down A counter)				
	CLK	BB B2 B4 B0				
-	$\rightarrow \circ$ $\downarrow 1$	0 0 0 (0)				
-	12	1 1 1 ((5)				
	V3	1 1 0 (14)				
	14					
	15	0 0 (12)				
			_			
	V 7 V 6	1 0 1 0 (10)				
	1 8	0 0 1 (9)				
	19					
-	1 10	0 1 1 (7)				
·	J II		-			
	VIL	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$				
	1 13					
	J 19					
	↓ 15					
	116	0 0 0 0 (0)				
	MOD	$\frac{16^{2} \text{ counter}}{13 = \frac{4}{16}}$				
<u> </u>	<u> </u>	$l_3 = \frac{4}{16}$.	_			
		The set of				
			_			
Sec. 3			_			
		Seemad by ComSeen				

Classmate Page 149 · Ripple Counter uing D-FF == > FF should be in toggle mode. · 2-bit Pipple counter m=2 01 80 D1 81 Po Do > FF. FFI B 80 CLK Timing Diagram -5 4 CLK 1 0 1 1 80 0 0 1 0 1 0 BI 0 0 Table -031 Bo B, 0,0 CLK 1 0 0t 0 V 1 0 ۱) 0 \checkmark 2 0 1 0) 4 3 1 0 D 1 ↓ 4 l 0. 1 0 1 5 0 L 0 UP Lou MOD-4 Ripple Up counter

classmate Page 145 · 3-bit Ripple Down Counter using the edge truggered D-FF = D2 Qu Do Bo Ð, 0x FF2 Q FF, To, FFOR (MJB) (LSB) CLK 921 Jable Bo 82 81 Bp B1 B0 CLK 1 1 $\rightarrow 0$ 1 0-0 0 D 0 0 1-7 11 1 0 1 1 0 0-2 0 1 1 2 1 0 1-1 1 0 Λ 3 0 0-0 1 4 1 0 0 1 1-7 D 0 1 5 Ø 1 0 1 0-2 6 1 ١ 0 T 1 1-1 0 0 个子 0 1 0 ١ 0 0-0 1 8 7+2->1->0 (MOD-8 Ripple Down counter) · MOD - N Ripple Counter ż modernes JK-FF with preset & clear inpts -> preset (pst) Preset (PST)] J 3 3 CIK-0 0 x clean (LLR) Clean (CLR) (Active high i/P) (Active Low i/p)

classnate) paga 196 10 100 active low i/p active high 1/P PST CIR CIR 03 03 PST -1-1 Ð 0 0 0) 0 1) 0 FF WOTKS X 1 1 0 D X FFWONKS .0 D nonmally • MOD-6 Ripple counter = N < 2 n > no of flip flops. 4 N <23 -> 8 6 < 8 PST= PITEI PST=1 Qt J Jo On 82 J, ō, ō, K2 B. KO K CLR CLR CLK CLR ... 82.01 . 82 . e) 0, Table B 31 CLK හිත >9 0 0. >0 Ð 1>1 D \checkmark 1 0 2 D D >2 1015 CLR=1)3 3 1. 0 4 >4. 1 0 D 110 3 CLR=0 D5 N 1 5 1. 0 SLR 1 V 6 >6 1 0 00 01 1 Ŧ one, -7 10 11 .1 1 ŀ 1 I 0 CLR= B2+B1 82.0 =

	Date Page 197-
 $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Count from 001 to 100. 1->2->3 Count MOD-3 UP Counter
$ \begin{array}{c} 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\$	PST=1 $PST=1$ $PST=1$ $PST=1$ $PST=1$ $PST=1$ $PST=1$ $PST=1$ R
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	B2-D B1-D B0-PST PST PST PST JB2 B0-J1 B1-J0 B1 JB2 B0-J1 B1-J0 B1 LKD B2 LKD B2 LKD B2 LKD B1 LKD B
$\frac{7}{8} \frac{0}{1} \frac{0}{1} \frac{0}{1} \frac{0}{1} \frac{0}{1} \frac{0}{1} \frac{0}{1} \frac{0}{1} \frac{1}{1} \frac{1}$	$4 \rightarrow 3 \rightarrow 7$ p_{own} (ounfett.

classmate Pege 148 MOD-10 Ripple counter 6 MOD-9 Ripple Counter Down counter. $10 \le 2^n = 2^q$ NS2M >Up counter 952m=24 4-FFS 4-FFs BI B2 B2 CIK CLK B2 B1 On 2 Oso-D) 1: l I 丁 P • • • 1, Ø • . . • 1 123 1 Ò CIR CLR X × X X. X 1 2 6.) XB X 12 X X X ID $Q_R = B_3 + 01 = \overline{B_3 B_1}$ CLR (LR TER CLRI CLR= 03+00 = 0300 D KIB CER PST J2 02 Jo of J3 93], B. ō, ō KO B KI B Q. (Decade counter) PCLR ELR TCLR CLR CLK (Divide by 10 country) D 0x

dassmate Date Page 149 14. <u>BCD Ripple Counter</u> (alway up counting) MOD-10 Ripple counter (100) MOD-10 Ripple Counter (01) Decade Counter (OR) Divisible by 10 Ripple Counter. (OTC) BCD Ripple counter. CLR CD 00 10 11 01 CLR CLK AB 6 D AB 1: 1. 1 00 Ø ١ ٥ 0 0 0 1 1. t 1 • 1 0 1 01 6 l 0 x 5× X X 1 0 0 1 11 0 2 X X • 1 1) 1 0 10 0 3 0 1 0 Ó l 4 0 1 CLR = A + 8 l 1 0 5 0 = AP 1 1 1 0 6) 1 1 7 0 1 D 0 0 1 8 1 Ó 1 1 0 1 9 1 0 0 D 10 • 10 J2 83 (A) -3, BI BZ 000 JO (3) (1) CLK Ø, 8, 83 Bo Ko Ko K CLR CER LLR CLR 1

classmate 150 · UP/ Down Ripple Counter = D 2-bit Up/Down Ripple counter = 0-1-2-3 m=2 -> NS2 3->2->1->0 N=4J, 81 Jo 30 > FFI TMUX FFo B) KI 80 ۱ Ko CLK M=0,1 when, M=1, Or will be Output of So will be the clock of second flip-flop. (UP counting) M=0, output of Bo will be the clock of record FF. (Down counting) 30 80 M=0,1 Y= BOM + MBO 4 (same function) M. TO Jo 80 81 7 CLK 80 1. KI BI 1. KD M=0, Up counting. M=1, Down counting.

classmate Date_____ Page___[5]____ (11) 3-bit Ripple Up/ Down Counters ----M=3, $N=2^3=8$ MO 0 2×1 MUT To -T2 82 0,0 BI 0 TI MUX 00 8, Ø CLK When, M=0 (Down counting) M=1 (UP (ounting). · <u>cascading of RPppic counteres</u> ----1. MOD-M > P/ T MOD-N 1 -F->MOD-MN->P/MN. example-(1) - [MOD-6] [MOD-10] > = ->[MOD-60] > \$160 · Drawback of Ripple counter on Asynchronous Counter = -> low speed counters, delay If no of FF- n then, Max pro tot = ntpd. tpd => propagation delay of 1' FF.

classmate () bete Pege 152 (-> If the propagation delay is large compare to clock period, then counter may skip a state. EX-Telk= 1 Msu tpd = 0.5 lice propagation delay. CLK 0 25 1 14 Jew 0 14 04 BO 1 0 0 2400 41 Vo 31 D 46 1 0 D 1 340 8L 0 0 ٥ 0 1 6 -4 Tev TCLK = 1 Juse tpd = 3 * tpd =3+0.5 =1.5 Tak & tpd 20 8, 8, CLK 0 0 0 0 J 0 0 1 0 0 1 2 3 0 1 > skiped D 0 4 0 1 S 1 1 0 6 I 1 1 1 * x for avoid this problem -= tpd= Pro delay of FF. n= no. of FF. Telk / nitpa 1 motpd => fack < n. tpd

classmate 15.3 The! · Synchronous Counteres à · Required steps to design Synchronous Counter= → No. of FFS required. — n=2, N≤2^m=4 → state diagram. — → choice of FF& excitation table of FF. → choice of FF& excitation table of FF. I minimal expressions for the excitations -> de Draw the logic diagram · Design of a Synchronous 2-bit Up counter -= $M = 2 (mo \cdot of FF) + N \leq 2^{M}$ $N \leq 4 \quad 0 \rightarrow 1 \rightarrow 2 \rightarrow 3$ •. (i) no of FF required = 72. (ຳຳ) 100 state diagram. E) 11 10) (ii) Bntt D-FF Bn D 0 0 0) 1 0 0 0 1 1 1 NS PS GV) required excitation Do 8,80 8,80 DI CLK 0 0 1 01 1 0 0 2 01 10 1 ι 10 1 1 3 L 0 0 4 0 0

classmate Page 154 $D_1 = O_1 \overline{O_0} + Q_0 \overline{O_1} = O_0 \oplus O_1$ 0,000 0 10 0 0 0 1 D= Do 0,0 8, • 0 D (1) 1 3) Do 00 21200 R/S.r.OI ď) -0 • 8, B do CEX total propagation delay = tpd N-5 81 80 0 1 PS 3,5 CLK1 00 10 CLK2 01 (LK3 1 10 00 11 CLKA_

descents - (- ⁰⁰¹⁴ Myr 154 Step-15: Draw the logic diagram -Ju=K0=1 $J_{i} = K_{i} = B_{0}$ CLK -> -ve edge truggering. 5500 05, 010 Jo 0,0 12 00 K BI XI CLK Max propagation delay = tpd (prop delay of I-FF). Noc Big Bio P.5 01 00 V CLK1 0 0 1 CLK2 6 1 V UK3 D 00 V LLKA 0 2-bit Synchronous Up Counter wing T-FF: $2^{n} = 4$ ·Step-(1): n=2 Step-(2): 700 K <u>dtep-(3): T-FF</u> exutation table of T-FF Bn+1 T on 0 Ø 0 ۱ 0 1 D 1 C

AL.				Dege 1	57- (
Sara -				S.	
Skp	-(4):	p.s	N•S	Required exis	tation
		00 B1	30 81	ToTI	
	celle i	0 0	0 1	0 = 1 1 2	
	2	0 01	1 0	1 1	
	3	[0]	1 1	0	
-201	4	1 1	0 0		
		<u></u>			
	To	81	T1 = 1		
	O	0		a Martinea	
	•	0 (1)	$T_0 = \Theta_1$		
	1	OVI			
			and have been a		
<u>42</u>	2p-(5) 5	Draw th	e Diagram -		1
3	1	See and the			
		To Bo	0 1-	TI BI	
CL	K-1	\rightarrow		À Ô	
		870		ତି, ୍	
				-	
		PS	N.S	1	
C	LKA	0, 0,	3,0 3,1		
	1	0 0	0 1		
	2	0	1 0		•
	3	1 0		Neger The second	6.5
	4				
			X	hy 1	
		t		1	
	The second	- 1. J		12 - TT	
			20	T = is	
					and the second second

dessente Data Page 158 · 2-bit Synchronous Down Counters -() n=2 (2) 001 0 OD XTO (3) JK-FF 18 excitation table on Omt1 ØJ K 0 0 D X X) A x ۱ X 0 (4)P.S N.S CLK Bo go 031. 03-1 JK J 1 0 X 0 1 2 D 0 Х X ١ 3 1 Х 1 1 X D 1 D ١ 0 4 X 0 1 X Ò 0 (5) Diggidering + Jo Ko 81 80 Bo ь 1 0 1 Ø 0 X X 0 Jo= BI Ko= BI $J_1 = 1$ $K_1 = 1$

classmate 159 (5) Bo 0 30 B JI -00 CLK 80 KI BI KO 10 Verufication = Nos D.C CLK 30 81 0,0 81 1 1 0 0 1 0 2 1 1 1 3 1 0 1 0 0 D 1 4 0 · 3-bit synchronous up counter .. 016 MOD-8 Synchronows UP counter. $m = 3(FF), N = 2^3 = 8$ (state) 0) (2)state diogram >000 UT 00 110 010 10 000 (3) choice FF3& excitation table = (T-FF) Bntl Bn-T 0 0 0 1 01 1 ١ 0 0 1 1

discuste Data Paga 160 (4) Minimay expressions for excitations Required excitation P.s NUS T2 T1 TO 82 8, 80 87 03, 0,0 CLK) J δ 0____ •) Ò Ø D D D D Tes Bi T D D . TI= BO T2 = 8,00 To = 1 (5) Draw Diagram 0, ø T, Q T To ø Ø • x CLK 3 bit upschropous up counter.

classmale Dote he1 Page 161 verification. By B1 B0 CLK_ 82 31 30 1 0 1 D 0 0 0 2 0 1 0 0 1 0 3 Ö 1 0 0 1 1 4 ١ 0 0 1 1 0 5 1 0 0 0 1 6 J D 1 0 7 1 1 1 1 1 0 8 1 1 1 0 0 0 • 3-bit synchronous Down counter = (or) 1. MOD-8 synchronous Down counter 000 (1) m = 3, $N = 2^3 = 8$ 4 100 . . . (3) 11-5 000 ACT ACT (III) 8->7+6+5+4+3+2->! (10) 100 COR B) Choice hippip X exitation table-D-FF gn) Sati D 0 0 D 1 1 D 0 1 D 1 1 1

dissense) Data Paga 162 minimal expressions for excitations Do D 0,2 0,1 0,0 Do CLK 0, 0, 00 1 1 D D D 0 1 2 0 1 1 0 1 3 0 0 0 0 1 0 D 4 0 1 * conservition No. 1 0 5 1 D 0 6 white most -1 7 0 0 8005 0 0 0 8 nind 67 Do 8190 0,00 32 051 82 10 11 Br 01 11 DI 10 TO 0 D D 0 6 .0 0 0 0 0 0 0 10 00 0 6 10 $D_1 = \sigma_1 \overline{\sigma_1} \overline{\sigma_2} \overline{\sigma_3} \overline{\sigma_2} \overline{\sigma_3} \overline{\sigma_3} \overline{\sigma_2} \overline{\sigma_3} \overline{\sigma_$ $D_2 = \mathcal{O}_2 \mathcal{O}_1 \mathcal{O}_0 + \mathcal{O}_2 \mathcal{O}_0 + \mathcal{O}_3 \mathcal{O}_1$ 3 Draw the Diag Logic Diagram D, 8,2 ,0, Bo D Do D ø Ð B2 00 8, 20 t 0 D CLK Do D. B. D. Dzoz Do Bo Ð D 0 80 BI 03: ak

classmate Page 163 venification -CLK 8, 8, 00 B, 0, 00 1 0 D . 1 1 0 1 2 1 01 D 2 10 L D 1 1 1 0 2000 4 01 1 0 D : 301 5 00) 0 ;;; 6 1 D 0 7 1 D 8 0 0 01 · 3-bit Synchronous Down Counter using JK-FF: 24 $0 \rightarrow 7 \rightarrow 6 \rightarrow 5 \rightarrow 4 \rightarrow 3 \rightarrow 2 \rightarrow 1$ (1) n = 3 $N = 2^3 = 8$ (MOD - 8 cynchronous down counter. (1) State diagram -(11)× 000× 601 1LO 101 (010) OIL 1002 (11) JK-FF & excitation table. Ontj J K om X 0 0 0 Х) 1 0 x 1 · . 0 Х 0

desense 161 JK K K 1 (iv) J 829,00 82 81 80 CLK × x ۱ 1 Ó Ó D 0 01 X 0 Х 2) 0 10 × 1 × 0 х 3 01 D X 0 61 0 X 0 D 4 X i Χ. 01 × 5 0 0 Х 01 X X 6 0 0) X 10 х 7 X × X 0 8 0 $J_0 = K_0 = 1$ (DR KI 82 8,00 길의 10 11 01 00 10 00 01 1 0 X X X D X 0 0 1 14 X 1 X 0 X 0 KI= So J= Oro oz K2 11 10 01 11 10 00 J2 30 00 01 x r x Ò 0 0 D 0 X 0 0 X X $J_2 = \overline{\vartheta_1} \overline{\vartheta_0}$ JK2 = 8,80 (V) Logic Diagtam 7,0,1 1 Bo J2 B Ter. Jo 0, K. BI K, B KOB CLK → we use JK-FF and T-FF toft simple circuit (WORK) Scanned by CamScanner

classmate Pepe 165 · Mo Design of a MODULUS-10 synchronous up counterc= m=4, $N=2^{4}=16$ (1) $N \leq 2^{M}$ $10 \leq 2^{4}$ (η) D (000) (000) x (0010) x (001) >01000 DIOD 1001× 1000× (011)× Decade counter (on) BCD Counter T-FF & excitation table = (11) :-Sn Bntl ST ļ D Nos 2-5 To (11) T, Tz T2_ Bg B2 B1 80 Orz On By Bro CLK O 0 0 1 b 0 0 1 ò . 0 1 D D 0 1 0 1 1 0 1 D Ô 0 1 1 1 1 1 n D 2 0 0 1 0 0 0 h O D I 0 0 0

	classenete
	Page IGG
	(Frage
	X
Total 8.00	$T_0 = 1$
15 ELSI B3B2 00 01 10 10 TI -	
$T_{1} = 00001100000000000000000000000000000$	
01 0 11 1) 8	
11 0 0 XX	$T_1 = \overline{\vartheta}_3 \vartheta_0 0 .$
$T_2 = 8, 8, 9, 80 00 01 10 10$	1
00 0 0 0 0 0	
010010	
	$T_2 = B_1 B_0$
10 0 0 X X	12 - 0/0/0
	No. Second
$T_3 = 3302 0100 01 11 10$	
	-4
	$T_3 = \vartheta_2 \vartheta_1 \vartheta_0 + \vartheta_3 \vartheta_0$
10 0 U X X	
Δ() ο	
(V) logic diagram	here and a
1	
<u>B</u> To Bol T, B,	D7 72 824 - T3 834
- Bo - Bol	ār ās
CLK	and the second sec
	A Starting and a start of the s
and the second sec	

dissoute Date Page 167 · Design of a synchromous MOD-6 Down Counter-(1) $M \leq 2^{n}$ 6523 n=3 $\langle \mathcal{S} \rangle$ 0->-->6->5-> Dioo DDI 20 0 D 3 5 4 DD. 1015 (3) JK-FF & its excitation table Bnti Bm-J K X D 0 0 1 D 1 x 1 D x 11-:-) χ 0 P.C N.C (4)CLW Ka J_Ko 81 80 J,K, J, B, B 0,2 X el X) 1 X 01 1 I 0 T 0 0 O.X.) 01 0 0 Х X 2 0) 1) 3 X 1 D XXI 01 D X 01 1) 9) Ø DX X OX XO Ď 0 A1 104 D 5 X OX IA SIX. 1 01 1 D n OX XI X 1 X 6 0 0.0 0 100 1 0 Jo= Ko = 1 9100 O21 82 8180 61 11 10 01 11 10 KIS 01 15 X X X D 0 X 0 X 3 X1= 0000 02+ 0,0 JI= 0000, 80 K2 = 00 00 200 10 U1 01 11 10 11 Jz X NX COSE Ø D Ø X Ø XX X Jr= Olto 01 / 50 K2= 0 01 00 Scanned by CamScanner

JASSMACE. 168 (5) J2 83 30] 8 1 KO K. SZ 000 K, B, CLK MOD-6 synchronous Down counter -> MOD-6 up count synchronous Up counter is self stanting. • Derign a counter that goes through states 0, 3, 5, 6,00 (\mathbf{i}) no. of FFS m=3. (1)) 1,2,4,2 600 OID 3 6610 1. in (00) 5. (11) choice of FF & excitation flipplop-T-FF gres gritt T 10 D 0 0 ١ 1 D 1 0 0 1pm 10 required excitation P.L NIS To CLK T2 TI 82 01 00 82 81 80 ١ 0 ۱ 1 0 1 0 D D 1 1 2 0 1 0 ١ 3 1 1 1 D 0 1 D 1 1 2 (1) 4 1 0 0 0 0 1 0 0 Giri

classmate Page 169 in (1V) minimus expression T2=01 191000 BZ 00 01 11 10 1 X X Ô 0 X X 1 D To=81. $T_1 = 1$ 03,000 0100 10 32 32 01 00 11 11 10 DO 01 X D X X X 1 0 1 X X X 1 1 (v)T, S, T : . -4040 To Bo 31 1-40 0 20 Q2 00 a (WORK) CLK 81-12 るって N.5 P.C 71 B, B, B, Do B, B, Bo CLK (1,2097) 1 00) 1 0 I 1 0 (1)0 0 2 0(4) 0 1 0 0 3 1(7) 1 1 1 1 0 D 0 0 1 () 1 0 4 1) 0 1 $|\rightarrow 2 \rightarrow 4 \rightarrow 7$ -> Lock out problem 1 to solve this problem = CIR = 3100 00 CLR 82 8, 30 11 610 1 01 10 ٥ 1 $\widehat{}$ Ò 1 Ø (2) 0 D 0 I 1 (1 (9) D 0 1 0 0 L (7) 1 1 1 $\Sigma(1,2,4,7) = \otimes_2 \oplus 9_1 \oplus \otimes_0$

classmeth D hate 170 T2 T32 To 90 TI 81 Br 820 34 CLK LLR ar CLR . B2 BB1 82 D 81 D 80 On E 071 020 When (1,2,4,7) any of them will come Counter willbe CLR. (000) 42 De electroto 1 8-..... 2.92 U not = (to b.

classmate Date Page 171 GRATE QUESTION ON JEQUENTIAL CIRCUIT: (n-1987) NXXX 6 121 P (0) -2V V1>V2->V0 +2V V2)V, -> Vo=+ UV =1,0,0 -1V X(1) for $V_i^o = -2V$, P=0 ($x=0^{-1}$, $y=1^{-1}$) VED FOR V° = +3V, P=0 (X=1, Y=0) $\chi_{o}(M)$ For $\chi_{i} = 0V$, P = 0 always $(\chi = 0, \gamma = 0^{2})$ (IN FOR VP = OV > P can be either 'd'on 1 cr-1987 03 ... 122 82 P1 81 Do Bo BI B2 CLK 30 PR R (CLR) R Feed back 10910 A Ripple counter wing -ve triggered D-FF is shown. The FFs are cleared to o' at R i/p. The Feedback logic is to be designed to obtain the Count sequence shown below. () MOP-6 # Asymetriconous Counter (6) 82 9190 110 81-8, 8180 -> Feed barn logic is = 020,00.

recuste 172 h=1988 The citruit shown below is a 1º2 -> SR (latch) & XOJK-FF XD Jonson's counter X@ RS-FF @ None of the above Fit is not FF secame it have not any clock Tifit is not FF, then it can't be counter n=199 8,4 4-bit modulo -16 rupple counter uses on J K-FF If the propagation delay of each FF is 50 ms. The "max clock frequency that can be used is equal to: @ 20 MHz @ 5 MHz Tent in the 10 MHz d 4 MHz > I top of one FF is = 50 ms f=+++ $=\frac{10^9}{200}=\frac{10^7}{2}$ = 5×10 G=1991 (85) = 5 MA An S.R-FF can be connected in a EFT-FF by connerting to REQ & Sto B SIRAT \$ 100 0 × 0 1=B.T REBIT

atlantis Date Page 17-3 UZ 1992 So A pulse train with a fireq of IMHz is counted modulo-1029 pipple counter built JK-FF. For proper openation of the counter. The max permissible prop delay per FF stage is too nue max tpd = Re-checer freq=1 Mitz Celeger TOLK = nx-bd tpa= Terk = 1 106 = 106 see 10-6 = MOD-1024 hipple 177 Sec N = 2027= 210 = 100 × 10 200 n=10 :-= 100 neu (B) In a JK-FF We have J= B, K=1. Assuming the FF was initially cleaned & then Clocked for 6 pieles reagnence at the of ofp will be • 0, 1, 0. 7 B a K 1,0,1 CLK CIK 8 1 1 3 0 1 3 9 0 ١ 5 6 0

atlantis Date Page F12 UE1228 = Eig OR Mod - K counter, Here K= 9 shows Jo Bo 31 31 0 60,0, 8 Ko 30 KIA 1. б 0.57 CLK e. 4 3 a Ø B 6) 2 91 00 カニン 2K P-5 N.S KI 3 CLK Go 97 000 631 NS2M. 1 1 1 1 0 A D N 522 -9 ١ 10 ٦ 1 0 ١ 1 0 1 1 3 NS4 0 0 D 0 4 G= 19 8 . 1 =0 . A=3/p B' is the now replaced by B=1 101010 . lequence x & y will be The 0/9 5.6 \rightarrow B × A 10 ١ 1 X = 01 0 1 0 1 Y = 1 0 l 1) . . ١ 0 1 0 T 1 0 1 0 1 0

atlantis State Page 175 9-2017 For the circuit shown, the counter wate (9,00) (9,10) follows the sequence -D1 91 Do Bo Bo BI (a) 00,01,10,11,00 (by 00,01, 10,00, 00,01,11,00,01. (1)8,+80 (d)00, 10, 11, 00, 10, P.S CLK 3, Bo 8, 8,0 NIS Do D CLK 80 1 J 1 0 0 D D D 0 2 1 1 1 0 3 0 0 0 1 0 0 ō 1 1 D 0 9 6 D 1 D 1 0 5 (B) For each of the the edge trigger & JK-FF used 2008 in the following fig. the propagation delay -31 JI 1 -30 CLK Ko KI CLK T Draw the op wave from form at Q1 4

atlantis Date_ Page 176 (T--> CLK 030 31 E AT B t+2AT 2008 8312 for the circuit shown in the Rig, D has a transi= tion from a to 21 after CLK changes from 1 to 0 Assume gote delays are ge negligible. To CLK 1,0 OPD 0,1 2 1,0 B 1,0 which of the following stalement is treve Q os goes to I at the clock transition & stay's at 1 & goes to 0 2, 72 " OB goes to ! 17 " & goes to of o goes to O 17 17 K 12 51 リ Dquistol ab Cv-2111 0,3 when the 0/p yin the circuit below is i , it implies Data has Data D 8 10 D 3 0 10 @ changed from a bol (a) not changed D changed » 1 to 0 \bigcirc my eithen direction Changed Scanned by CamScanner

31 37115 1=7 SN Call TWO D-FFG Lol as in -- 10ampter that area through the fillowing 5, 10- - 10-Elluni 00to the ips by & De ane (a) $D_A = B_B$ = 8A 3 Do (b) DA = 3 A Da = Ba $O DA = (a_A \oplus B_B)$ Dg = BA (DA = (BA 0 85) > DB= 50 No-6 2-5 -. a_s SB 9A OL 2 DA 111 0 0 M 1 ş T, 2 1 0 3 (for Ð (1) 4 ñ 1 \cap 13.040 5 54 Do Da (Th) 6 0 X Ď P3=50 DB = SA 6 Br M 0 ٥ 1+0-1.1 -DA = SA OF P= 89 SA + 84 88 = 0 $p_{4} = \overline{a}_{4} \oplus \overline{a}_{8}$

atlantis Dele Pope 178 9-2015 815 A MODIN counter using a cynchronous binany Up-counter with synchronous dear i/p is shown in the fig. The value of n is -4-bit binany BA BR Counter BL OBD CLK CLR = 0 SB 8A Br SD ->6 0) 1 0 -1-2-3-9-5-6 MOD-7 Counter 2015 (316) A 3-bit pseduo random number generater is shown. Initially the value of i/p y = Y2 Y1 Yo is set to 111. after 3 clock cyclesis Y Y, 1 701 Dz DI 81 Do 30 32 CLK p.c BIDS0 By CLK 8081 80 9, 30 Q2 1 1 6) ¥ D 1 2 1 0 1 1 0 h ١ D 3 0 0 0 1 0 (1 0 0 1 y=

Fortune Page No : $\int G_{1}H_{1} = 10^{9}$ 10 200 = 1 mar Date : 1-4-0 For a circuit summ in the fig, The dealy of the bubbled NAND gate is 2ns & that of the counter (SIA) is assumed to be Zerro. B. (LSB) 3 bit 81 Synchronous B2(MIB) Counter CLK RST=0 If the clock freq is I atz, then the counterc behaves_as_a (01) Mod - 5 Country (b) 1) ") (0) - 7 >) 17 (d) » - 8 » fork= 1 Gitty = 10° see $T_{CLK} = \frac{1}{10^{9} cee} = 10^{9} see = 1 ms$ N524523 82 81 20 N=8 -> 6+2->8 Discourte acegos Mod-8

Fortune Page No : Date: 180 REGUISTERS : 0 > a Flip- Flop Can store 12-bit of binary information. -> A tregistere is a group of flip-flops which can store a group of binany information. -> n-bit register, concits of n, no. of FFS, it can Store h-bit of binary information. -> 4-bit register, 8 bit register. A, B, ··· E, E · <u>4-bit registers</u>: -> generaly D-FF are use in register. 3 0, B 1 0 ā ak CLK J=D=K=D $S = D, R = \overline{D}$ $I_2 = 0$ I0 = 0 J2=1 $I_{1} = 1$ B OB 0, R MJB LSB CLK CLR CP B 0 0 tMSB2 (LSB)

Fortune Page No : Date: 187 openation = (1) (LR = 0, R = 0)BA OB BC BD 0 0 0 0 (2)I3 =1 $I_{7} = 1$ J1=0 Jo=0 ... $D_3 = 1, D_2 = 1, D_1 = 0, D_6 = 0$ when we apply a clk BA BB BC BD CLK-1->1 1 0 0 • symbol -I3 I2 I1 I0 DDDD BBBBB CLK Loud BA BB BC BD Load = 0 -> The O/p of register will remain same Load = 11 -> The Data Which is available at the i/p of the D-FF will be transferrent -> This Load can be - Synchronous → (Load A, CLKA) Asynchronous -> Load T (It will not depend on the CLK)

- Fortune Page No : Date : 182 Load = 0 -> same O/P. Load =1 -> Load new information. 10 -0 0/P MUX O/p= Io Load + I, Load. Load - %P Loud-ĐO · Register with patrollel Load 1000 -Jo B **F**3 .I. 0 D D 03 D 0 D B AR CLK CLR > 2, 4, 6, 8 AND gates (Enables) 20ad=0 will be so on 1, 3, 5, 7 -> OFF pissable Load =1 -> 1, 3, 5,7 -> (trable) 2, 4, 6, 8 -> (Disable) Malan undenstanding) headar

Fortun Page No : Date: 183 · Applications of Registers = = will be used as a generical put pore registers in tep. michophocescores. 8085, 8036 A,B,C, ··· E,F,GL 8-bit hegisten Semiconduita temporrary registers. (temopony stonage memory) RABO (Territ Storre) og OIT ROM EX: ADD A (permanent storage memory) (phogstam store) -> shift Register = > SISD SIPO PIPO P150 Chift registers : Types of shift registers = t -> Seriar - in serial out (SISO) shift rugisker. -> serieu-in parallel-out (SIPO) shift register. -> Parallel-in serial out (SIPO) shift register. -> Parallel-in parallel out (PIPO) shift register. (1) SISO chift negister = (a) (b) Sercial data of Seria serial Serias data i/p data data chift-Right SISO º/P shift - bft SISO. Scanned by CamScanner

Fortune Page No : 184 Date : (2) SIPO shift register = +++ + Enclade charlese of p. Servial data parallel data 0/p (3) pI so chift rugister = Parralle) data 1/p + union data ofp. (4) PIPO shift Register parallel data i/p 1 1 parallel data 0/p (5) Bidiruhonal chift register = IISO, shift-left, shift-right. > out In (6) Rotate night shift requiser = (7) rotate-left shift nog= 4-4-51 +++

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Fortune Page No : Date: 185 satta SISO (cerian in cerian out) will register = (a) shift-Right: Data In Do Og D2 820 D3 03 0 FF4 FF3 FFI CLK state 83 32 3, 30 MSB -> 10 -> LSB Operation S In \$0 3, a, CLK DataIn 02 In hally 0 0 JN 0 8 >11 Storred deter. out 8 Patrin 00 82 32 31 seniat out put. UK LIB D IniHally 2 5 1 0 60K 0 6 0 7 MIR -> totas 7' cik puties required to store the dort senially so taken out senially. -> NIF n-bit Wilt reg SISO (2n-1) -> clock pulses required. percissional transpil

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Fortune Page No : Date: 186 (b) shift bett " In P3 83 0 Do 300 12020 D1 81 (1SB) CLK (MSB) Store 1010 Mis YLSB Operation = 83 02 B1 CLK On Initially OK DE 1 1 0 0 `1 0 4 OF stoned data net put CLK 03 0300, 00 In VO in Pally. 0 0 0 0 0 1 0 D DEDE 2 1 NOK OK OK O D 0 -> Total -7 CLK plus required to complete the spenation 7 CIK Pulses -1010 1010 Tur= 1 lise Flerer -1010 1015 -> SILO -> Time delay application (und pigitas Signer proceeding)

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Fortune Page No : Date: 187 101 Panallel · 1-Bit sipo (Cirular in Serias sut) shill registers = 90=0 ST =0 83=0 92=0 Data D, BR D080 D2 82 Jn P3 83 \$FF7 FFO CY FF2 FF3 1SB MCB CLK. Storce 1011 ->LCB openation 8, 91 30 CLK Data-In Q2 Initially D SO 40 1 1 40 63 1 9 stone. -> After 4 UK pulses the data is grailable. Application of SIPO chilt-Registers -= Data-In SRG2 4 1011 CLK parallet-out N partallel convertion of data - unial 10 Hid Menel

Fortune Page No : Date: 188 · PIPO (panalles in parallel out) shift - Pegister -IO Ip=0 J2 -I3 Do Bo D, 81 P2 Q2 83 Dz FFO FFI FF2 FFZ (LSB) (MiB) CLK 30 =0 81=0 82=1 B3 =1 also called ligsten/ storage rugiten/ Button register. 80 81 I2 J1 In on UK 0 0 Initially 0 0 D D D 1 0 L 1 (chifting is not happening in this reg) · PISO (paralles-in-seried - out) shift - negisters parallel-In Data CLK servial-out Data Shift/1000 shift/Load = 0 -> parallel data will be loaded into the Register. The Data will be shifted towards shift/ Load Right side . Lood 2×1 o/p= 5. Load + S. shift MUX (S) Shift Load/shift 0

Fortune Page No : Date: 189 581 1000 ----5-10-0/P . shift • A-bit piso shift register - (store 1100) Shift/Load : " -Do T_= 0 11=0 172=1 13=1 D, 8, Do 80 D3 03 Dy By (238) (MSB) CLK MIB 1100 LSB Operation = servial output parallel-data B2 B2 B, BO shift/load CLK I3 I2 II JO 00 0 0 initially 6) -0 1 1 00 OD 介(1) 0 IL 6 710 J 0 0 1 (2) 1 14 VOI ۱ 0 A(3) 1 1 0 IN RIGIE 0 1 1 0 1 T(9) Jotas 4- clock pt pulses required to complete the openation. (loading & shifting) When, shift/soad = 0, (2, 4, 6) AND gate are enable. (1, 3, 5) 1, 3 are disable. shift/load=1 =, (1,3,5) AND gate are remable. (2,4,6) AND gate are disable.

Page No : Date : 190 · Application = -> parallel - to-seriar Conversion. - used in michophocessons (3085, 3086). · Bidirectional shift Register = LCLK > out In 1> >-- In out < 1 A Right/Left (R/E) Arhere high i/p Active low 1/p $\rightarrow R/L = 0 \rightarrow Left - shift$ $\rightarrow R/I = 1 \rightarrow Right - shift$ Left 6/P= J.L+S.R 281 MUX (5) Right shift RILA Left shift - 0/p=(J.L+S.R) STDO Right shift

Fartune Page No : 0 Logic dragroom of 9-bit bidiruhonal shift Date : 191 MSE 1001 LSE Din-(0,1) R/I E. F 5 H Do 30 DIBI 0,3 D2 82 D3 Right left-shift cuilt . 0/p DIP CLK openation - 1101 R/I 0/p Bo Ba B2 B, Din CLK Inibally 0 0 D K 1 10) NO Ċ. 10 1 -> NO DE K 1(3) 1 0 -> DE ... 500 + (4) NO 1 NI 1-9 ١ NO 14 1 -Boz 80, 82 Real BA 1(5) 1. D 0 90 20% 46) 0 5 4 (8) 0 ン DK -0 >D B3 B2 B1 B0 21 1 >1 0 . 1 1 0 1 1.1 N. 611-485

- Fortune Page No : Date : 192 • Universal Shift registers = A Register capable of shifting in one direction only is a unidirectional shift register. > A Register that can shift in both directions is a de bidirectionay shift register. If the register has both chifts and parrallel load capabilities, it is referred to as a universal shift registero · Block diagram of 4-bit Universal shift register -3 control 1/p S. Parcallel 1/p ; : Servial In -> servial -out 4-bit universal for shif-Right Shift Registers < serviced In fore servial out Shift Left. panallel oppi · function table -50 Register Operation No change 0 0 shift waysbullt 1 shift boll Right 0 Panallel Load. No change Ic -R JI T2 1X4 T3 MUX 51 50

Fortune Page No : Date: 193 • <u> <u> </u>-Bit Universal shift Registers -</u> Panallel D/P 050 31 1033 32 0,2 03 Bo 81 Dy R la DI (JB) CLK (MJB) YAXI MUX 4x1 MUX1 ST 4×1 MUX 4×1 MUX So Not. seria In shift-)eft serias In Shift-Right T I? I3 ... panallel 1/p. Shift Register Counterra = 0 -> Ring counter. -> Johnson counter (twisted ring counter) · Ring Counter = Ph = 1 130=0 1 Pro=1 Do Boli D2 0,20 DABIO Bo 82 0, 9CLR=1 ICLR=0 CLR=0 LLK Pr=0, B=1 3-bit king Counter CLR=0, B=0)

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-. Fortune Page No : Date : 194 operation 030 On UK 31 CLK 8, 8-Qo 0 niballe } 0 Initially 20 1() 3 个()) 0 2 1 个(2) A (3) 0. D \$ r (3) 0 1(3) 0 It counts 3 clock pulses It counts 3 CEK pulse ** Ring Ring Counter count n- clock pulse Counter using JK-FF iling 5 5, 30 90 52 3 0 Ba ā 0 B2 KZ KO CLI openation 20 au 03 Initialle 0 Y 2(1) × 1 1 (2) 132 50 K 19 17 counts 3 CLK pulses Application -> psuede (we in) generatori Random requence

Fortune Page No : 4 24 Date : 195 Johnson's Ring Counter (Twisted Ring counter) = 102 31 30 Do Sot 81 DI Dz By FFB BI FFA By FFL QD Q CLR CLK operation = Bo 80 81 By CLK D 0 Inifally 0 NO 40 (1) 1 GK 1 (2) 11 317 (3)J1 . 1 0 0 (4)NI1 0 (5) 0 SD (6) 0 >A 3-bit Twisted Ring counter can count 6- cik pluus ** An n-bit Twisted ping counter can count 2n-cp. 1-frequency division > n-bit Pipple (ounter = \$/27 Rign counter = fm -> n Tronson's counter = 1/27 \rightarrow "

Fortan Page No : Date : #6 196 • Twisted Ring Counter uning JK-FF = S1 843 8 30 30 30 8 1]3 Q, 3, 8, K.8 KI BI a K CLK э -> It can count - 2n clock pulses. · 3-bit 1150 Shift register wing JK-FF Servial - In R .. D · · 7,8, 3,0 3.8 Was KO K.B CLK J = DKED