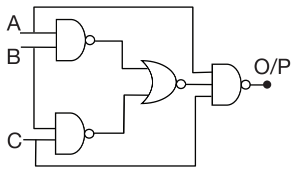
Digital Circuits Test I

Number of Questions: 35 **Time: 90 min.**

Directions for questions 1 to 35: Select the correct alternative from the given choices.

1. The output of the following circuit is



(A) $\overline{AB}+\overline{BC}$ (B) $\overline{AB}+\overline{BC}+\overline{AC}$
(C) $\overline{A}+\overline{B}+\overline{C}$ (D) $\overline{AB+BC}$

2. Match the following
List I (Numbers in Decimal)
List II (equivalents in signed 2's complement representation)

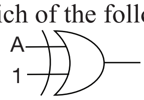
	List-I		List-II
P.	– 43	1.	01100000
Q.	– 78	2.	00110110
R.	+ 54	3.	111010101
S.	+ 96	4.	10110010

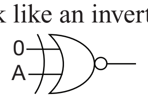
(A) $P-3, Q-4, R-1, S-2$
(B) $P-4, Q-3, R-1, S-2$
(C) $P-3, Q-4, R-2, S-1$
(D) $P-4, Q-3, R-1, S-2$

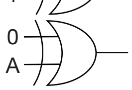
3. Which of the following functions will satisfy the property
Dual of function = complement of the function?
(A) $f(A, B, C) = \Sigma m\ (0, 1, 2, 3)$
(B) $f(A, B, C) = \Sigma m\ (4, 5, 6, 7)$
(C) $f(A, B, C) = \Sigma m\ (0, 2, 4, 6)$
(D) $f(A, B, C) = \Sigma m\ (0, 1, 6, 7)$

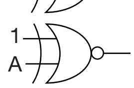
4. The number of min terms for the function
$F(a, b, c, d, e) = b + cd$ is
(A) 24 (B) 20
(C) 32 (D) 16

5. Which of the following will work like an inverter?

(*P*) 

(*Q*) 

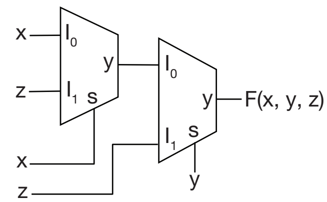
(*R*) 

(*S*) 

(A) *P,Q* (B) *Q,R*
(C) *R,S* (D) *P,S*

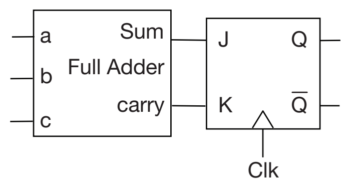
6. How many number of 2 input NAND gates are required to impalement $f(A, B, C) = \Sigma m\ (1, 3, 4, 5, 6, 7, 9, 11, 12, 13\ 14, 15)$?
(A) 4 (B) 3
(C) 2 (D) 1

7. The output of the following Multiplexer circuit is



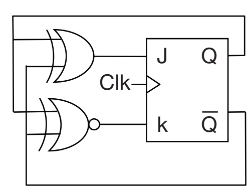
(A) $x^1 + yz$ (B) $x^1 y + z$
(C) $(x^1 + y)z$ (D) $x^1 y^1 + yz + xy^1 z$

8. Initially $Q_n = 0$, $\overline{Q_n} = 1$, after clk pulse $Q_n + 1 = 1$, $\overline{Q}_{n+1} = 0$. Then the input *a,b,c*



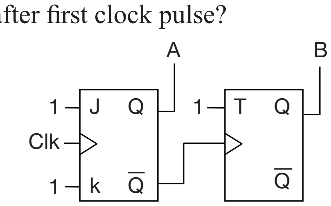
(A) two or more inputs should be 1
(B) only one input has to be 1, or all inputs should be 1
(C) *c* should be zero, *a*, *b*, can be 11 or 00
(D) All inputs should be zero

9. The states of Q, $\overline{Q}$ after clock pulse are



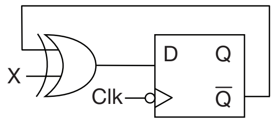
(A) 0, 1
(B) 1, 0
(C) 1, 1
(D) cannot be determined without initial states

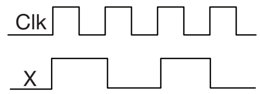
10. The initial state of counter is $AB = 01$, what is the output (AB), after first clock pulse?

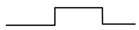
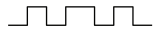


(A) 10 (B) 11
(C) 01 (D) 00

11. The initial value of $Q = 0$, then the output Q waveform for the applied clk, x inputs is





(A) 
(B) 
(C) 
(D) 

12. An 8 bit Digital to Analog converter has an output current of 5.8 mA, for the input 10010001, then the output current for input 11110100 is (in mA)

(A) 9.25
(B) 9.76
(C) 8.43
(D) 8.23

13. At the end of this program, the contents of Accumulator are?

MVI A, 64 *H*
MOV B, A
STC
CMC
RAL
X RA B

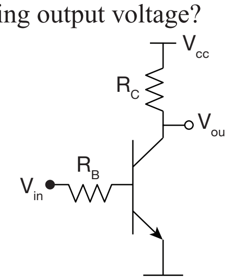
(A) *C8H*
(B) 2*CH*
(C) 00*H*
(D) *ACH*

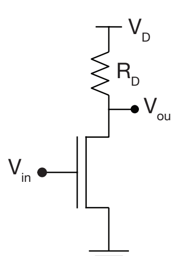
14. What is the operation performed in the following program.

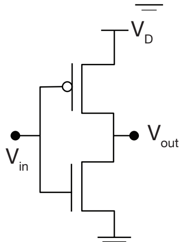
LXI H, 4123 *H*
MOV A, M
CMA
MOV M,A
XRA A

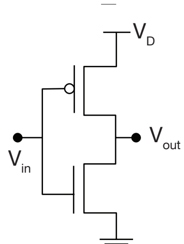
(A) Contents of Register *M* are moved to Accumulator
(B) $H = 23H$, $L = 41H$, $A =$ Un known
(C) contents of Memory location 4123 *H* are complemented. and stored in the same location
(D) contents of Memory location 4123*H* are XORed with Accumulator and retained in Accumulator

15. Which of the following inverter circuits will have full swing output voltage?

(P) 

(Q) 

(R) 

(S) 

(A) only Q
(B) only R
(C) Q and R
(D) P and Q

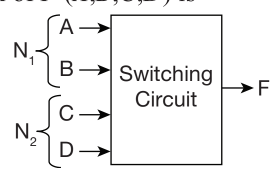
16. Perform the following operation in 2's complement signed representation, and the result in 2's complement signed notation is $(-13)_{10} + (-28)_{10} =?$

(A) 10101001
(B) 11010111
(C) 11010110
(D) 00101001

17. Convert the following number to base 9.
$(1101222.201121)_3$

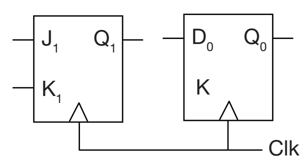
(A) 1358.647
(B) 4172.647
(C) 4178.153
(D) 1358.153

18. A switching circuit has four inputs as shown, A and B represent the first and second bits of a binary number $N1$, C and D represent the first and second bits of a binary number N_2, The output is 1 only, if the product $N_1 \, x \, N_2$ is less than or equal to 2.
The *POS* form of $F(A,B,C,D)$ is



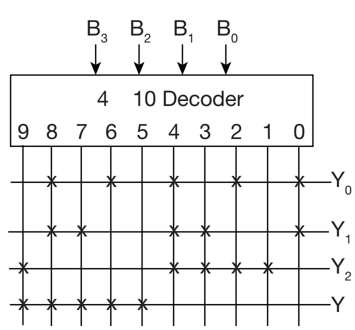
(A) $\overline{A}\,\overline{B}+\overline{C}\,\overline{D}+\overline{A}\,\overline{C}+\overline{A}\,\overline{D}+\overline{B}\,\overline{C}$
(B) $(A + C)(A + B + D)(B + C + D)$
(C) $\left(\overline{A}+\overline{D}\right)\left(\overline{A}+\overline{B}+\overline{D}\right)\left(\overline{B}+C+\overline{D}\right)$
(D) $\left(\overline{A}+\overline{C}\right)\left(\overline{A}+\overline{B}+\overline{D}\right)\left(\overline{B}+\overline{C}+\overline{D}\right)$

19. The synchronous counter which follows (Q_1Q_0) $00 \rightarrow 10 \rightarrow 11 \rightarrow 01 \rightarrow 00$ by using *JK* flip flop and *D* flip flop, has inputs as



(A) $J_1 = \overline{Q}_1, K_1 = Q_O, D_O = Q_O$
(B) $J_1 = Q_1, K_1 = \overline{Q}_1, D_O = Q_O$
(C) $J_1 = \overline{Q}_0, K_1 = Q_O, D_O = Q_1$
(D) $J_1 = Q_0, K_1 = \overline{Q}_O, D_O = Q_1$

20.



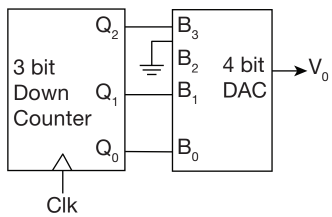
In the above PLD x means connection is present, else no connection present 4 input, 10 output Decoder is used

If the inputs $B_3\ B_2\ B_1\ B_0$ are in BCD system, then $Y_3\ Y_2\ Y_1\ Y_0$ output are in

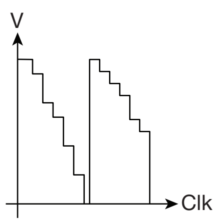
(A) EXS –3 (B) 84 – 2 – 1
(C) Gray code (D) 2421 code

21. Consider the digital circuit, in which a 3 bit down counter is connected to a 4 bit Digital to Analog converter, then the output of DAC Versus the clk pulse graph will look like.

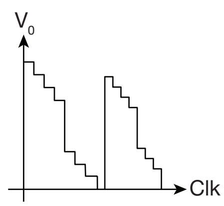
Assume counter starts from all preset state ground shown is logic 0).



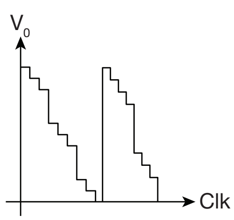
(A)



(B)



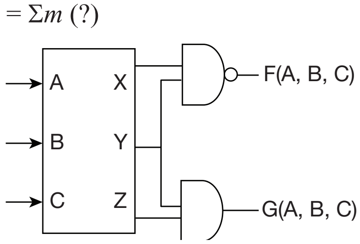
(C)



(D) None of these

22. A combinational circuit has 3 inputs A,B,C, and 3 outputs x,y,z. and the functions F (A, B, C)and G (A, B, C)are generated from the combinational logic circuit as shown here with NAND, AND gates. Find the least possible minterm expression for Y (A,B,C).

F (A, B, C) = Σm (1, 3, 4, 5, 7)
G (A, B, C) = Σm (4, 6)
Y(A, B, C) = Σm (?)



(A) Σm (0, 2, 3, 6, 7) (B) Σm (1, 3, 4, 5, 7)
(C) Σm (0, 2, 4, 6,) (D) Σm (0, 2, 4)

23. From the above data, for which input A,B,C
The outputs all X, Y, Z will become 1, 1, 1 (i.e. XYZ = 1)

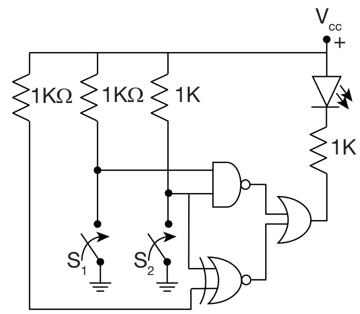
(A) 010 (B) 101
(C) 100 (D) 110

24. The minimum SOP form of

$$f(P,Q,R) = (\overline{P} + R + \overline{Q})(\overline{P} + \overline{R} + Q)(\overline{P} + R + Q)$$

(A) $\overline{P} + QR$ (B) $\overline{P} + Q$
(C) $\overline{PQ} + R$ (D) P

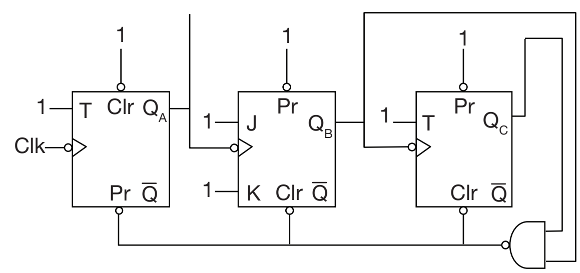
25.



In the above switching circuit (logic 1 = V_{cc}, logic 0 = ground), The LED glows when

(A) both switches $S1$, & $S2$ are closed
(B) only one switch of $S1$ & $S2$ is closed
(C) both switches $S1$ & $S2$ are open
(D) Never glows irrespective of switch positions

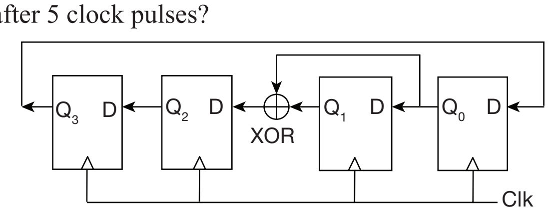
26.



A counter formed with T, JK flip flops, as shown above, preset (Pr), clear (clr) are active low, asynchronous inputs, T,J,K are synchronous inputs The modulus of the counter is

(A) 4 (B) 5
(C) 6 (D) 7

27. A 4 bit shift register is connected as shown with initial states $Q_3\ Q_2\ Q_1\ Q_0$ = 0100 What is state $Q_3\ Q_2\ Q_1\ Q_0$ after 5 clock pulses?



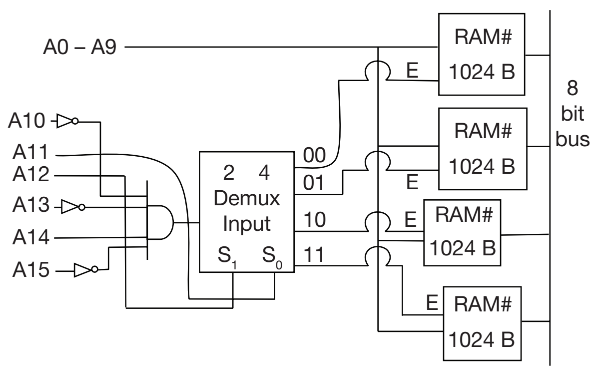
(A) 0111 (B) 1100
(C) 1111 (D) 1001

28. Consider the following program
MVI A, Byte1

ORA A
JP SUB1
XRA A
SUB1 OUT Port Addr
HLT
Byte1 is a 2's complemented signed number, then at output port Address (Port Addr) The number will be
(A) Even Number (B) Positive Number
(C) Odd Number (D) Negative Number

29. 6000 : LXI H, 4C83H
6003: MOV A, L
6004: ADD H
6005: DAA
6006: MOV H, A
6007: PCHL
At the end of this program, from which address next instruction will be fetched?
(A) 9038*H* (B) 8438*H*
(C) 8A38*H* (D) 6008*H*

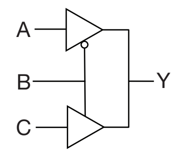
30. There are four chips each of 1024 bytes connected to a 8085 Microprocessor. As shown in the figure below, RAM_s 1, 2, 3, and 4 respectively are mapped to addresses.



(A) 0800H-OBGGH, 180H-IBGGH, 2800H-2BGGH,3800H – 3BFFH
(B) 0500H-O8FFH, 1500H- 18FFH, 3500H-38FFH,5500H – 58FFH
(C) 1800H-IFFFH, 2800 – 2FFFH, 2800H-3FFFH,5500H – 58FFH
(D) 5800H – 5BFFH, 5000H – 53FFH, 4800H – 4BFFH, 4800H – 4FFFH

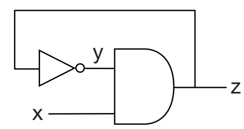
31. MVI B, 46H
MVI A, 39H
ADD B
STC
RAL
XRI F0H
The contents of Accumulator at the end of this program
(A) 00*H* (B) 01*H*
(C) *F*0*H* (D) 0*FH*

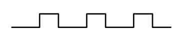
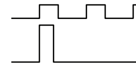
32. The following circuit using three – state buffer works like



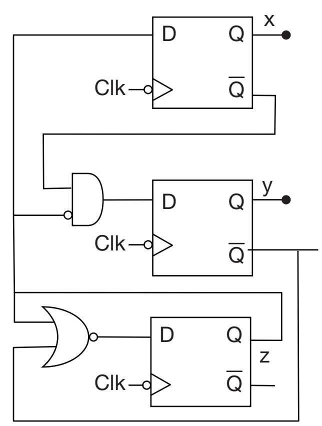
(A) Data Decoder
(B) Binary Encoder
(C) Data selector
(D) Data Distributor

33. Assume initially $x = 0$, $y = 1$, and x becomes 1 for 40*ns*, and then x is 0 again. The inverter in the given circuit has a propagation delay of 5*ns*, and AND gate has a propagation delay of 10*ns*.
Then the wave form for z is



(A)  (B) 
(C)  (D) 

Common Data for Questions 34 and 35:
Consider the following circuit involving three D – type flip-flops used in a certain type of counter configuration



34. If at some instance prior to the occurrence of the clock edge x,y ad z have a value 0, 1, and 1, what shall be the value of xyz after the clock edge?
(A) 000 (B) 100
(C) 010 (D) 101

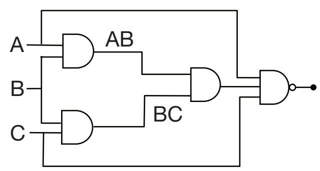
35. If all the flip flops were reset to 0 at power on what is the total number of distinct outputs (states) represented by xyz generated by the counter?
(A) 4 (B) 5
(C) 6 (D) 7

Answer Keys

1. C	**2.** C	**3.** D	**4.** B	**5.** A	**6.** B	**7.** B	**8.** B	**9.** B	**10.** B
11. A	**12.** B	**13.** D	**14.** C	**15.** B	**16.** B	**17.** A	**18.** D	**19.** C	**20.** A
21. B	**22.** C	**23.** D	**24.** A	**25.** D	**26.** B	**27.** D	**28.** B	**29.** C	**30.** D
31. D	**32.** C	**33.** D	**34.** B	**35.** A					

Hints and Explanations

1. In the circuit NAND – NOR structure can be redrawn as AND – AND Structure



$\overline{A.ABC.C} = \overline{ABC} = \overline{A} + \overline{B} + \overline{C}$ Choice (C)

2. Positive numbers will be represented in their original binary magnitude but sign bit will be zero (0) to make it as positive number.
Negative Numbers are represented as 2's complement of their positive numbers representation in 2's complement signed number.
$+ 43 = 000101011$
$– 43 = 111010101$ (By taking 2's complement)
$+ 78 = 01001110$
$– 78 = 10110010$ (By taking 2's complement)
$+ 54 = 00110110$
$+ 96 = 01100000$ Choice (C)

3. Dual of function can be obtained by making min terms to max terms, 0 to 1, 1 to 0.
dual
$000 \leftrightarrow 111$
$001 \leftrightarrow 110$
$010 \leftrightarrow 101$
$011 \leftrightarrow 100$
$F = \Sigma m\ (0, 1, 6, 7)$
Dual is $f^D = \pi\ M\ (7, 6, 1, 0)$
$= \pi\ M\ (0, 1, 6, 7)$
$= \Sigma\ m\ (2, 3, 4, 5)$
Which is equal to f^1 (complement of f)
Choice (D)

4. $F = b + cd$
The term 'b' = - b - - - will have 16 min terms
the term cd = - - - cd – will have 8 min terms, out of those 8 min terms, four min terms will be having $b = 1$, already covered in previous term 'b'.
So remaining are $8 – 4 = 4$
So total min terms $= 16 + 4 = 20$ Choice (B)

5. P is $1 \sum A = \overline{A}.1 + A.\overline{1} = \overline{A}$

Q is $A \Theta 0 = \overline{A}.1 + A.0 = .\overline{A}$

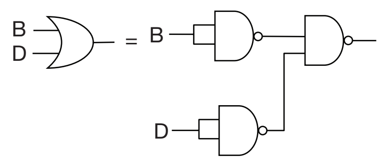
R is $0 \sum A = 0.\overline{A}. + 1.A. = A$

S is $A \Theta A = 1\,A + 0.\overline{A} = A$.
So P, Q work like inverter Choice (A)

6. $F(A, B, C, D) = \Sigma m\ (1, 3, 4, 5, 6, 7, 9, 11, 12, 13, 14, 15)$

AB \ CD	00	01	11	10
00		1	1	
01	1	1	1	1
11	1	1	1	1
10		1	1	

$F = B + D$



So 3, 2 input NAND gates are required to implement $F(A, B, C, D) = B + D$ Choice (B)

7. The first multiplexer output is
$Y = I_o\ \overline{S} + I_1 S$
$= x^1.\ x^1 + z.x = x^1 + zx = x^1 + z$
The output of second multiplexer is
$Y = I_1 S + I_o \overline{S}$
$= (x^1 + z)y + z.y^1$
$= x^1 y + yz + y^1 z$
$= x^1\ y + (y + y^1)z = x^1\ y + z$ Choice (B)

8. $Q_n = 0$, $Q_{n+1} = 1$
i.e. the state gets toggled i.e. when $J = 1$, $K = 1$
or the next state is set, $Q_{n+1} = 1$ i.e., when $J = 1$, $K = 0$
so $J = 1$, $K = x$ (either zero or 1)
so sum should be one, carry either zero or one.
So a,b,c should have only one 1 (sum = 1, carry = 0) or All inputs a,b,c can be 1 so that sum = 1, carry = 1.
Choice (B)

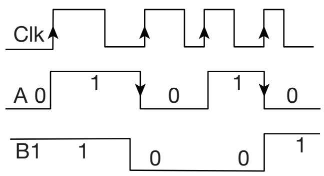
9. $J = Q_n \sum \overline{Q_n}\ \ (EX - OR\ of\ Q, \overline{Q}) = 1$

$K = Q_n \Theta\ \overline{Q_n}\ \ (EX - NOR\ of\ Q, \overline{Q})\ = 0$

When $J = 1$, $K = 0$, next clk pulse will give $Q = 1$, $\overline{Q} = 0$ Choice (B)

10. Given circuit is an Asynchronous counter. clk is connected as rising edge

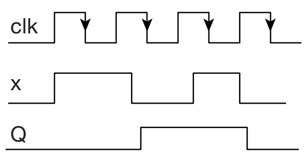
$\overline{Q}$ connected to rising edge means this is a UP counter.
A is LSB, B is MSB.
$\overline{Q_A}$ connected to rising edge
i.e., for every falling edge of Q_A, B will change so $AB = 11$



Clk	BA
0	10
1	11
2	00
3	01
4	10

Choice (B)

11. given is D flip flop
$Q_{n+1} = D$
$= x \sum \overline{Q_n} = x \Theta Q_n$
Q_{n+1} = Qn when $x = 1$
$Q_{n+1} = \overline{Q_n}$ when $x = 0$



Choice (A)

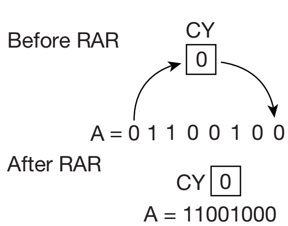
12. Given 8 bit DAC
Output current is 5.8mA
For input $(10010001)_2 = (145)_{10}$
$I_o = K$(input in Decimal)
5.8 mA = k (145)

$$k = \frac{5.8mA}{145} = 0.04mA$$

For input $(11110100)_2 = (244)_{10}$
$I_o = k$ (input) $= 0.04 \times 244 = 9.76$ mA

Choice (B)

13. MVI A, 64 H – move 64 H to Accumulator
MOV B, A $\rightarrow$ move (64H) A to B.
STC – set carry ($CY = 1$)
CMC – complement carry ($CY = 0$)
RAL – Rotate Accumulator left Arithmetically
Before RAR



XRA B $\rightarrow$ XOR Accumulator with B
$A = 11001000$
$B = \underline{01100100}$
$10101100 = ACH$

Choice (D)

14. LXI H, 4123H $\rightarrow$ 4123H are moved to HL register pair, i.e., $H = 41H$, $L = 23H$.
M stands for Memory Address specified by HL register pair
MOV A, M- contents of memory location
(Here 4123H) are moved to Accumulator
CMA – Complement Accumulator
MOV M,A – Contents of Accumulator are moved to memory location 4123H (HL contents)
i.e., the complemented contents
XRA A $\rightarrow$ XOR ACC with Acc only
So Acc = 00H. – reset Accumulator

Choice (C)

15. Given circuit P is a BJT inverter,
$V_{out} = (V_{cc} - I_{ccutoff} R_c)$ (logic 1) or $V_{out} = V_{CEsat}$ (logic 0)
It will not give full swing 0 to V_{CC} at output
Q is inverter by using NMOS with resistor
V_{out} (logic1) $= V_{cc} - I_D R_D$
So not possible to get full swing
R is CMOS circuit, which has PMOS, pull up and N MOS, pull down network, so full swing at output is possible

Choice (B)

16. $(-13)_{10} + (-28)_{10} = (-41)_{10}$
The operation in 2's complement signed representation also gives the same answer.
$(-41)_{10}$ in signed 2's complement representation is
$+41 = 00101001$
$-41 = 11010111 \rightarrow$ 2's complement

Choice (B)

17. Base 9 and base 3 are related ($3^2 = 9^1$)
2 digits of base 3 is equal to base 9 one digit.

base 3	base 9
00	0
01	1
02	2
10	3
11	4
12	5
20	6
21	7
22	8
100	10

Given number in base 3 is
$\underline{01}\ \underline{10}\ \underline{12}\ \underline{22}.\ \underline{20}\ \underline{11}\ \underline{21}$
1 3 5 8 . 6 4 7
$(1358 . 647)_9$

Choice (A)

18. The function output is 1 when ever the product of N_1, N_2 is less than or equal to 2
The minterms will be

N_1 \ N_2	0	1	3	2
AB \ CD	00	01	11	10
0 00	1	1	1	1
1 01	1	1		1
3 11	1			
2 10	1	1		

The max terms will be (for POS form)

AB \ CD	00	01	11	10
00				
01			0	
11		0	0	0
10			0	0

So $F = \left(\overline{A}+\overline{C}\right)\left(\overline{B}+\overline{C}+\overline{D}\right)\left(\overline{A}+\overline{B}+\overline{D}\right)$ Choice (D)

19. The excitation tables for *JK*, *D* are

Q_1	Q_O	J	K	D
0	0	0	X	0
0	1	1	X	1
1	0	X	1	0
1	1	X	0	1

Present state		Next state		Inputs		
Q_1	Q_O	Q_1	Q_O	J_1	K_1	D_O
0	0	1	0	1	X	0
1	0	1	1	X	0	1
1	1	0	1	X	1	1
0	1	0	0	0	X	0

From the above table

Writing the inputs interms of present state

$D_o = Q_1$; $J_1 = \overline{Q_0}$, $K1 = Q_O$ Choice (C)

20. The truth table can be written based on connection

B_3	B_2	B_1	B_0	Y_3	Y_2	Y_1	Y_o
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

By observation

Input is in BCD

Output is in EXS – 3 Choice (A)

21. The counter output is connected to DAC like $B_3 = Q_2$, $B_2 = 0$, $B_1 = Q_1$, $B_o = Q_o$

If we assume resolution is 1, (just for graph use)

The output for every clk pulse will be as shown, output of DAC is proportional to input binary

Clk	B_3	B_2	B_1	B_0	V_o
0	1	0	1	1	11
1	1	0	1	0	10
2	1	0	0	1	9
3	1	0	0	0	8
4	0	0	1	1	3
5	0	0	1	0	2
6	0	0	0	1	1
7	0	0	0	0	0
8	1	0	1	1	11

Choice (B)

22. When we consider two min terms AND operation

$mi.\ mj = 0$ if $i \neq j$

ex :– $A\overline{B}C.A\overline{B}\,\overline{C} = 0$; $ABC.\overline{A}\,\overline{B}\,\overline{C} = 0$

$mi.\ mj = mi$ if $i = j$

ex :– $A\overline{B}\,\overline{C}.A\overline{B}\,\overline{C} = A\overline{B}\,\overline{C}$

If two functions ANDed with minters

Then resultant is common min terms of the two functions

Example:

If $F_1\ (a,b,c) = m_1 + m_2 + m_3$

$F_2\ (a,b,c) = m_3 + m_4$

$F_1 \,.\, F_2 = (m_1 + m_2 + m_3)\ (m_3 + m_4)$

$= m_1.\ m_3 + m_1.\ m_4 + m_2.\ m_3 + m_2\ .\ m_4 + m_3\ .\ m_3 + m_3\ .m_4$

$= m_3$ (all other terms will be zero)

In the given problem $F(A,B,C) = \overline{X.Y}$

$= \Sigma m(1,3,4,5,7)$

So $XY = \Sigma m$ (0,2,6) (the remaining min terms)

$G(A,B,C) = Y.Z = \Sigma m$ (4,6)

X and *Y* are having (0, 2, 6) min terms in common, i.e., *Y* will have all these 3 min terms

Similarly *Y* and *Z* have (4,6) min terms in common,

So *Y* will have these 2 min terms also

So $Y = \Sigma m$ (0, 2, 4, 6) Choice (C)

23. From the above solution

$F(A,B,C) = \overline{XY} = \Sigma m$ (1, 3, 4, 5, 7)

$X.Y = \Sigma m$ (0, 2, 6)

G (*A*, *B*, *C*) $= Y Z = \Sigma m(4, 6)$

the min terms common to *X*, *Y* and *Y*, *Z* are

$XY\ YZ = XYZ = \Sigma m$ (6)

i.e., The output $x = 1, y = 1, z = 1$ only for the min term 6,

i.e., $ABC = 110$ Choice (D)

24. given function is in standard POS form

$f(P,Q,R) = \pi M$ (5, 6, 4) $= \Sigma m$ (0,1,2,3,7)

P \ QR	00	01	11	10
0	1	1	1	1
1			1	

$f\,(P, Q, R) = \overline{P} + QR$ Choice (A)

25. The LED will glow when the output of *OR* gate is zero. I.e., input of *OR* gate has to be logic 0 (both inputs) NAND gate output is zero when both inputs are logic 1. So both switches has to be open.
(when closed, logic level at input of NAND gate becomes zero).
But outputs of XNOR gate is logic 1 when switch $s2$ is open
So OR gate never gets zero –zero input condition.
The logic expression can be written as (OR output)
$$\overline{S_1.S_2}+(S2\oplus 1)=\overline{S_1}+S_2+S_2.=1$$
OR output is always logic 1, so Never glows
Choice (D)

26. Given circuit is an Asynchronous counter (ripple counter). All flip flops are in toggle mode. ($T = 1, J = K = 1$).
Q_A is LSB (clk input is connected to Q_A)
Negative edge Clk is connected from Q, so it works like UP counter.
$Q_C\, Q_B\, Q_A$ is the sequence, UP counter.
The NAND gate connected from $Q_B\, Q_C$
i.e., when ever output $Q_C\, Q_B\, Q_A$ becomes 110 or 111, the NAND gate output is zero.
i.e., the same zero applied to the active low asynchronous inputs pr, clr, clr of Q_A, Q_B, Q_C
so initial state is 001.

Clk	Q_C	Q_B	Q_A	
0	0	0	1	
1	0	1	0	
2	0	1	1	
3	1	0	0	
4	1	0	1	
5	~~1~~	~~1~~	~~0~~	→ 001

So total
5 different states
We will get Modulus = 5
Choice (B)

27.

					Q_2	$Q_1\Sigma Q_0$	Q_0	Q_3
Clk	Q_3	Q_2	Q_1	Q_0	D_3	D_2	D_1	D_0
0	0	1	0	0	1	0	0	0
1	1	0	0	0	0	0	0	1
2	0	0	0	1	0	1	1	0
3	0	1	1	0	1	1	0	0
4	1	1	0	0	1	0	0	1
5	1	0	0	1	0	1	1	1
6	0	1	1	1				

Choice (D)

28. MVI A, Byte1 → copy Byte1 to Accumulator
ORA A → OR Accumulator with Accumulator, store in Accumulator, this instruction will keep the contents of Accumulator as they are, $A + A = A$.
But carry, Auxiallary carry will be reset, remaining flags (sign, parity, zero) will be changed as per contents of Accumulator
JP SUB1 – Jump on plus to SUB1, so when sign flag is 0, i.e., positive number go to SUB1 address. (where the positive number will be the output at port Address).
XRA A → if the above Jump instruction fails, (-ve Number) then execution comes here xor Accumulator with Accumulator, store the result in Accumulator.
$A \sum A = 0$, so Accumulator will reset (00H)
OUT port Addr → out put the contents of Accumulator at port Addres. So all –ve numbers will become zero, and $+ve$ numbers will be output
HLT – STOP
Choice (B)

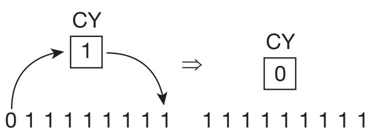
29. LXI H 4C38H → copy 4C38 H to HL register pair, i.e. H = 4CH, L = 38 H
MOV A,L → Move L = 38H to Accumulator,
ADD H → Add H = 4CH add Acc = 38H
Store in Accumulator
Acc = 0011 1000
H = 0100 1100
Acc = 10000100
Acc = 84H, and there is a auxiliary carry
DAA → Decimal Adjust Accumulator, if the reset is having any number more than 9 or if there is any auxiliary carry then DAA will add 6 to the result in Accumulator,
So Acc = 84 H + 06H = 8AH
MOV H, A → Acc = 8A H will be moved to H register.
Now HL = 8A38H
PCHL → Copy HL to program cainter
So PC = 8A38H
Choice (C)

30. The interfacing of 4 RAMS with 8bit microprocessor 8085 (i.e., 16 bit Address) is shown in given problem.
The lower order bus bits Ao – A9 are connected to Address bits of RAM (1024 Bytes = 2^{10}) (10 Address bits)
A_{12}, A_{11} are connected to selection bits of De multiplexer
The input has to be 1, so AND gate output has to be 1
Address of RAM #4 is
$A_{15}\, A_{14}\, A_{13}\, A_{12}\, A_{11}\, A_{10}\, A_9\, A_8\, A_7 \ldots\ldots A_0$
0 1 0 0 0 0 0 0 0 0
to
0 1 0 0 0 0 1 1 1 1
So range of address = 4000H to 43FFH
Address of RAM # 3 is
$A_{15}\, A_{14}\, A_{13}\, A_{12}\, A_{11}\, A_{10}\, A_9\, A_8\, A_7 \ldots\ldots A_0$
0 1 0 0 1 0 0 0 0 0
to
0 1 0 0 1 0 1 1 1 1
range of address = 4800 – 4BFFH
Address of RAM #2 is
Selections line
$A_{15}\, A_{14}\, A_{13}\, A_{12}\, A_{11}\, A_{10}\, A_9\, A_8\, A_7 \ldots\ldots A_0$
0 1 0 1 0 0 0 0 0 0
to
0 1 0 1 0 0 1 1 1 1
range = 5000H to 53FFH
Address range of RAM # 1 is
$A_{15}\, A_{14}\, A_{13}\, A_{12}\, A_{11}\, A_{10}\, A_9\, A_8\, A_7 \ldots\ldots A_0$

0 1 0 1 1 0 0 0 0 0
to
0 1 0 1 1 0 1 1 1 1
range = 5800 – 5BFFH Choice (D)

31. MVI B, 46H → Load b with 46H, B = 46H
MVI A, 38H → Load Accumulator with 38H, A = 38H
ADD $B \rightarrow A = A + B \Rightarrow$
A = 00111001
B = 01000110

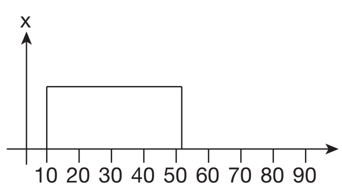
A = 01111111
STC – set carry CY = 1
RAL → rotate Arithmetically left (Accumulator rotation with carry)



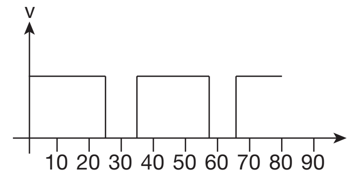
XRI F0H → Accumulator with F0H
A = 1 1 1 1 1 1 1 1
F0H = 1 1 1 1 0 0 0 0
________________ ⊕ XOR
0 0 0 0 1 1 1 1
After XOR, Accumulator contents are 0FH
Choice (D)

32. When B = 0, A will get enabled and $y = A$
When B = 1, C will get enabled and $y = C$
So Data selector 2 x 1 MUX. Choice (C)

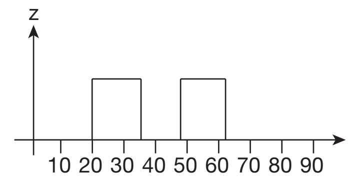
33.



Given x Starting from 10ns And is 1 for next 40 ns



Y is 5 seconds Delayed version of Inverted z (z is AND of Y and X with 10 sec delay)



Choice (D)

34. From the given circuit, inputs are

$$D_x = Z, D_y = \overline{X}, \overline{Z}, D_z = \overline{Z + \overline{Y}} = \overline{Z}.Y$$

As all flip flops are D flip flops, same output (as of input) will be the next state
Given initially xyz = 011.
So Dx = 1, Dy =0, Dz=0
So next state xyz = 100. Choice (B)

35.

Clk	X	Y	Z	$Dx = Z$	$Dy = \overline{x}\,\overline{z}$	$Dz = \overline{z}y$
0	0	0	0	0	1	0
1	0	1	0	0	1	1
2	0	1	1	1	0	0
3	1	0	0	0	0	0
4	0	0	0			

After 4 clk pulses again come back to original state (000) so number states are 4 Choice (A)