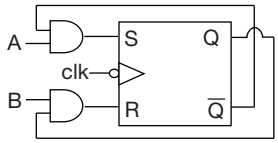
DIGITAL CIRCUITS TEST 2

Number of Questions: 35 **Time: 90 min.**

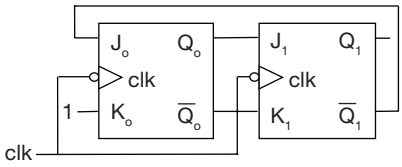
Directions for questions 1 to 35: Select the correct alternative from the given choices.

1. The following flip flop is



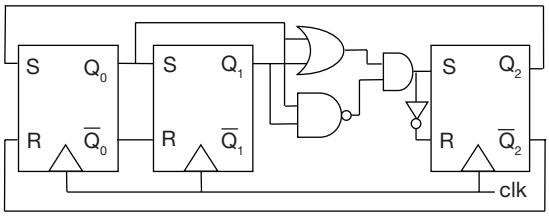
(A) D flip flop when A = 0
(B) D flip flop when A = B
(C) T flip flop when A = 0
(D) T flip flop when A = B

2. The flip flops used in this circuit are master slave JK flip flops. If the counter is initially at reset state after how many clock pulses it gets reset?



(A) 2 (B) 3
(C) 4 (D) 1

3.

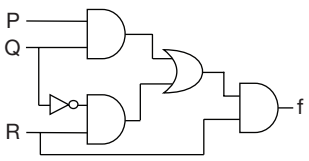


The above counter shown has initial state $Q_2\ Q_1\ Q_0$ = 111(7), then the next states are? (in decimal) ($Q_2\ Q_1\ Q_0$)
(A) 7621435 (B) 7352614
(C) 7324165 (D) 7514236

4. If $a \le b$, which of the following is true
(P) $a^1 + b = 1$ (Q) $a^1 \le b^1$
(R) $ab^1 = 0$
(A) P, Q (B) P, R
(C) Q, R (D) P, Q, R

5. If $a = (b + c)\ (b^1 + c^1)$, then the value of b is
(A) $(a^1 + c)\ (a + c^1)$ (B) $a^1c + ac^1$
(C) $a^1c^1 + a^1c$ (D) $(a^1 + c^1)(a + c^1)$

6. Calculate switching function realized by this network in minimized SOP form.

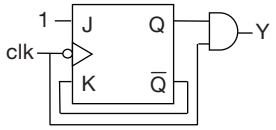


(A) $PQ + \overline{Q}R$ (B) $PQR + \overline{Q}R$
(C) $PR + \overline{Q}R$ (D) $P\overline{Q} + R$

7. The max term expression of a four variable even function is
(A) π M (0, 2, 4, 6, 8, 10, 12, 14)
(B) π M(1, 3, 5, 7, 9, 11, 13, 15)
(C) π M (0, 3, 5, 6, 9, 10, 12, 15)
(D) π M (1, 2, 4, 7, 8, 11, 13, 14)

8. Find which of the following is not a minimum sum of the products expression for $f(w, x, y, z)$
$= \Sigma m(0, 3, 5, 7, 8, 9, 10, 12, 13) + d(1, 6, 11, 14)$
(A) $\overline{w}z + x\overline{y} + w\overline{x} + \overline{y}z$ (B) $w\overline{x} + w\overline{y} + \overline{x}\overline{y} + \overline{w}z$
(C) $\overline{x}\overline{y} + \overline{w}z + w\overline{z} + \overline{y}z$ (D) $w\overline{z} + \overline{x}\overline{y} + w\overline{y} + \overline{w}z$

9. The input clock frequency is 10kHz, then the frequency of Y is (initially $Q = 0$)



(A) 5 kHz (B) 10 kHz
(C) 2.5 kHz (D) 0 Hz

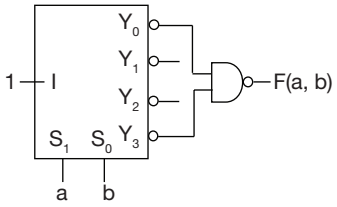
10. A Hexa Decimal Number X is converted to binary initially, then all zero and one's are interchanged with 1's and 0's. Then it was incremented by 1 in binary, finally the binary number was converted back to Hexa Decimal again, this number is
(A) 15's complement of X.
(B) 16's complement of $X + 1$.
(C) 15's complement of $X + 1$.
(D) 1's complement of X.

11. The minimum decimal equivalent of the number $(21A)_x$ is
(A) 538 (B) 1032
(C) 263 (D) 220

12. If $(3.5)_{\text{base } 6} + (2.3)_{\text{base } 6} = (X)_{\text{base } 6}$ then the value of X is
(A) 5.8 (B) 10.2
(C) 6.2 (D) 5.6

13. A number in 4 bit two complement signed representation is $a_3\ a_2\ a_1\ a_0$. The same number, when stored using 8 bits will appear like.
(A) 0000 $a_3\ a_2\ a_1\ a_0$
(B) $\overline{a}_3\ \overline{a}_3\ \overline{a}_3\ \overline{a}_3\ a_3\ a_2\ a_1\ a_0$
(C) $a_3a_2a_1a_0a_3a_2a_1a_0$
(D) $a_3a_3a_3a_3a_3a_2a_1a_0$

14.



In the above circuit the function $F(a, b)$ in POS form

(A) $(a + b)(a^1 + b^1)$ (B) $(a^1 + b)(a + b^1)$

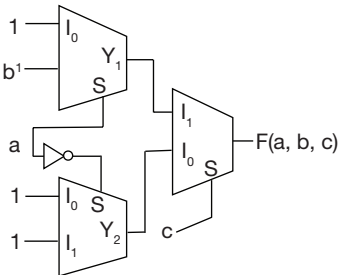
(C) $(a + b^1)(a^1 + b^1)$ (D) $(a + b)(a^1 + b)$

15. A combinational circuit takes input in the range of 000 to 101, (remaining combinations are unused) The output of the circuit is 1 when ever input is a power of 2 (in decimal) find the minimized expression for output, if x, y, z are inputs of the combinational circuit.

(A) $x^1 y \sum z^1$ (B) $(x + y) \odot z$

(C) $x^1 y^1 \sum z$ (D) $(x + y) \sum z$

16.

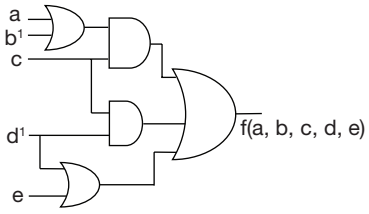


The function $F(a, b, c)$ is

(A) $a^1 + b^1 + c$ (B) $(abc)^1$

(C) $(a^1 + b^1)c^1$ (D) $(a + b)^1 + c^1$

17. If the following circuit is converted to all-NAND network, then how many number of NAND gates are required? (inverted inputs are available)



(A) 3 (B) 4

(C) 5 (D) 6

18. A 5 × 32 Decoder can be constructed by using

*S*1: four 3 × 8 Decoders and one 2 × 4 Decoder

*S*2: five 2 × 4 Decoders

*S*3: eight 2 × 4 Decoders, one 3 × 8 Decoder

*S*4: four 3 × 8 Decoders

Consider all the decoders are having enable input.

(A) *S*1, is true alone (B) *S*1, *S*3, *S*4 are true

(C) *S*2, *S*3 are true (D) *S*1, *S*3 are true

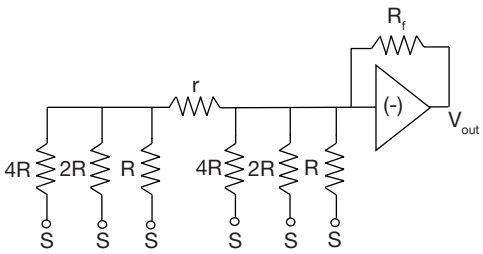
19. A digital to analog converter accepts 12 input bits, i.e., has a resolution of 12 bits, and provides an output which is 12V maximum.

Suppose that as a result of drift of component values etc,. The output may be in error by an amount ΔV. How large can ΔV be before the LSB would no longer be significant?

(A) 5.51 mV (B) 2.93 mV

(C) 9.3 mV (D) 3.75 mV

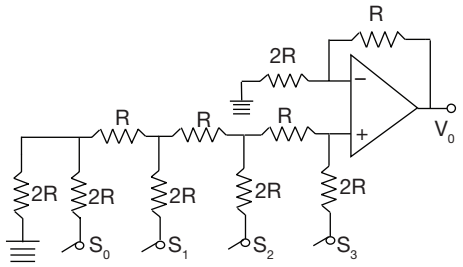
20. A 3 bit Digital to Analog converter is modified as follows, to make it 6 bit Digital to analog converter. So what will be the value of resistor 'r' for proper operation?



(A) 16 R (B) 8 R

(C) 4 R (D) 2 R

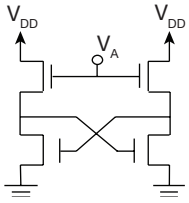
21. The switches S_i will be connected to V_R = 1V for logic 1, and will be connected to 0V for logic 0. Find the output V_o for input $S_3S_2S_1S_0 = 0101$



(A) 0.468 V (B) 5 V

(C) 7.5 V (D) 0.3125 V

22. The following circuit is $(0 < V_A < V_{DD})$



(A) 1 bit counter

(B) 1 bit memory element

(C) 1 bit DRAM cell

(D) 1 bit buffer

23. How many number of 256 × 8 bit RAMs are required to build 1kB × 16 RAM?

(A) 5 (B) 6

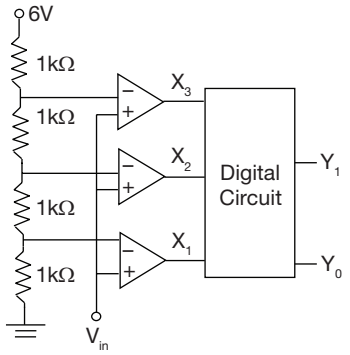
(C) 4 (D) 8

24. A 2048 × 8 bit memory element is interfaced with 8085 microprocessor, if the address of first memory location

in the RAM is 0900H. Then the address of the last memory location will be?

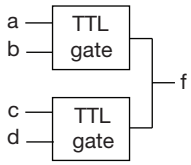
(A) 1000H (B) 0FFFH
(C) 27FFH (D) 10FFH

25. The circuit shown in the figure below works as 2-bit analog to digital converter for $0 \le V_{in} \le 6V$. The MSB of output Y_1, expressed as Boolean function of input X_3, X_2, X_1 is given by



(A) $X_1 + X_3$ (B) $X_2 + X_1$
(C) $X_3 + X_2$ (D) X_3

26. Two basic TTL gates are connected as shown in the figure, the function f is



(A) $ab + cd$ (B) $(a + b)(c + d)$
(C) $(a^1b^1 + c^1d^1)^1$ (D) $(a^1 + b^1)(c^1 + d^1)$

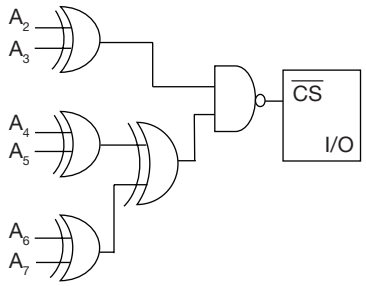
27. The voltage and current parameters of ECL logic family are given by
$V_{OH} = -0.76$ V, $V_{IH} = -1.1$ V,
$V_{OL} = -1.58$ V, $V_{IL} = -1.25$ V
$I_{OH} = 3$ mA, $I_{IH} = 107$ μA, $I_{OL} = 3.7$ mA, $I_{IL} = 137$ μA
The fan out, noise margin of the logic family are?

(A) 28, 0.34 V (B) 27, 0.34 V
(C) 28, 0.33 V (D) 27, 0.33 V

28. 4000: L X I SP, 5000 H
4003: L X I H, 5050 H
4006: SPHL
4007: PUSH H
4008: PUSH B
4009; CALL 4050H
400C: POP D
400D: HLT
at the end of this program, contents of SP and PC are

(A) 4FFEH, 400DH (B) 5048H, 400EH
(C) 504EH, 400EH (D) 5052H, 400EH

29. An I/O device is interfaced with μP 8085 in the following circuit diagram then the range of address for the I/O is



(A) A8H – ABH (B) 80H – 83H
(C) 68H – 6BH (D) 44H – 47H

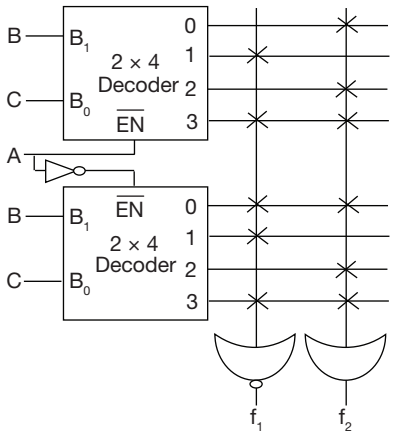
30. MVI A, 69H
CMA
MOV B, A
STC
CMC
RAR
RAR
XRA B
NOP
at the end of this program contents of Accumulator, Carry are?

(A) B3, 1 (B) B3, 0
(C) F3, 1 (D) F3, 0

31. MVI A, Byte1
ORA A
JM Output
XRA A
Output: OUT Port
HLT
The program will give output,

(A) negative numbers
(B) positive numbers
(C) odd numbers
(D) negative numbers or zero

Common Data for Questions 32 and 33:



32. The function $f_1(A, B, C)$ in SOP form is

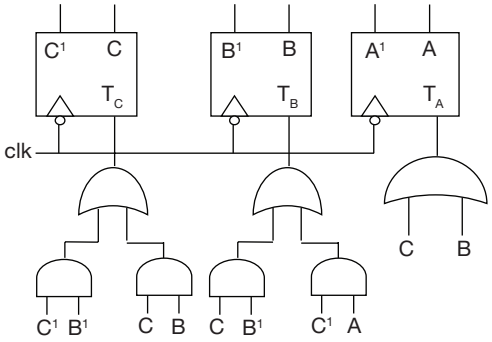
(A) $\overline{A}B + B\overline{C}$ (B) $\overline{A}\,\overline{C} + B\,\overline{C}$
(C) $\overline{A}B + A\overline{C}$ (D) $\overline{A}C + B\overline{C}$

33. The function $f_2(A, B, C)$ in POS form is

(A) $\overline{B}+A$ (B) $\overline{A}+C$

(C) $B+\overline{C}$ (D) $A+\overline{C}$

Statement for Linked Answer Question 34 and 35:



34. If the counter is initially at reset state, the total number states are (i.e., modulus of counter is)

(A) 6 (B) 5

(C) 7 (D) 8

35. Initially ABC is 100 then next state of the counter is?

(A) 100 (B) 101

(C) 111 (D) 110

Answer Keys

1. D	**2.** B	**3.** C	**4.** B	**5.** B	**6.** C	**7.** D	**8.** A	**9.** B	**10.** C
11. C	**12.** B	**13.** D	**14.** B	**15.** D	**16.** B	**17.** A	**18.** D	**19.** B	**20.** C
21. A	**22.** B	**23.** D	**24.** D	**25.** C	**26.** D	**27.** D	**28.** C	**29.** D	**30.** B
31. D	**32.** B	**33.** C	**34.** B	**35.** C					

Hints and Explanations

1. The characteristic equation of SR flip flop is

$Q_{n+1} = S + \overline{R}\,Q_n$

Given (from circuit) $S = A.\overline{Q_n}$, $R = B.Q_n$

$Q_{n+1} = A\,\overline{Q_n} + \overline{B.Q_n}\,Q_n$

$= A\overline{Q_n} + \left(\overline{B} + \overline{Q_n}\right)Q_n$

$Q_{n+1} = \mathrm{A}\,\overline{Q_n} + \overline{B}\,Q_n$

The equation like JK flip flop

(JK equation $Q_{n+1} = J\overline{Q_n} + \overline{K}Q_n$)

So it works like T flip flop if $A = B$.

Choice (D)

2. Master slave flip flop also works like normal flip flop only, to eliminate race around condition in JK latch, we go for JK master slave flip flop.

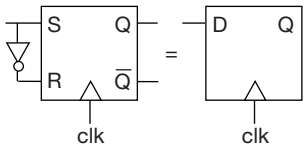
From the circuit $J_0 = \overline{Q_1}$, $K_0 = 1$, $J_1 = Q_0$, $K_1 = \overline{Q_o}$

clk	Q_1	Q_0	$J_1=Q_0$	$K_1=\overline{Q_0}$ $K_0=1$	$J_0=\overline{Q_1}$
0	0	0	0	1	1 1
1	0	1	1	0	1 1
2	1	0	0	1	0 1
3	0	0			

3 clk pulses required to reset again.

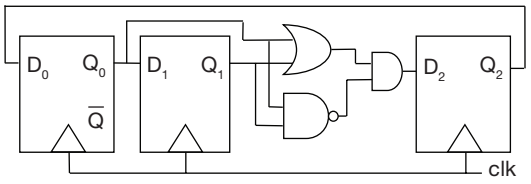
Choice (B)

3.



We can observe that SR connected in D flip flop mode, S, R are connected with normal (Q), complemented $\left(\overline{Q}\right)$ out put forms.

We can draw the circuit as follows



From given circuit $D_0 = Q_2$, $D_1 = Q_0$

$D_2 = \left(Q_1 + Q_0\right)\overline{\left(Q_1.Q_0\right)} = \left(Q_1 + Q_0\right)\left(\overline{Q_1} + \overline{Q_0}\right) = Q_1 \oplus Q_0$

clk	Q_2	Q_1	Q_0	$D_2=Q_1 \oplus Q_0$	$D_1=Q_0$	$D_0=Q_2$
0	1	1	1	0	1	1
1	0	1	1	0	1	0
2	0	1	0	1	0	0
3	1	0	0	0	0	1
4	0	0	1	1	1	0
5	1	1	0	1	0	1
6	1	0	1	1	1	1
7	1	1	1			

Choice (C)

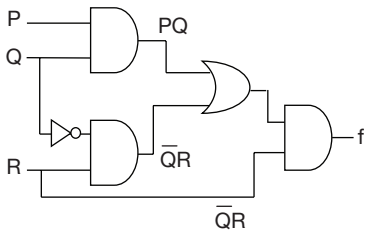
4. If $a \le b$ then

a	b	$a^1 + b$	ab^1
0	0	1	0
0	1	1	0
1	1	1	0

($ab = 10$ is not valid condition for $a \le b$)
We can observe that $a^1 \ge b^1$, so only (*P*) $a^1 + b = 1$, (*R*) $ab^1 = 0$ are true. Choice (B)

5. From given $a = (b + c)(b^1 + c^1)$
$= bc^1 + b^1 c = b \sum c$
EXOR with c both sides
$a \sum c = b \sum c \sum c = b \sum 0 = b$
So $b = a \sum c = a^1 c + ac^1$ or $(a + c)(a^1 + c^1)$.
Choice (B)

6.



$\overline{Q}R$

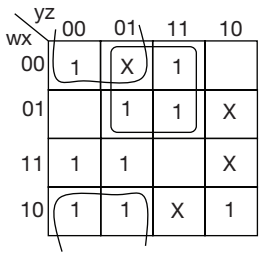
$f = (PQ + \overline{Q}R)R = PQR + \overline{Q}R$

$= (PQ + \overline{Q})\mathrm{R} = (P + \overline{Q})\mathrm{R} = PR + \overline{Q}R$

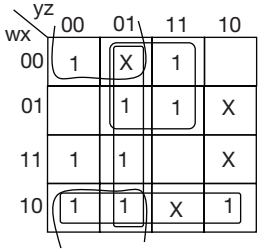
Choice (C)

7. Even function is a Boolean function, and it will be equal to 1, if the input variables have an even number of 0's.
(odd function is a Boolean function for which output is 1, for input combinations with odd number of 1's)
So for 4 variables, even number of zeroes occur for input combinations
0000, 0011, 0101, 0110, 1001, 1010, 1100, 1111
For these combinations, even function output is 1.
So remaining terms are max terms.
So $f_{even} = \prod M(1, 2, 4, 7, 8, 11, 13, 14)$ Choice (D)

8.



$\overline{x}\,\overline{y}, \overline{w}z$ is the essential prime implicants, remaining prime implicants can be used to cover all the min terms.



$\overline{w}\overline{z}, \overline{x}\overline{y}, \overline{w}\overline{x}, \overline{y}\overline{z}$ will not implement the k-map as in the above k-map min term $wxyz = 1100$ is not covered.
Choice (A)

9. When $Q = 0$, initially, $\overline{Q} = 1$
So $J = K = 1$, by applying first clk pulse $Q_{n+1} = 1$, Then $\overline{Q}_{n+1} = 0$. So $J = 1$, $K = 0$, after clock pulse $Q_{n+2} = 1$, … and for next clock pulses it will remain in same state, so the frequency of $Q = 0$Hz ($Q = 1$ always) but $Q = 1$, so the clk pulse ANDed with $Q = 1$ and Y is same as clk pulse so frequency of Y is 10kHz. Choice (B)

10. The explained process is converting to binary, and interchanging 1 to 0's and 0's to 1's, same as 1's complement in binary, by adding 1 to 1's complement number we will get 2's complement.
Converting it back to Hexa Decimal, gives 16's complement of X, or it is also same as 15's complement of the Hexa Decimal number $X + 1$. Choice (C)

11. Here $(21A)_x$ is a number with unknown number system x.
When we need to find out minimum decimal equivalent value, then the base of the number system should be minimum.
Here ($A = 10$) is the largest number in the number system, so possible base will be 11.
So minimum decimal equivalent of $(21A)_{11} = 2 \times 11^2 + 1 \times 11 + 10 = 263$. Choice (C)

12.
$$\begin{array}{r} 3.5 \\ +\ \underline{2.3} \\ ? \end{array}$$
$5 + 3 = 8$
$(12)_6$ so result is 2 and carry is 1.
$$\begin{array}{r} 1 \\ 3.5 \\ +\underline{2.3} \\ ?.2 \end{array}$$
$1 + 3 + 2 = 6$
$(10)_6$ so result is 0 and carry is 1
$$\begin{array}{r} 3.5 \\ +\ \underline{2.3} \\ 10.2 \end{array}$$
Choice (B)

13. When a signed integer stored in 2's complement format, the MSB will give the sign, if MSB = 0, then it's a positive number, else if MSB = 1 it's a negative number.

When we are extending the number of bits, the sign of the number should not change, so all negative numbers will be appended with 1's and all positive numbers will be appended with 0's. So the same MSB will be repeated for extra bits on left hand side.

Choice (D)

14. Given circuit is Demultiplexer

Output equation are $Y_0 = I\bar{S}_1\bar{S}_0$

$$Y_1 = I\bar{S}_1 S_0$$

$$Y_2 = I S_1 \bar{S}_0$$

$$Y_3 = I S_1 S_0$$

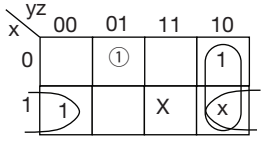
$$F(a, b) = \overline{\bar{Y}_0.\bar{Y}_3} = Y_0 + Y_3 = 1.a^1 b^1 + 1.ab$$

$$= a^1 b^1 + ab = (a^1 + ab)(b^1 + ab)$$

By applying $x + yz = (x + y)(x + z)$

$$= (a^1 + b)(a + b^1)$$ Choice (B)

15. If the output of the circuit is F then $F(x, y, z) = \Sigma(1, 2, 4) + \phi\, d(6, 7)$ in the given range 000 to 101, only for inputs 001, 010, 100 output is 1 (min terms) 110, 111 are unused combinations (don't cares)



$F(x, y, z) = xz^1 + yz^1 + x^1 y^1 z$

$= (x + y)z^1 + x^1 y^1 z$

$= (x^1 y^1)^1 z^1 + (x^1 y^1)z = (x + y)z^1 + (x + y)^1 z$

$= x^1 y^1 \odot z = (x + y) \sum z$ Choice (D)

16. Output of 1st MUX $Y_1 = 1.a^1 + b^1.a$

$= a^1 + b^1$

Output of 2nd MUX $Y_2 = 1.a + 1.a^1 = 1$

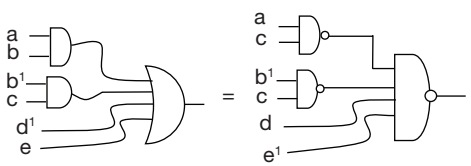
Output of 3rd MUX $F(a, b, c) = Y_1.c + Y_2.c^1$

$= (a^1 + b^1)c + 1.c^1 = a^1 + b^1 + c^1$ Choice (B)

17. Given function has to be in SOP form, so it can be implemented by AND-OR gates, same as NAND-NAND gates

$f(a, b, c, d, e) = (a + b^1)c + cd^1 + (d^1 + e)$

$= ac + b^1 c + cd^1 + d^1 + e$



$= ac + b^1 c + d^1 + e$ Choice (A)

18. 5 × 32 Decoder has 32 outputs, we can built 32 outputs By using four 3 × 8 Decoders, and again one of these four 3 × 8 Decoders can be selected by using a 2 × 4 Decoder

Similarly we can build 32 outputs by using eight 2 × 4 Decoders, and one of these 8 Decoders can be selected by using one 3 × 8 Decoder.

So valid statements are $S1$ and $S3$. Choice (D)

19. The LSB (Least Significant Bit) would be no longer be significant if ΔV is more than LSB value.

So here max output is = 12V.

Maximum input we can apply (12 bit) = $2^{12} - 1$

So resolution = $\dfrac{12}{2^{12} - 1} = 2.93\,\text{mV}$

Value of $LSB = 2^{\circ} \times$ resolution = resolution = 2.93mV.

Choice (B)

20. The $S_2\ S_1\ S_0$ are lower order bits, $S_5\ S_4\ S_3$ are higher order bits so the current due to bits $S_2\ S_1\ S_0$ should be one eighth of the current due to $S_5\ S_4\ S_3$.

The resistor r has been inserted to provide the attenuation.

Such attenuation, is possible when $r = 4R$. Choice (C)

21. Given circuit is a DAC. ($R - 2\ R$ type)

So the voltage at non inverting terminal is

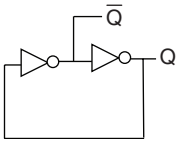
$$V_+ = \frac{V_R}{2^n}\ (S_0 \times 2^0 + S_1 \times 2^1 + S_2 \times 2^2 + S_3 \times 2^3)$$

$$= \frac{1}{16} \times (1 + 0 + 4 + 0) = \frac{5}{16}$$

$$V_0 = \left(1 + \frac{R}{2R}\right)\frac{5}{16} = \frac{3}{2} \times \frac{5}{16} = \frac{1}{2} \times \frac{15}{16} = 0.46875\ \text{V}$$

Choice (A)

22. The given circuit has 2 NMOS inverters, connected back to back,



it forms a 1 bit memory element.

1 bit buffer will have 1 input and 1 output

Because of feedback connection it will work like basic memory element latch,

This is the basic structure in SRAM cell, Dynamic RAM requires only 1 MOSFET for 1 bit storage, as the bit will be stored in gate capacitance. Choice (B)

23. No. of memory elements = $\dfrac{\text{required memory}}{\text{Available memory}}$

$$= \frac{1kB \times 16}{256 \times 8} = \frac{1024 \times 16}{256 \times 8} = 8$$ Choice (D)

24. Address of last memory location – Address of first Memory location

= (Number of address locations – 1)

Here given RAM number of address locations = 2048

$(2048)_{10}$ = 0800H

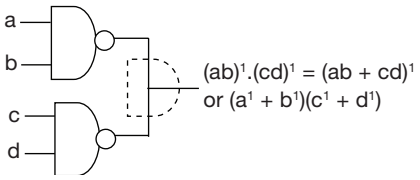
0800H – 1 = 07FFH

X – 0900H = 07FFH

X = 07FF + 0900H = 10FFH Choice (D)

25. The given circuit is flash type ADC, and the Digital circuit is priority Encoder. So when Y_1(MSB) = 1, then output can be 11 or 10 so input X_3 has to be present or if not X_3, X_2 has to be there $Y_1 = X_3 + \overline{X}_3\ X_2 = X_3 + X_2$ (Priority Encoder equation) Choice (C)

26. Basic TTL gate is NAND gate, and TTL has wired AND operation.
So given circuit is like



Choice (D)

27. **Noise Margin**
$\Delta 1 = -0.76 - (-1.1) = 0.34V$
$\Delta 0 = -1.25 - (-1.58) = 0.33V$
Noise margin is min ($\Delta 0$, $\Delta 1$) = 0.33V.

Fanout:- $N_1 = \frac{I_{OH}}{I_{IH}} = \frac{3mA}{107\mu A} = 28$

$N_0 = \frac{I_{OL}}{I_{IL}} = \frac{3.7mA}{137\mu A} = 27$

Fanont = min (N_1, N_0) = 27 Choice (D)

28. As the above programs ends at memory location 400*DH*, the address of next memory location is 400*EH*, which will be stored in Program Counter at the end of the program.
L X I SP, 5000H → load SP = 5000H
L X I H, 5050H → load HL = 5050H
SPHL → move HL to SP, so SP = 5050H
PUSH H → SP decremented by 2 (SP – 2)
PUSH B → SP decremented by 2 (SP – 4)
CALL 4050H → after call instruction, again returned to next instruction, so no charge for SP.
POP H → increment SP by 2 (SP – 4 + 2) = SP – 2
HLT – stop
So contents of stack pointer are 5050-2 = 504*EH*.
Choice (C)

29. For the chip select to get enable CS = 0.
Nand gate output = 0, when inputs are 1 and 1.
So Exor operation of A_2, A_3 and A_4, A_5, A_6, A_7 should be 1.
exor operation gives output 1, when input is having odd number of 1's

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	1	1	0	1	0	x	x	→ E 8 – EB H
1	1	1	0	0	1	x	x	→ E 4 – E7 H
.....								
0	0	0	1	0	1	x	x	→ 14 – 17 H
0	0	0	1	1	0	x	x	→ 18 – 1B H

In this way many ranges we will get
as per options 44 – 47H Choice (D)

30. MVI A, 69H → A = 69H
CMA → complement Accumulator
Now A = 96H
MOV B, A → Copy A to B → B = 96 H
STC – set carry CY = 1
CMC – complement carry CY = 0
RAR – rotate arithmetically right (Accumulator)

0 0
1 0 0 1 0 1 1 0 → 0100 1011

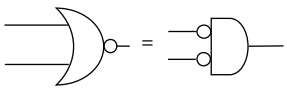
RAR – rotate arithmetically right (Accumulator)

0 0
0 1 0 0 1 0 1 1 → 0 0 1 0 0 1 0 1

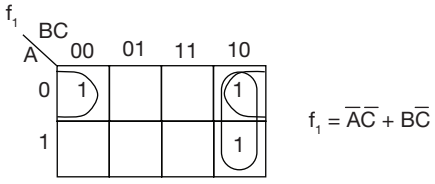
XRA B – XOR B with Accumulator store in Accumulator
A = 0 0 1 0 0 1 0 1
B = 1 0 0 1 0 1 1 0 (XOR)
1 0 1 1 0 0 1 1
A = 10110011, CY = 0 (logical operation) Choice (B)

31. MVI A, Byte1 → A = Byte1, copy number to A.
ORA A – make $A + A = A$, contents of Accumulator remain same but CY = 0, and other flags will change as per number in Accumulator.
JM output – Jump on minus to output port if S = 1 go to output.
XRA A – else XOR A with A, $A \sum A = 00H$
A = 00H
OUT port → send the contents of Acc to output port
HLT – stop.
So if there is any negative number it will be the output or zero is the output. Choice (D)

32. Given is a 3 × 8 Decoder with two 2 × 4 Decoders, and a NOT gate, LSB are connected to inputs of Decoder (B_1 B_0 = BC), MSB (A) is connected to check which decoder has to be selected by using enable input, When A = 0, first Decoder will be selected, when A = 1, second decoder will be selected.
f_1 is connected through NOR gate

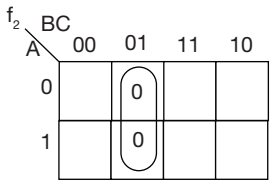


outputs of Decoder (here active High outputs) are min terms, min terms connected to NOR gate.
$f_1 = \pi M(1, 3, 4, 5, 7) = \Sigma m(0, 2, 6)$ because in second decoder A = 1, BC vary as per inputs applied so 4, 5, 6, 7 are output of second decoder (min terms)



Choice (B)

33. f_2 is connected to OR gate, so sum of min terms
$f_2 = \Sigma m(0, 2, 3, 4, 6, 7) = \pi M(1, 5)$



$f_2 = \left(B + \overline{C}\right)$

Choice (C)

34. From the circuit diagram
$T_A = C + B$, $T_B = CB^1 + C^1 A$, $T_C = CB + C^1 B^1 = B \odot C$

Clk	$Q_A\ Q_B\ Q_C$	$T_A\ T_B\ T_C$
0	0 0 0	0 0 1
1	0 0 1	1 1 0
2	1 1 1	1 0 1
3	0 1 0	1 0 0
4	1 1 0	1 1 0
5	0 0 0	

So mod–5 counter, when it starts from reset state.

Choice (B)

35. If present state ABC = 100
then $T_A\ T_B\ T_C = 011$ then next states ABC = 111.

Choice (C)