Number of Questions: 35 **Section Marks: 90**

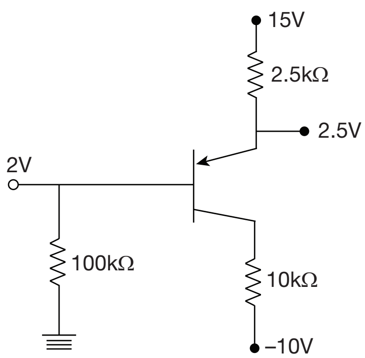
Directions for questions 1 to 35: Select the correct alternative from the given choices.

1. The output impedance of a BJT under common collector configuration is
   (A) high (B) medium
   (C) low (D) very high

2. Body effect in MOSFETS results in
   (A) Increase in the value of output resistance
   (B) Increase in the value of transconductance
   (C) change in the value of threshold
   (D) decrease in the value of transconductance

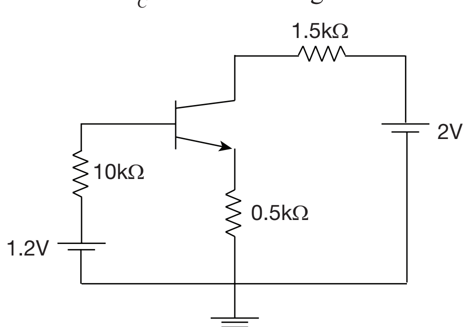
3. The modified work function of an *n*-channel MOSFET is – 0.75V. If the interface charge is 2×10^{-4} C/m^2 and the oxide capacitance is 250μF/m^2, the flat band voltage is
   (A) 1.4 V (B) 1.25 V
   (C) 1.75 V (D) 0.2 V

4. A circuit using the BJT is shown in the below figure, the value of β is



   (A) 250 (B) 175
   (C) 176 (D) 249

5. For the circuit shown in the below figure, by assuming β = 150 and V_{BE} = 0.7V, the best approximation for the collector current I_C in the active region is

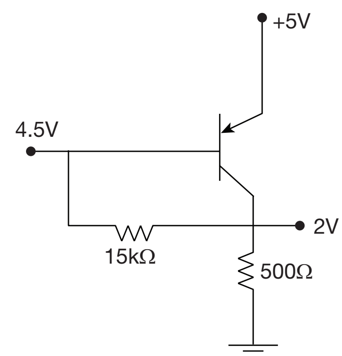


   (A) 0.65 mA (B) 2.5 mA
   (C) 1.23 mA (D) 0.87 mA

6. The purpose of emitter capacitor across R_E is to
   (A) reduce noise in the amplifier
   (B) protect the transistor
   (C) avoid voltage gain drop
   (D) provide biasing

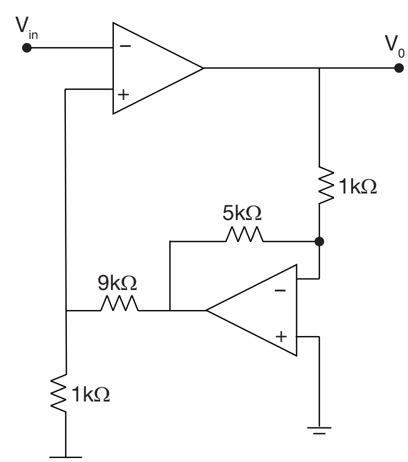
7. What are the effects of cascode amplifier stages?
   (1) Low input impedance
   (2) High input impedance
   (3) Wideband amplifier
   (4) Narrow band amplifier
   (A) (1) and (3) only (B) (2) and (3) only
   (C) (1) and (4) only (D) (2) and (4) only

8.



   The value of β is
   (A) 24 (B) 25
   (C) 26 (D) 27

9. For the circuit shown in figure, the voltage gain $\left(\frac{V_0}{V_i}\right)$ is



   (A) $\frac{-1}{2}$ (B) 1
   (C) –2 (D) 4

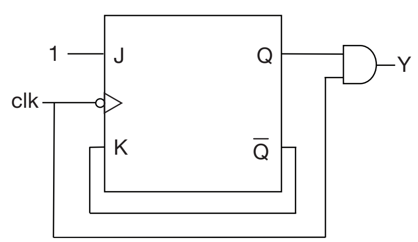
10. Which one of the following oscillators is well suited for the generation of wide range audio – frequency waves?
(A) Hartley oscillator
(B) Wein – bridge oscillator
(C) Colpitt's oscillator
(D) crystal oscillator

11. If $a = (b + c)(b^1 + c^1)$, then the value of b is
(A) $(a^1 + c)(a + c^1)$ (B) $a^1c + ac^1$
(C) $a^1c^1 + a^1c$ (D) $(a^1 + c^1)(a + c^1)$

12. The max term expression of a four variable even function is?
(A) $\pi M(0, 2, 4, 6, 8, 10, 12, 14)$
(B) $\pi M(1, 3, 5, 7, 9, 11, 13, 15)$
(C) $\pi M(0, 3, 5, 6, 9, 10, 12, 15)$
(D) $\pi M(1, 2, 4, 7, 8, 11, 13, 14)$

13. Find which of the following is not a minimum sum of the products expression for $f(w, x, y, z) = \Sigma m(0, 3, 5, 7, 8, 9, 10, 12, 13) + d(1, 6, 11, 14)$
(A) $\bar{w}z + \bar{x}\bar{y} + w\bar{x} + \bar{y}z$ (B) $w\bar{x} + w\bar{y} + \bar{x}\bar{y} + \bar{w}z$
(C) $\bar{x}\bar{y} + \bar{w}z + w\bar{z} + \bar{y}z$ (D) $w\bar{z} + \bar{x}\bar{y} + w\bar{y} + \bar{w}z$

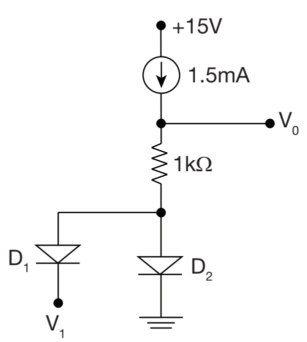
14. The input clock frequency is 10 kHz, then the frequency of Y is (initially $Q = 0$)



(A) 5 kHz (B) 10 kHz
(C) 2.5 kHz (D) 0 Hz

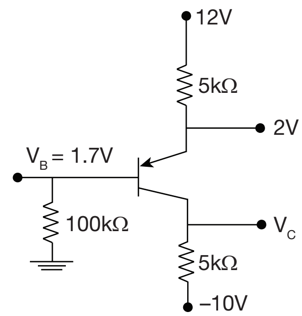
15. If $(3.5)_{\text{base 6}} + (2.3)_{\text{base 6}} = (X)_{\text{base 6}}$ then the value of X is
(A) 5.8 (B) 10.2
(C) 6.2 (D) 5.6

16.



Consider diodes are ideal, If $V_1 = -2V$, find the value of V_o.
(A) – 3.5V (B) 0.75V
(C) – 0.5V (D) 2.8V

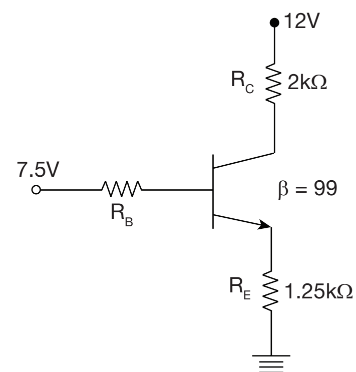
17.



Find the voltage across capacitor V_C.
(A) –0.023 V (B) 9.91 V
(C) 19.915 V (D) –0.085 V

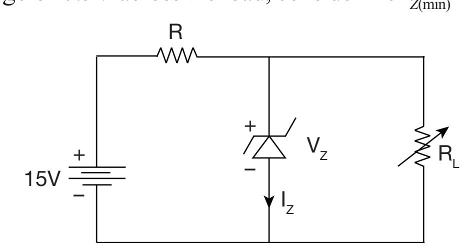
18. The data sheet for an E-MOSFET gives $I_{D(on)}$ = 4mA at V_{GS} = 10V and $V_{GS(th)}$ = 2V. Then find the value of K.
(A) 62.5 μA/V² (B) 54.75 μA/V²
(C) 6.25 mA/V² (D) 5.47 mA/V²

19. For the transistor circuit shown in figure I_B = 35 μA and V_{BE} = 0.7V



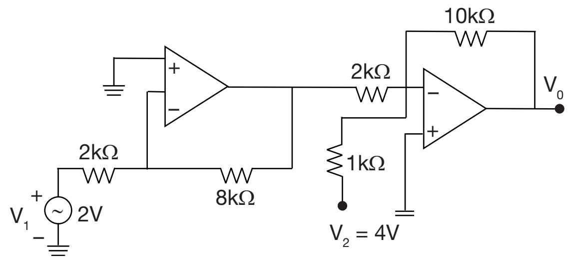
The value of R_B would be
(A) 55 kΩ (B) 5.23 kΩ
(C) 69.28 kΩ (D) 7.28 kΩ

20. A 7.5V zener diode is used in the circuit shown in figure, and the load current is to vary from 15 to 80mA. Find the value of series resistance 'R' to maintain a voltage of 7.5V across the load, consider the $I_{Z(min)}$ = 8mA.



(A) 85.22Ω (B) 8.27kΩ
(C) 4.25kΩ (D) 98.24Ω

21.



The resulting output V_0 is

(A) zero (B) –40 V
(C) –10 V (D) –8 V

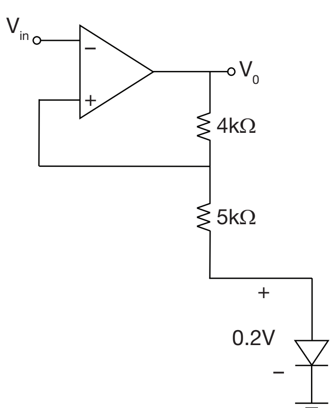
22. The tuned collector oscillator circuit used in the local oscillator of a radio receiver makes use of an *LC* tuned circuit with L_1 = 50μH, and C_1 = 250pF. Then the frequency of oscillators is

(A) 14.23 KHz (B) 1.423 MHz
(C) 284 MHz (D) 1.5 MHz

23. In a current amplifier, with A = 1000 and β = 0.25, the input resistance is 100Ω before negative feedback is applied. After negative feedback is applied it's input resistance will be

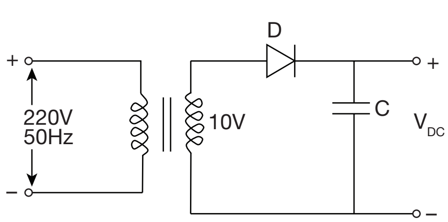
(A) 0.4Ω (B) 251Ω
(C) 150Ω (D) 100Ω

24. The Schmitt trigger circuit is shown in the below figure. If V_{sat} = ±12V, the upper threshold voltage would be



(A) 1.38 V (B) 1.02 V
(C) 13.8 V (D) –15 V

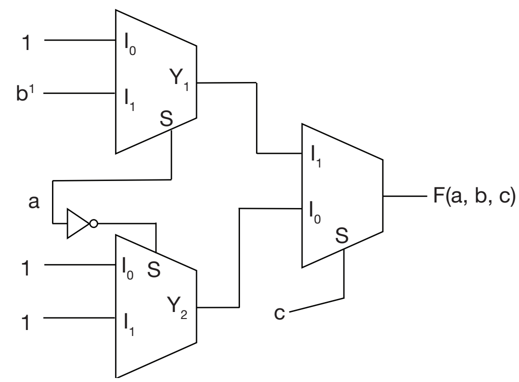
25. In the rectifier circuit shown in figure. The minimum peak – inverse – voltage (PIV) rating of the diode is



Consider diode D is ideal.

(A) 10 V (B) $20\sqrt{2}$ V
(C) $10\sqrt{2}$ V (D) 20 V

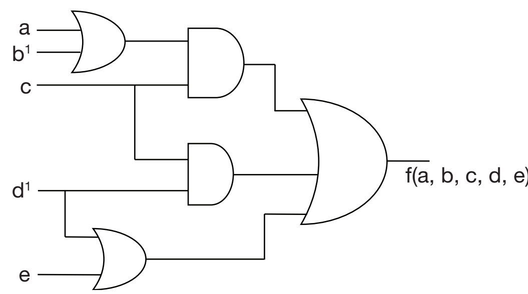
26.



The Function $F(a, b, c)$ is

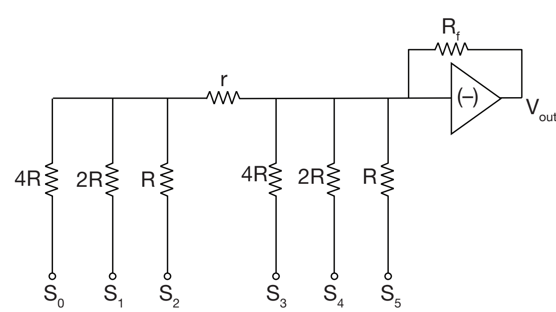
(A) $a^1 + b^1 + c$ (B) $(abc)^1$
(C) $(a^1 + b^1)c^1$ (D) $(a + b)^1 + c^1$

27. If the following circuit is converted to all-NAND network, then how many number of NAND gates are required? (inverted inputs are available)



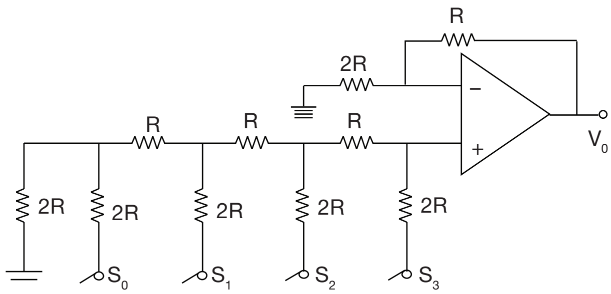
(A) 3 (B) 4
(C) 5 (D) 6

28. A 3 bit Digital to Analog converter is modified as follows, to make it 6 bit Digital to analog converter. So what will be the value of resistor '*r*' for proper operation?



(A) 16 R (B) 8 R
(C) 4 R (D) 2 R

29. The switches S_i will be connected to V_R = 1V for logic 1, and will be connected to 0V for logic 0. Find the output V_o for input $S_3S_2S_1S_0$ = 0101



(A) 0.468 V (B) 5 V
(C) 7.5 V (D) 0.3125 V

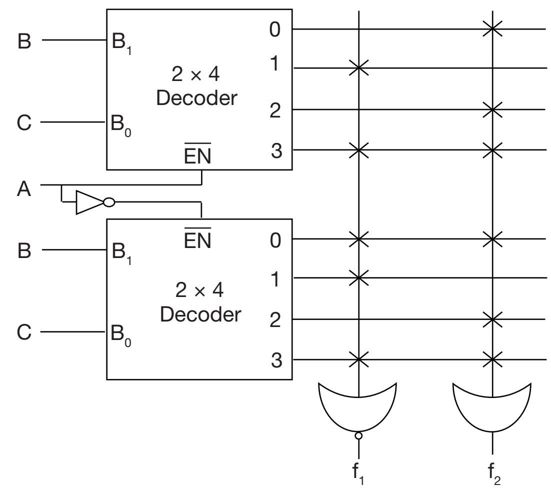
30. A 2048 × 8 bit memory element is interfaced with 8085 microprocessor, if the address of first memory location in the RAM is 0900H. Then the address of the last memory location will be?
(A) 1000H (B) 0FFFH
(C) 27FFH (D) 10FFH

31. The voltage and current parameters of ECL logic family are given by
$V_{OH} = -0.76$ V, $V_{IH} = -1.1$V,
$V_{OL} = -1.58$V, $V_{IL} = -1.25$ V
$I_{OH} = 3$mA, $I_{IH} = 107\mu$A, $I_{OL} = 3.7$ mA, $I_{IL} = 137\mu$A
The fan out, noise margin of the logic family are?
(A) 28, 0.34 V (B) 27, 0.34 V
(C) 28, 0.33 V (D) 27, 0.33 V

32. 4000: L X I SP, 5000 H
4003: L X I H, 5050 H
4006: SPHL
4007: PUSH H
4008: PUSH B
4009: CALL 4050H
400C: POP D
400D: HLT
at the end of this program, contents of *SP* and *PC* are
(A) 4FFEH, 400DH (B) 5048H, 400EH
(C) 504EH, 400EH (D) 5052H, 400EH

33.
```
         MVI   A, Byte1
         ORA   A
         JM    Output
         XRA   A
Output:  OUT   Port
         HLT
```
The program will give output,
(A) negative numbers
(B) positive numbers
(C) odd numbers
(D) negative numbers or zero

Common Data for Questions 34 and 35:



34. The function $f_1(A, B, C)$ in SOP form is
(A) $\overline{A}B + B\overline{C}$ (B) $\overline{A}\,\overline{C} + B\overline{C}$
(C) $\overline{A}B + A\overline{C}$ (D) $\overline{A}C + B\overline{C}$

35. The function $f_2(A, B, C)$ in POS form is
(A) $\overline{B} + A$ (B) $\overline{A} + C$
(C) $B + \overline{C}$ (D) $A + \overline{C}$

Answer Keys

1. C	**2.** C	**3.** A	**4.** D	**5.** D	**6.** C	**7.** B	**8.** A	**9.** C	**10.** B
11. B	**12.** D	**13.** A	**14.** B	**15.** B	**16.** C	**17.** D	**18.** A	**19.** C	**20.** A
21. A	**22.** B	**23.** A	**24.** A	**25.** B	**26.** B	**27.** A	**28.** C	**29.** A	**30.** D
31. D	**32.** C	**33.** D	**34.** B	**35.** C					

Hints and Explanations

1. For *CC* amplifier
R_{in} = high
R_o = low Choice (C)

2. Choice (C)

3. We know that flat band voltage $V = \frac{q}{C}(1 - W_c)$ volts
$= \frac{2\times10^{-4}}{250\times10^{-6}}(1+0.75) = 1.4$ volts Choice (A)

4. $I_E = \frac{15\text{-}2.5}{2.5\text{k}\Omega} = 5\text{mA}$

$I_B = \frac{2}{100}\text{mA} = 20\mu\text{A}$

$(1+\beta) = \frac{I_E}{I_B} = 250$

$\therefore \beta = 249$ Choice (D)

5. Applying *KVL* to the input loop

$1.2 - I_B R_B - V_{BE} - R_E . I_E = 0$

$1.2 - 0.7 = I_B[10 \times 10^3 + 0.5 \times 10^3 \times 151]$

$I_B = 5.8479\mu A$

$I_C = \beta . I_B$

$= 150 \times 5.8479\mu A$

$= 0.877mA$ Choice (D)

6. For *D*, *C* analysis R_E advantage it improves the stability. But *A*. *C* analysis R_E decrease the gain.

$\therefore$ Capacitor across R_E it eliminates the R_E effect

$\therefore$ Short circuit parallel to R_E Choice (C)

7. (1) Cascode amplifier (*CE – CB)* gives the high input impedance

(2) It is providing high frequency performance of *CB*

(3) It is also used as wide band amplifier Choice (B)

8. From the given circuit

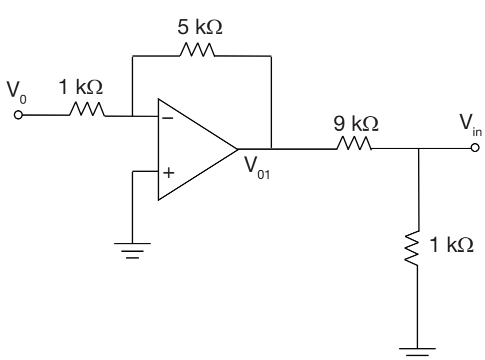
$$I_C = \frac{2}{500} = 4 \text{ mA}$$

$$I_B = \frac{4.5-2}{15} \text{ mA} = 0.1666 \text{ mA}$$

$$I_C = \beta\, I_B$$

$$\beta = \frac{I_C}{I_B} = 24$$ Choice (A)

9. Applying virtual GND concept and redrawing the given circuit.



$$V_{01} = \frac{-R_f}{R_1} . V_0$$

$$V_{01} = -5V_0$$

$$V_{in} = \frac{1K}{10K} \times V_{01}$$

$$V_{in} = \frac{-1}{2} V_0$$

$$\frac{V_0}{V_{in}} = -2$$ Choice (C)

10. Audio frequency oscillators (<20 KHz)

(1) *RC* – phase shift

(2) Wein bridge

RF oscillators (> 20 KHz)

(1) Colpitt's oscillator

(2) Crystal oscillator

(3) Hartly oscillator

(4) Clapp oscillator

......……….etc Choice (B)

11. From given $a = (b + c)(b^1 + c^1)$

$= bc^1 + b^1 c = b \oplus c$

EXOR with c both sides

$a \oplus c = b \oplus c \oplus c = b \oplus 0 = b$

So $b = a \oplus c = a^1 c + ac^1$ or $(a + c)(a^1 + c^1)$.

Choice (B)

12. Even function is a Boolean function, and it will be equal to 1, if the input variables have an even number of 0's.

(odd function is a Boolean function for which output is 1, for input combinations with odd number of 1's)

So for 4 variables, even number of zeroes occur for input combinations

0000, 0011, 0101, 0110, 1001, 1010, 1100, 1111

For these combinations, even function output is 1.

So remaining terms are max terms.

So $f_{even} = \Pi M(1, 2, 4, 7, 8, 11, 13, 14)$ Choice (D)

13.

wx \ yz	00	01	11	10
00	1	X	1	
01		1	1	X
11	1	1		X
10	1	1	X	1

$\bar{x}\,\bar{y}, \bar{w}z$ is the essential prime implicants, remaining prime implicants can be used to cover all the min terms.

wx \ yz	00	01	11	10
00	1	X	1	
01		1	1	X
11	1	1		X
10	1	1	X	1

$\bar{w}z, \bar{x}\bar{y}, w\bar{x}, \bar{y}z$ will not implement the *k*-map as in the above *k*-map min term $wxyz = 1100$ is not covered.

Choice (A)

14. When $Q = 0$, initially, $\bar{Q} = 1$

So $J = K = 1$, by applying first clk pulse $Q_{n+1} = 1$, Then $\bar{Q}_{n+1} = 0$. So $J = 1$, $K = 0$, after clock pulse $Q_{n+2} = 1$, …

and for next clock pulses it will remain in same state, so the frequency of $Q = 0$Hz ($Q = 1$ always) but $Q = 1$, so the clk pulse ANDed with $Q = 1$ and Y is same as clk pulse so frequency of Y is 10 kHz. Choice (B)

15. 3.5
+ 2.3
?
5 + 3 = 8
$(12)_6$ so result is 2 and carry is 1.

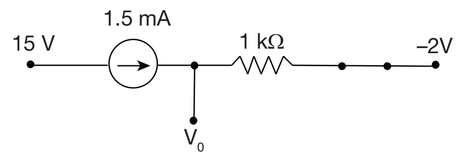
$$\begin{array}{r} 1 \\ 3.5 \\ +2.3 \\ \hline ?.2 \end{array}$$

1 + 3 + 2 = 6
$(10)_6$ so result is 0 and carry is 1

$$\begin{array}{r} 3.5 \\ +2.3 \\ \hline 10.2 \end{array}$$

Choice (B)

16. From the given circuit
$D_1 \rightarrow$ ON, $D_2 \rightarrow$ OFF
∴ It becomes



$V_o = 1.5 - 2$
$= -0.5$ volts Choice (C)

17. We know $I_E = I_B + I_C$

$$I_E = \frac{12-2}{5}\text{mA} = 2\text{mA}$$

$$I_B = \frac{1.7}{100}\text{mA} = 0.017\text{mA}$$

$I_C = 1.983$mA

$$I_C = \frac{V_C + 10}{5}\text{mA}$$

$V_C + 10 = 1.983 \times 5$
$V_C = 9.915 - 10 = -0.085$ volts. Choice (D)

18. $I_D = k[V_{GS} - V_{GS(\text{th})}]^2$ Amp

$$K = \frac{I_{D(on)}}{\left[V_{GS(on)} - \text{V}_{\text{GS(th)}}\right]^2}$$

$$= \frac{4\times10^{-3}}{[10-2]^2} = 62.5\times10^{-6}\ \frac{A}{V^2}$$

Choice (A)

19. Applying KVL to input loop
$7.5 - R_B.I_B - V_{BE} - R_E.I_E = 0$
$I_E = (1 + \beta).I_B$
$= 100 \times 35 \times 10^{-6}$
$= 3.5$ mA
$7.5 - 0.7 - 4.375 = R_B.I_B$

$$R_B = \frac{2.425}{35}\times10^6 = 69.28\text{k}\Omega$$

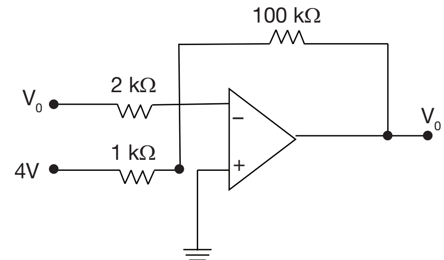
Choice (C)]

20. $I = I_Z + I_L$
$I_{R(\max)} = I_{Z(\min)} + I_{L(\max)} = (8 + 80)$ mA $= 88$ mA

$$R = \frac{15-7.5}{88}\text{k}\Omega = 85.22\Omega$$

Choice (A)

21.



The o/p voltage of 1st stage is V_{01}

$$V_{01} = \frac{-8}{2}\times2 = -8\text{volts}$$

Redrawing the given circuit
$V_0 = -5 \times (-8) - 10 \times 4$
$= 40 - 40 = 0$V Choice (A)

22. Frequency of oscillation, $f = \dfrac{1}{2\pi\sqrt{L_1C_1}}$

$$f = \frac{1}{2\pi\sqrt{50\times10^{-6}\times250\times10^{-12}}} = \frac{1\times10^{+8}}{2\pi\sqrt{125}}$$

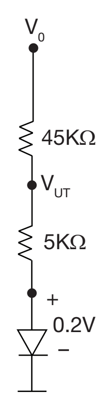
$= 1.426$ MHz Choice (B)

23. From the given data
$A = 1000$; $\beta = 0.25$
$R_i = 80\Omega$
$1 + A\beta = 1 + 1000 \times 0.25 = 251$
Current amplifier
$i/p \Rightarrow$ current source
$o/p \Rightarrow$ current source
i.e, it is a current shunt amplifier
∴ $R_i \Rightarrow$ decreases
$R_0 \Rightarrow$ increases

$$\therefore\ R_{\text{if}} = \frac{R_i}{1 + A\beta} = \frac{100}{251} \approx 0.4\Omega$$

Choice (A)

24. Max. output $V_0 = \pm V_{\text{sat}} = \pm12$V
If $V_{in} = V_{UT}$, redrawing the given circuit.
$V_+ = V_- = V_{UT}$



Applying nodal analysis at node V_{UT}

$$\frac{V_{UT}-V_0}{45K}+\frac{V_{UT}-0.2}{5K}=0$$

$V_{UT} - V_0 + 9V_{UT} - 1.8 = 0$

$10V_{UT} = V_0 + 1.8$

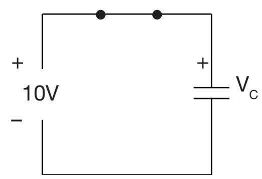
But $V_0 = +V_{sat} = +12V$

$V_{UT} = 1.38$ Volts Choicer (A)

25. During $+Ve$ half cycle

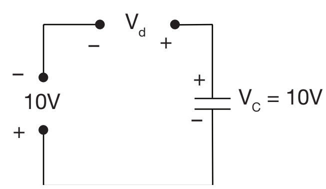
$D \rightarrow$ ON

$\therefore$ Voltage across capacitor $V_C = 10V_{rms}$.



$\therefore$ $V_C = 10V_{rms}$.

During $-Ve$ half cycle $D \rightarrow$ OFF



PIV = $V_d = (10 + 10)V_{rms} = 20\sqrt{2}$ volts. Choice (B)

26. Output of 1[st] MUX $Y_1 = 1.a^1 + b^1.a = a^1 + b^1$

Output of 2[nd] MUX $Y_2 = 1.a + 1.a^1 = 1$

Output of 3[rd] MUX $F(a, b, c) = Y_1.c + Y_2.c^1$

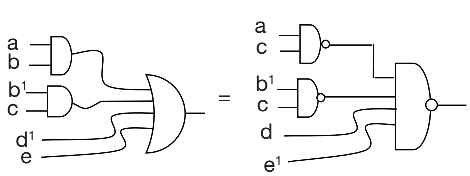
$= (a^1 + b^1)c + 1.c^1$

$= a^1 + b^1 + c1$ Choice (B)

27. Given function has to be in SOP form, so it can be implemented by AND-OR gates, same as NAND-NAND gates

$f(a, b, c, d, e) = (a + b^1)c + cd^1 + (d^1 + e)$

$= ac + b^1 c + cd^1 + d^1 + e$



$= ac + b^1 c + d^1 + e$ Choice (A)

28. The S_2 S_1 S_0 are lower order bits, S_5 S_4 S_3 are higher order bits so the current due to bits S_2 S_1 S_0 should be one-eighth of the current due to S_5 S_4 S_3.

The resistor r has been inserted to provide the attenuation.

Such attenuation, is possible when $r = 4R$. Choice (C)

29. Given circuit is a DAC. ($R - 2R$ type)

So the voltage at non inverting terminal is

$$V_+ = \frac{V_R}{2^n}\ (S_0 \times 2^0 + S_1 \times 2^1 + S_2 \times 2^2 + S_3 \times 2^3)$$

$$= \frac{1}{16}\times(1+0+4+0) = \frac{5}{16}$$

$$V_0 = \left(1+\frac{R}{2R}\right)\frac{5}{16} = \frac{3}{2}\times\frac{5}{16} = \frac{1}{2}\times\frac{15}{16}$$

$= 0.46875$ V Choice (A)

30. Address of last memory location – Address of first Memory location

= (Number of address locations – 1)

Here given RAM number of address locations = 2048

$(2048)_{10}$ = 0800H

0800H – 1 = 07FFH

X – 0900H = 07FFH

X = 07FF + 0900H = 10FFH Choice (D)

31. **Noise Margin**

$\Delta 1 = -0.76 - (-1.1) = 0.34V$

$\Delta 0 = -1.25 - (-1.58) = 0.33V$

Noise margin is min ($\Delta 0$, $\Delta 1$) = 0.33V.

Fanout:- $N_1 = \frac{I_{OH}}{I_{IH}} = \frac{3mA}{107\mu A} = 28$

$$N_0 = \frac{I_{OL}}{I_{IL}} = \frac{3.7mA}{137\mu A} = 27$$

Fanont = min (N_1, N_0) = 27 Choice (D)

32. As the above programs ends at memory location 400DH, the address of next memory location is 400EH, which will be stored in Program Counter at the end of the program.

L X I SP, 5000H $\rightarrow$ load SP = 5000H

L X I H, 5050H $\rightarrow$ load HL = 5050H

SPHL $\rightarrow$ move HL to SP, so SP = 5050H

PUSH H $\rightarrow$ SP decremented by 2 (SP – 2)

PUSH B $\rightarrow$ SP decremented by 2 (SP – 4)

CALL 4050H $\rightarrow$ after call instruction, again returned to next instruction, so no charge for SP.

POP H $\rightarrow$ increment SP by 2 (SP – 4 + 2) = SP – 2

HLT – stop

So contents of stack pointer are 5050–2 = 504EH.

Choice (C)

33. MVI A, Byte1 $\rightarrow$ A = Byte1, copy number to A.

ORA A – make A + A = A, contents of Accumulator remain same but CY = 0, and other flags will change as per number in Accumulator.

JM output – Jump on minus to output port if S = 1 go to output.

XRA A – else XOR A with A, A $\oplus$ A = 00H

A = 00H

OUT port $\rightarrow$ send the contents of Acc to output port

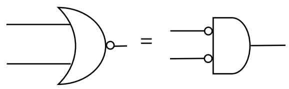
HLT – stop.

So if there is any negative number it will be the output or zero is the output. Choice (D)

34. Given is a 3 × 8 Decoder with two 2 × 4 Decoders, and a NOT gate, LSB are connected to inputs of Decoder

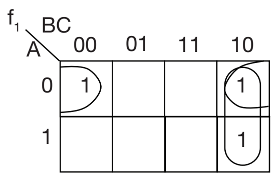
(B_1 B_0 = BC), MSB (A) is connected to check which decoder has to be selected by using enable input, When A = 0, first Decoder will be selected, when A = 1, second decoder will be selected.

f_1 is connected through NOR gate



outputs of Decoder (here active High outputs) are min terms, min terms connected to NOR gate.

$f_1 = \pi M(1, 3, 4, 5, 7) = \Sigma m(0, 2, 6)$ because in second decoder A = 1, BC vary as per inputs applied so 4, 5, 6, 7 are output of second decoder (min terms)



$f_1 = \overline{A}\overline{C} + B\overline{C}$

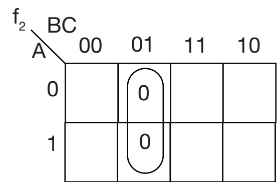
$$f_1 = \overline{A}\,\overline{C} + B\overline{C}$$

Choice (B)

35. f_2 is connected to OR gate, so sum of min terms

$f_2 = \Sigma m(0, 2, 3, 4, 6, 7) = \pi M(1, 5)$

$$f_2 = \left(B + \overline{C}\right)$$



$f_2 = (B + \overline{C})$

Choice (C)