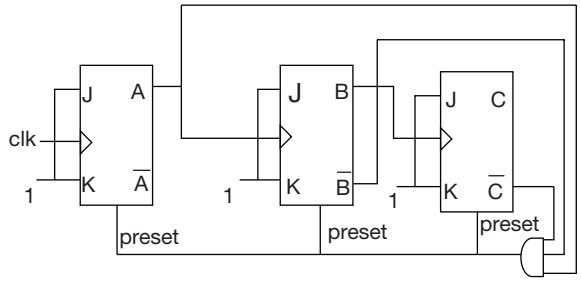
DIGITAL CIRCUITS TEST 4

Number of Questions: 25 **Time: 60 min.**

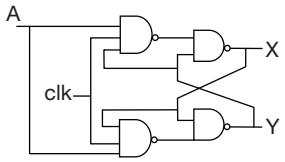
Directions for questions 1 to 25: Select the correct alternative from the given choices.

1. The ripple counter shown in figure works as a



(A) Mod-6 up counter (B) Mod-5 up counter
(C) Mod-5 Down counter (D) Mod-6 Down counter

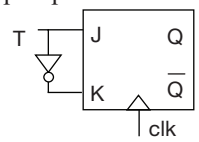
2. Consider the given circuit

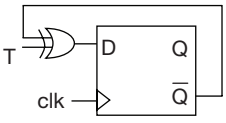


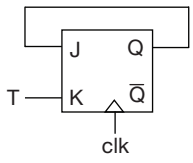
In this circuit, the race around condition
(A) does not occur
(B) occurs when clk = 0
(C) occurs when clk = 0, $A = 1$ and $X = Y = 1$
(D) occurs when clk = 1, $A = 1$

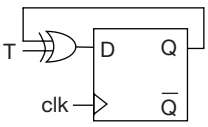
3. Three, modulo-4 counters are cascaded together then the resultant counter modulus is
(A) 3×4 (B) 3^4
(C) $4 \times 4 \times 4$ (D) $3 + 4$

4. Which of the following flipflop configuration works as *T* flip flop?

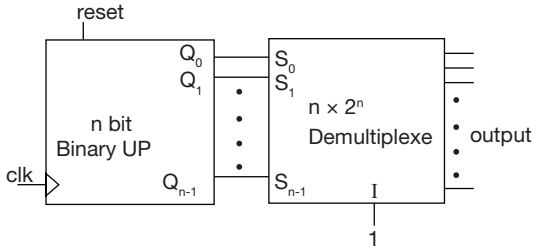
(A)


(B)


(C)


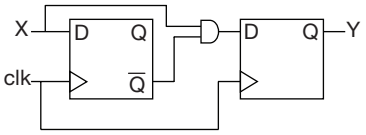
(D)


5. '*n*' bit Binary *UP* counter is connected to $n \times 2^n$ Demultiplxer with input $I = 1$, as shown in the figure.

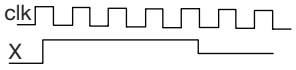


If the counter starts from reset, the above configuration works as
(A) Modulo – 2^n twisted ring counter
(B) Modulo – *n* ring counter
(C) Modulo – 2*n* Johnson counter
(D) Modulo – 2^n ring counter

6. Consider the following circuit with initial state $Q_o = Q_1 = 0$. The *D* flipflops are positive edge triggered.

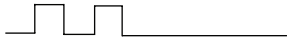


Consider the following timing diagrams of *X* and clk. Which one is the correct wave form of *Y*?



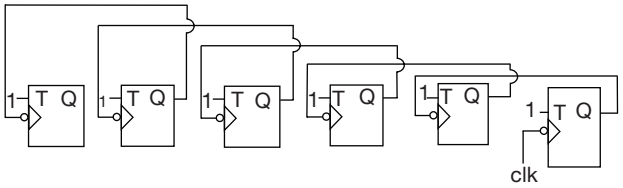
(A)


(B)


(C)


(D)

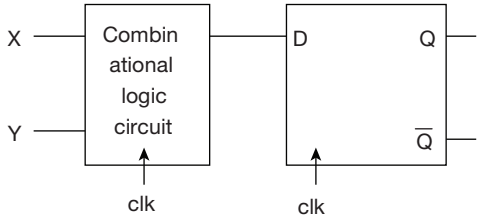

7. Six *JK* Flip flops are cascaded to form the circuit shown in figure. Clock pulses at a frequency of 128 kHz are applied as shown, The frequency (in kHz) of the wave form at Q_4 is _____.



(A) 32 kHz (B) 16 kHz
(C) 8 kHz (D) 4 kHz

8. The following truth table has to be realized with *D* flip flop.

X Y	Q_{n+1}
0 0	Q_n
0 1	1
1 0	0
1 1	$\overline{Q_n}$

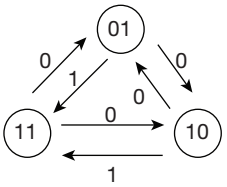


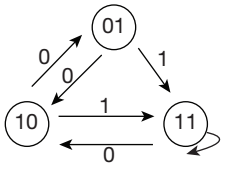
Then what is the equation of combinational logic circuit output in terms of X, Y and Q_n?

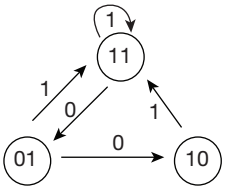
(A) $D = \overline{X}\, Q_n + Y\overline{Q_n}$ (B) $D = X\overline{Q_n} + \overline{Y}Q_n$

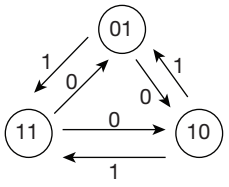
(C) $D = XY \sum Q_n$ (D) $D = (X + Y) \sum Q_n$

9. A clocked sequential circuit has 3 states A, B, C and 1 input X. As long as input $X = 0$, the circuit alternates between states A and B, if input $X = 1$(either in state A or B), The circuit goes to state C and remain in state C as long as $X = 1$, from state C, circuit returns to state A when input $X = 0$, and then a repeats its behavior. Assume $A = 01$, $B = 10$, $C = 11$ the state diagram will be?

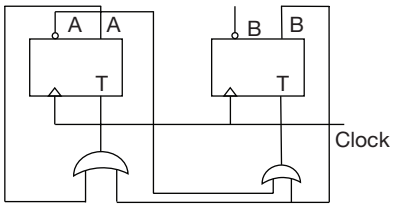
(A) 

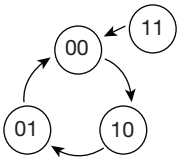
(B) 

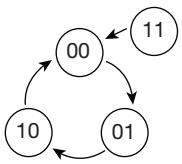
(C) 

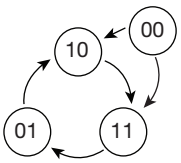
(D) 

10. Find the state (AB) diagram for the following sequential circuit?



(A) 

(B) 

(C) 

(D) None of these

11. The following program is intended to clear memory locations starting from memory address 0000H. How many memory locations will be cleared? ($A = 01$H)

	LXI	H, 0010H
	ORA	A
loop:	MVI	M,00H
	DCX	H
	JNZ	loop
	HLT	

(A) 10

(B) 9

(C) 16

(D) a large memory block will be erased

12. The following program reads one data byte (X) at a time from input port1.

IN	PORT1
MVI	B, 20H
CMP	B
JC	REJECT
JM	REJECT
STA	3010H
JMP	ACCEPT
REJECT:	JMP INVALID

Indentify the range of number is Decimal that will transfer the program to location INVALID.

(A) $20H < X < A0H$

(B) $X < 20H$ and $X > A0H$

(C) $X < 32$ and $X > 160$

(D) $32 < X < 160$

13. At the end of the following program

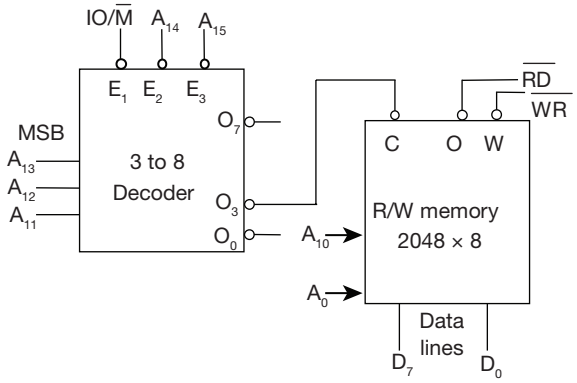
LXI	SP, 31AE H
MOV	C, 00H
PUSH	B
POP	PSW
RET	

(A) The contents of Accumulator has been reset

(B) All the flags has been reset

(C) The contents of Accumulator and Register B has been swapped.

(D) Program status word is loaded on stack.

14. 

A R/W memory is interfaced with 8085 microprocessor as shown. What is the range of memory map connected to O_3 line.

(A) 6800 – 6FFFH (B) 9000 – 98FFH

(C) 9800 – 9FFFH (D) 2300 – 2FFFH

15. If we use all output lines ($O_7 - O_0$) of the above decoder circuit to select eight memory chips of the same size (2048 × 8). What is the total range of the memory map?

(A) 8000 – BFFFH (B) 9000 – CFFFH

(C) 7000 – AFFFH (D) 0800 – ABFFH

16. The following program get a data byte Byte 1 to Accumulator, then the output at PORT address 01H is?

```
MVI        A, Byte 1
ORA        A
JM         OUTPUT
OUT        01H
HLT
OUTPUT:    CMA
           ADI 01H
           OUT 01H
           HLT
```

(A) positive numbers except 00H, 01H
(B) negative numbers
(C) negative numbers except 00H, 01H
(D) positive numbers and negative numbers 2's complement

17. Which one of the following is not true during the execution of an interrupt service routine, which does not contain any EI instruction?
(A) The µ*P* can be interrupted by a non maskable interrupt
(B) The µ*P* cannot be interrupted by any interrupt
(C) The µ*P* cannot be interrupted by a maskable interrupt
(D) All interrupts except the non maskable interrupt are disable.

18. Match with the semiconductor technology used for fabrication

List-I	List-II
P. dynamic RAM	1. bipolar technology
Q. static RAM	2. MOS technology
R. EPROM	3. either bipolar or MOS technology

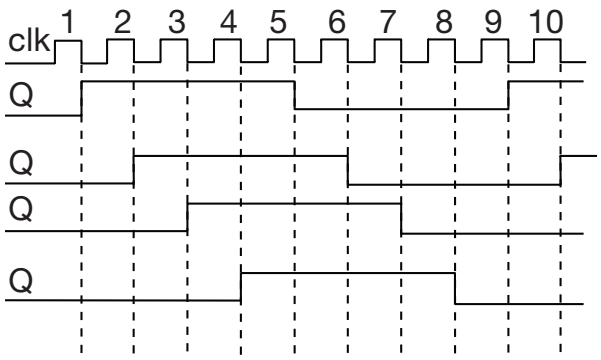
(A) $P-2, Q-1, R-2$ (B) $P-1, Q-2, R-3$
(C) $P-2, Q-3, R-2$ (D) $P-2, Q-1, R-3$

19. The resolution of a *D*/*A* converter is approximately 0.4 percent of its full scale range. It is
(A) an 8 bit converter (B) a 10 bit converter
(C) a 12 bit converter (D) a 16 bit converter

20. For a 12 bit *A*/*D* converter the range of input signal is 0 to +10V. The voltage corresponding to 1 *LSB* will be
(A) 0 (B) 0.0012V
(C) 0.0024V (D) 0.833V

21. *A D*/*A* converter has 5 V full scale output voltage and an accuracy of + 0.2%, the maximum error for any output voltage will be
(A) 5 mV (B) 10 mV
(C) 20 mV (D) 30 mV

22. The waveforms of a counter are shown below, this is a

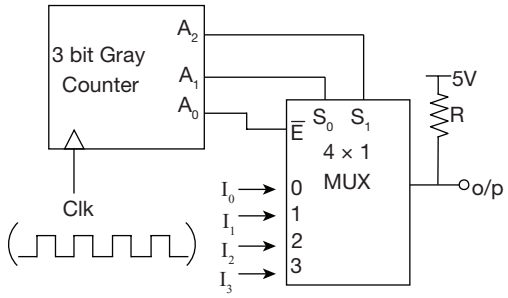


(A) synchronous BCD counter
(B) ripple counter
(C) ring counter
(D) twisted ring counter

23. Symmetrical square wave of time period 200 µs can be obtained from square wave of time period of 20 µs by using a
(A) 4-bit binary counter
(B) divide by 5 counter
(C) *BCD* counter
(D) divide by 5 counter followed by a divide by 2 counter

24. The outputs Q and $\overline{Q}$ of a master slave *SR* flipflop are connected to its *R* and *S* inputs respectively. What happens to output Q when clock pulses are applied.
(A) permanently 0
(B) permanently 1
(C) fixed 0 or 1
(D) complementing with every clock pulse

25. A 3 bit gray counter is used to control the output of the multiplexer as shown in figure, the initial state of the counter is 000. The output is pulled high, the output of the circuit follows the sequence



(A) $1, I_0, I_1, 1, 1, I_3, I_2, 1, 1$
(B) $I_0, 1, 1, I_1, I_3, 1, 1, I_2, I_0$
(C) $I_0, 1, I_1, 1, I_2, 1, I_3, 1, I_0,$
(D) $1, I_0, 1, I_1, I_2, 1, I_3, 1, I$

Answer Keys

1. D	**2.** D	**3.** C	**4.** D	**5.** D	**6.** A	**7.** D	**8.** A	**9.** C	**10.** B
11. D	**12.** C	**13.** B	**14.** C	**15.** A	**16.** D	**17.** B	**18.** C	**19.** A	**20.** C
21. B	**22.** D	**23.** D	**24.** D	**25.** B					

Hints and Explanations

1. All flipflops have $J = K = 1$, so all are toggle switches
The output of flipflop is connected to rising edge clk input of next flip flop, so Down counter. clk input is given to flip flop A. (*LSB*).
Preset is active high, so as preset = 1, all flip flops get 111, so AND gate $o/p = 1$, when $A = 1$, $B = 0$, $C = 0$ as A, $\overline{B}$, $\overline{C}$ are inputs, so the CBA = 001, modulus = 111 – 001 = 6. Choice (D)

2. The given circuit is T latch, The input A is connected to first two NAND gates (J, K inputs connected together to make T latch)
So race around condition occurs when $A = 1$, clk = 1.
Choice (D)

3. When two counters are connected in cascade, the resultant modulus is the multiplication of the individual modulus.
So 3 counters are connected so resultant modulus = 4 × 4 × 4 = 64. Choice (C)

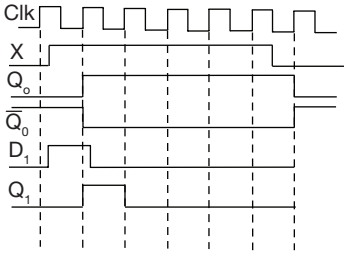
4. JK flip flop works as T flip flop if $J = K = T$
For D flip flop $Q_{n+1} = D$, $Q_{n+1} = T \oplus Q_n$(T flip flop)
So by taking $D = T \oplus Q_n$ we get T flip flop.
Choice (D)

5. n bit binary UP counter counts in Binary sequence, so same binary sequence is applied to Demultiplexer, so input $I = 1$, will be at output in sequence, for 3 bit example.

$Q_2\ Q_1\ Q_0$	$S_2\ S_1\ S_0$	$Y_0\ Y_1\ Y_2 \ldots . Y_7$
0 0 0	0 0 0	1 0 0 0
0 0 1	0 0 1	0 1 0 0
0 1 0	0 1 0	0 0 1 0

It works like a module 2^n ring counter. Choice (D)

6. For D flip flop whatever input we apply, same output we get after clk pulse



Choice (A)

7. The frequency of $Q_o = \dfrac{fclk}{2}$

Frequency of $Q_1 = \dfrac{fclk/2}{2} = \dfrac{fclk}{4}$

Frequency of $Q_2 = \dfrac{fclk/4}{2} = \dfrac{fclk}{8}$

Frequency of $Q_3 = \dfrac{fclk}{16}$

Frequency of $Q_4 = \dfrac{fclk}{32} = \dfrac{128}{32} = 4\,\text{kHz}$

Frequency of $Q_5 = \dfrac{fclk}{64}$ Choice (D)

8. The given XY flip flop truth table is

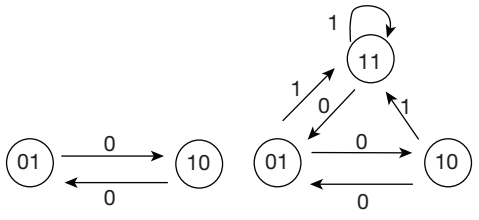
X	Y	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

X \ Y Q	00	01	11	10
0		1	1	1
1				1

$Q_{n+1} = \overline{X}\,Q_n + Y\overline{Q_n}$

The characteristic equation of D flip flop is $Q_{n+1} = D$, This has to work like above XY flip flop. By equating
$Q_{n+1} = D = \overline{X}\,Q_n + Y\overline{Q}_n$ Choice (A)

9. $A = 01$, $B = 10$, alternate states when $X = 0$



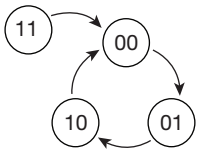
When $X = 1$, A, B go to state $C = 11$ as long as $X = 1$, C will remain in same state

When $X = 0$, C will return to state $A = 01$

Choice (C)

10. Let us consider states as AB if initially state of the circuit is 00 (reset)

Clk	A B	T_A	T_B	
		$(A + B)$	$(A^1 + B)$	
0 1 2 3	0 0 0 1 1 0 0 0	0 1 1	1 1 0	If initially at 00 state, after 3 Clk pulses it comes back to same state 00.
0 1	1 1 0 0	1	1	If initial state is 11, it goes to 00 state after clock pulse



Choice (B)

11. *LXI H*, 0010 H → Load $HL = 0010$
ORA A → *OR* Accumulator with itself
$A = A + A$ → contents will be same but flags will change as per result So $Z = 0$, $(A \neq 00H)$
MVI *M*, 00H → Copy 00H to memory location *M* address specified by *HL* register pair.
DCX *H* → Decrement *HL* register pair but this instruction will not effect the flags.
JNZ loop – If No zero flag go to loop, else Halt.
but zero flag = 1 because *ORA A* instruction and this will iterate infinitely and a large memory block will be erased. Choice (D)

12. IN Port 1 – take input from port 1 to Accumulator
MVI *B*, 20 H → Copy 20H to $B = B = 20$ H
CMP *B* → compare *B* with Accumulator
This will be performed by subtraction of (Accumulator – *B*) if input byte is *X*, then as per $X - B$ the flags will be effected.
We will get a carry flag when $X - 20H < 00H$ $[CY = 1]$
We will get a sign flag when $X - 20 > 80H$ $[S = 1]$
JC REJECT – Jump on carry to REJECT location $(CY = 1)$
JM REJECT – Jump as Minus to REJECT location $(S = 1)$
So $X < 20H = (32)_D$
$X > A0H = (160)_D$ Choice (C)

13. LXI SP, 31AEH → load $SP = 31AE$, initialization of stack pointer
MOV *C*, 00H → The contents of *C* were reset $C = 00H$
PUSH *B* → The contents of *BC* register pair loaded on top of stack.
POP PSW → retrieve the top of stack (now *BC*) to program status word (Accumulator + Flag register)
So Accumulator = *B*, Flags = $C = 00H$
So contents of flag register were made reset.

Choice (B)

14. For the decoder to be enabled $E_2 = A_M = 0$, $E_3 = A_{15} = 1$, $E_1 = IO/\overline{M} = D$ for memory operation
Address range is to select O_3, $A_{13}\,A_{12}\,A_{11} - 011$

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7 ..... A_0
1	0	0	1	1	0	0	0	0.....0 → 9800*H*
1	0	0	1	1	1	1	1	1.....1 → 9*FFFH*

Choice (C)

15. Eight memory chips are used each of size 2048 × 8
⇒ 2k Bytes
So total size = $8 \times 2k = 16k$ Bytes
O_o will be selected when $A_{13}\,A_{12}\,A_{11}$ are 000 and 0_7 will be selected when $A_{13}\,A_{12}\,A_{11}$ are 111. The range can be known by the first address of memory connected to O_0 to last address of memory connected to 0_7

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7 .. A_0
1	0	0	0	0	0	0	0	0.....0 → 8000*H*
1	0	1	1	1	1	1	1	1.....1 → BFFFH

Range = 8000 – BFFFH Choice (A)

16. MVI *A*, Byte 1 – load *A* = Byte 1
ORA *A* → OR Accumulator with *A* itself
$A = A + A$ → all flags will be set as per Byte 1
JM OUTPUT → if sign = 1 (negative number) to go output else go to next instruction.
OUT 01H → Display Accumulator at port Address 01H. (positive numbers)
HLT – stop
OUTPUT: CMA – Complement Accumulator
ADI 01H → Add 01H to Accumulator
Now the contents of Accumulator are in 2's complement OUT 01H → Display Accumulator at port Address 01H. So positive numbers and 2's complement of negative numbers will be given to OUT port Address 01H. Choice (D)

17. Choice (B)

18. Choice (C)

19. Resolution = 0.4% of full scale

$$= \frac{0.4}{100} \times F.S.V = \frac{FSV}{250}$$

$$\text{Resolution} = \frac{FSV}{2^n}$$

So $2^n \approx 250$ approximately $n = 8$ Choice (A)

20. Resolution = 1

$$LSB = \frac{FSV}{2^{12}} = \frac{10}{2^{12}} = \frac{10}{4096} = 0.0024\text{V}$$

Choice (C)

21. Error = Full scale output × Accuracy

$= 5V \times \frac{0.2}{100} = 10mV$ Choice (B)

22. By observing sequence 0000 → 1000 → 1100 → 1110 → 1111 → 0111 → 0011 → 0001 → 0000

It is twisted ring counter. Choice (D)

23. As symmetrical square wave is required and time period got multiplied 10 times (i.e., frequency is divided 10 times)

But *BCD* counter will not give symmetrical square wave so divide by 5 counter followed by divide by 2 counter is correct. Choice (D)

24. Q is connected to R, $\overline{Q}$ to S input

So $Q_{n+1} = S + \overline{R}\,Q_n = \overline{Q}_n + \overline{Q}_n . Q_n$

So $Q_{n+1} = \overline{Q}_n$ so next state is complement of present state. Choice (D)

25.

$A_2 A_1 A_0$	$E S_1 S_0$	o/p
0 0 0	0 0 0	I_0
0 0 1	1 0 0	1
0 1 1	1 0 1	1
0 1 0	0 0 1	I_1
1 1 0	0 1 1	I_3
1 1 1	1 1 1	1
1 0 1	1 1 0	1
1 0 0	0 1 0	I_2
0 0 0	0 0 0	I_0

Enable is active low, when $E = 1$, the output is logic 1

When $E = 0$, output is from multiplexer.

Choice (B)