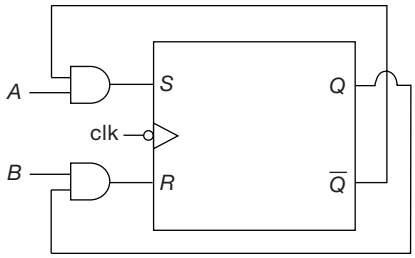
Digital Logic and Computer Organization and Architecture Test 6

Number of Questions: 35 **Section Marks: 30**

Directions for questions 1 to 35: Select the correct alternative from the given choices

1. The following flip flop is

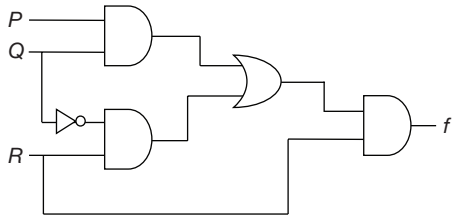


(A) D flip flop when $A = 0$
(B) D flip flop when $A = B$
(C) T flip flop when $A = 0$
(D) T flip flop when $A = B$

2. If $a \le b$, which of the following is true
(P) $a^1 + b = 1$ (Q) $a^1 \le b^1$
(R) $ab^1 = 0$
(A) P, Q (B) P, R
(C) Q, R (D) P, Q, R

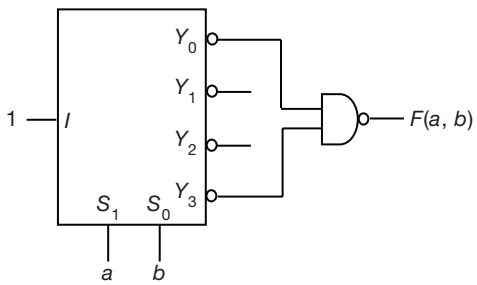
3. If $a = (b + c)(b^1 + c^1)$, then the value of b is:
(A) $(a^1 + c)(a + c^1)$ (B) $a^1c + ac^1$
(C) $a^1c^1 + a^1c$ (D) $(a^1 + c^1)(a + c^1)$

4. Calculate switching function realized by this network in minimized SOP form



(A) $PQ + \bar{Q}R$ (B) $PQR + \bar{Q}R$
(C) $PR + \bar{Q}R$ (D) $P\bar{Q} + R$

5.



In the above circuit the function $F(a, b)$ in POS form
(A) $(a + b)(a^1 + b^1)$ (B) $(a^1 + b)(a + b^1)$
(C) $(a + b^1)(a^1 + b^1)$ (D) $(a + b)(a^1 + b)$

6. A combinational circuit takes input in the range of 000 to 101, (remaining combinations are unused) The output of the circuit is 1 when ever input is a power of 2 (in decimal). Find the minimized expression for output, if x, y, z are inputs of the combinational circuit.
(A) $x^1 y \oplus z^1$ (B) $(x + y) \odot z$
(C) $x^1 y^1 \oplus z$ (D) $(x + y) \oplus z$

7. A boolean function defined as $f(a, b, c, d, e) = b + d(c + ae)$
How many number of min terms will be present for the function $f(a, b, c, d, e)$?
(A) 20 (B) 24
(C) 28 (D) 16

8. The characteristic equation of the flip-flop with functional table given below is, $(Q_{n+1}) =$

X Y	Q_{n+1}
0 0	$\overline{Q_n}$
0 1	1
1 0	0
1 1	Q_n

(A) $\bar{X}Q_n + Y\bar{Q}_n$ (B) $\bar{X}Q_n + YQ_n$
(C) $\bar{X}Q_n + \bar{Y}Q_n$ (D) $\bar{X}\bar{Q}_n + YQ_n$

9. Consider reading a block from a disk using DMA technique. Then which of the following factors will limit the rate of transfer?
(i) Limiting speed of I/O devices
(ii) Speed of bus
(iii) Too small internal buffering space
(A) (i), (ii) only (B) (ii), (iii) only
(C) (i), (iii) only (D) (i), (ii), (iii)

10. If a normal processor memory Read (RD) and write (WR) control outputs are connected to I/O interface adapters, then which type of I/O technique is used?
(A) Memory mapped
(B) Isolated I/O
(C) Both Memory mapped and Isolated I/O
(D) Interrupt-driven I/O

11. What is the signed decimal equivalent of the 2's complement number: 00001111
(A) –15 (B) –240
(C) +15 (D) +241

12. Right arithmetic shift of ones complement of –6 is (in 8-bits)
(A) 00000011 (B) 01000011
(C) 01111100 (D) 11111100

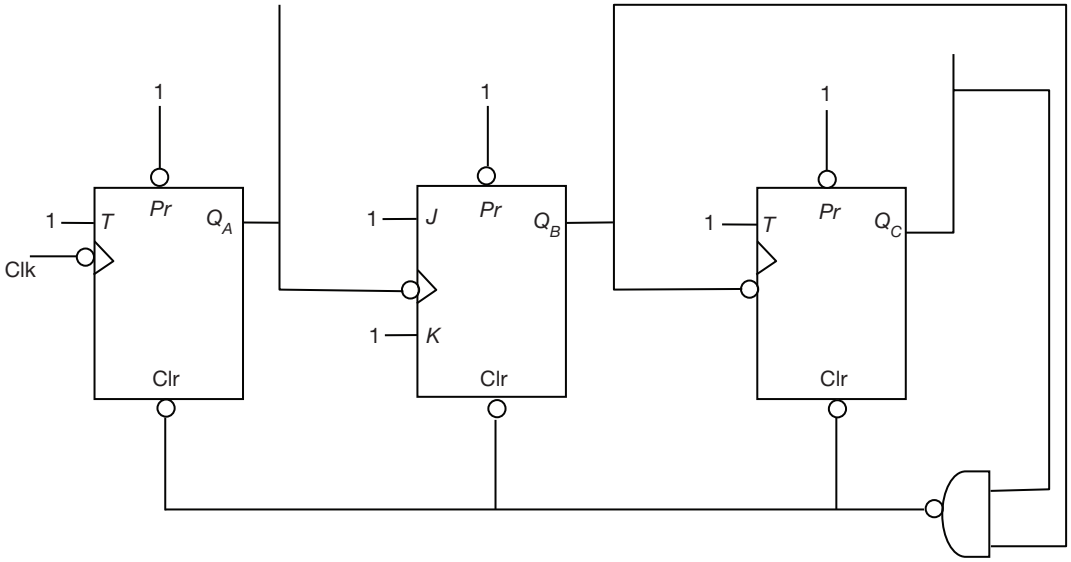
13. LRU is an effective cache replacement policy primarily because

(A) Programs exhibit locality of reference.
(B) Programs usually have small working sets.
(C) Programs read data much more frequently than write data.
(D) Program can generate addresses that collide in the cache.

14. "The purpose of cache memory is to increase the size of main memory". This statement is
(A) Always true (B) Always False
(C) Sometimes true (D) Sometimes false

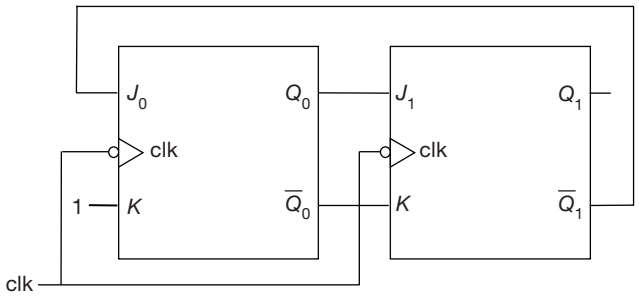
15. A memory has 2^{36} addressable locations. What is the smallest width in bits that the address can be, while still being able to address all 2^{36} locations?
(A) 36-bits (B) 72-bits
(C) 18-bits (D) 9-bits

16.



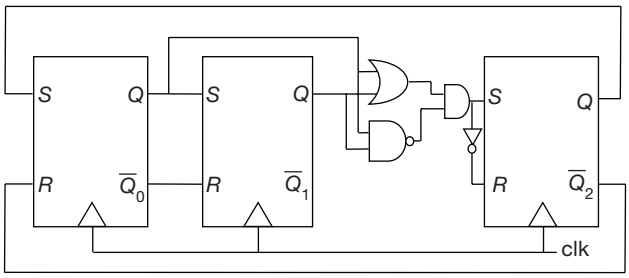
A counter formed with T, JK flip flops, as shown above, preset (Pr), clear (clr) are active low, asynchronous inputs, T, J, K are synchronous inputs. The modulus of the counter is:
(A) 4
(B) 5
(C) 6
(D) 7

17. The flip flops used in this circuit are master-slave JK flip flops. If the counter is initially at reset state after how many clock pulses it gets reset?



(A) 2 (B) 3
(C) 4 (D) 1

18. The counter shown above has initial state $Q_2\ Q_1\ Q_0 = 111(7)$, then the next states of $(Q_2\ Q_1\ Q_0)$ (in decimal) are?



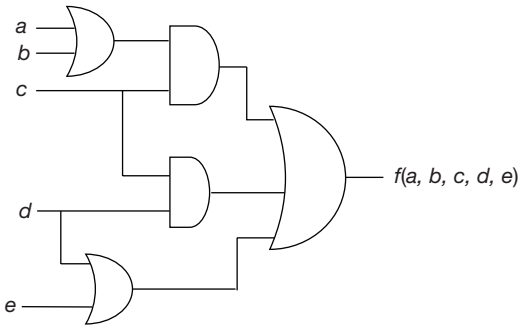
(A) 7, 6, 2, 1, 4, 3, 5 (B) 7, 3, 5, 2, 6, 1, 4
(C) 7, 3, 2, 4, 1, 6, 5 (D) 7, 5, 1, 4, 2, 3, 6

19. The max term expression of a four variable even function is?
(A) $\pi M\,(0, 2, 4, 6, 8, 10, 12, 14)$
(B) $\pi M(1, 3, 5, 7, 9, 11, 13, 15)$
(C) $\pi M\,(0, 3, 5, 6, 9, 10, 12, 15)$
(D) $\pi M\,(1, 2, 4, 7, 8, 11, 13, 14)$

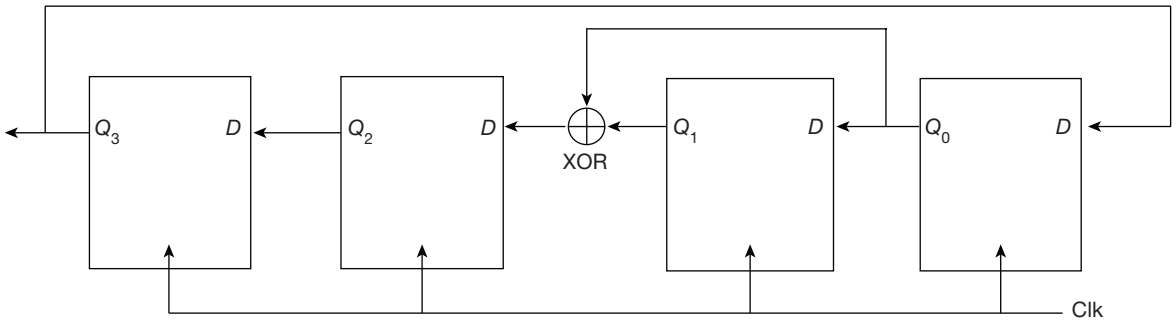
20. If $(3.5)_{\text{base 6}} + (2.3)_{\text{base 6}} = (X)_{\text{base 6}}$ then the value of X is:
(A) 5.8 (B) 10.2
(C) 6.2 (D) 5.6

21. If the following circuit is converted to all-NAND network, then How many number of NAND gates are required? (inverted inputs are available)

(A) 3 (B) 4
(C) 5 (D) 6

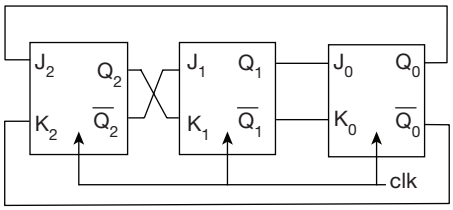


22. A 4-bit shift register is connected as shown with initial states $Q_3\ Q_2\ Q_1\ Q_0 = 0100$. What is state $Q_3\ Q_2\ Q_1\ Q_0$ after 5 clock pulses?



(A) 0111 (B) 1100
(C) 1111 (D) 1001

23.



For the counter shown above the initial state is $Q_2Q_1Q_0$ is 101, what is state after 5 clock pulses?

(A) 111 (B) 011
(C) 100 (D) 000

24. A cache access requires one clock cycle and handling cache miss stalls the processor for an additional 4 clock cycles. Which of the following cache hit rates comes closest to achieve an average memory access of 2 cycles?

(A) 75% (B) 80%
(C) 85% (D) 90%

25. Consider a byte-addressable system with 16-bit addresses associated a cache, which has a two-way set-associative write-back cache with perfect LRU replacement. The Tag store requires a total of 4608 bits of storage. What is the block size of the cache?

(A) 4 B (B) 5 B
(C) 32 B (D) Data insufficient

26. Consider a system employing interrupt-driven I/O for a particular device that transfers data at an average of 10 KB/sec on a continuous basis. Assume that interrupt processing takes about 200 µs. What fraction of processor time is consumed by this I/O device if it interrupts for every byte?

(A) 0.2 (B) 2
(C) 20 (D) 200

27. Consider a program which takes 200 seconds to execute. Of his time, 30% is used for multiplication, 40% for memory access instructions and 30% for other tasks. To enhance the performance, make multiply instructions run four times faster than before. What will be the speed up be if you improve the multiply instruction time?

(A) 0.29 (B) 0.71
(C) 1.29 (D) 1.71

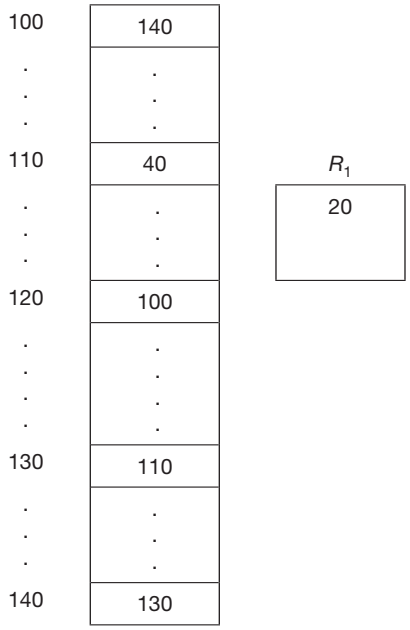
28. Consider the following code sequence (First operand is destination):

LOOP: LOAD R_0, 0(R_{10})
MUL R_0, R_0, R_2
LOAD R_4, 0(R_{11})
ADD R_0, R_0, R_4
STORE R_0, 0(R_{11})
SUB R_{10}, R_{10}, #8
SUB R_{11}, R_{11}, #8
BNEZ R_{10}, LOOP

How many 'WAW' hazards are there in given code?

(A) 8 (B) 5
(C) 3 (D) 0

29. Suppose we have an instruction
'LOAD 100'.
The memory and register R_1 contain the values as given below:

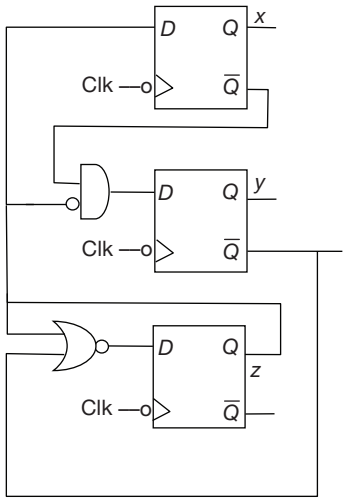


Assuming R_1 is implied in the indexed addressing mode, what will be the actual value loaded into accumulator in immediate, direct, indirect and indexed mode respectively:
(A) 140, 140, 130, 100 (B) 100, 140, 130, 100
(C) 140, 100, 130, 20 (D) –, 100, 140, 120

30. How many bits would you need, to address a $2G \times 32$ memory, if the memory is byte-addressable and word addressable respectively?
(A) 36, 31 (B) 31, 31
(C) 31, 36 (D) 36, 36

31. Suppose a computer using direct mapped cache has 2^{20} words of main memory and a cache of 32 blocks, where each cache block contains 16 words. To which cache block will the memory reference $(0DB63)_{16}$ map?
(A) 3 (B) 22
(C) 32 (D) 10

Common Data for Questions 32 and 33:
Consider the following circuit involving three D-type flip flops used in a certain type of counter configuration.



32. If at some instance prior to the occurrence of the clock edge x, y and z have a value 0, 1, and 1, what shall be the value of xyz after the clock edge?
(A) 000 (B) 100
(C) 010 (D) 101

33. If all the flip flops were reset to 0 at power on, what is the total number of distinct outputs (states) represented by xyz generated by the counter?
(A) 4 (B) 5
(C) 6 (D) 7

Common Data for Questions 34 and 35:
A processor requires 2000 cycles to perform a context switch and start an interrupt handler or 1000 cycles to poll an I/O device. An I/O device attached to that processor makes 100 requests per second, each of which takes 10,000 cycles to resolve once the handler has been started. By default, the processor polls every 0.5 ms if it is not using interrupts.

34. How many cycles per second does the CPU spend handling I/O from the device if interrupts are used?
(A) 1400000 (B) 1200000
(C) 14000 (D) 12000

35. How many cycles per second are spent on I/O if polling is used?
(A) 1000000 (B) 2000000
(C) 3000000 (D) 5000000

Answer Keys

1. D	**2.** B	**3.** B	**4.** C	**5.** B	**6.** D	**7.** A	**8.** D	**9.** D	**10.** A
11. C	**12.** D	**13.** A	**14.** B	**15.** A	**16.** B	**17.** B	**18.** C	**19.** D	**20.** B
21. A	**22.** D	**23.** A	**24.** A	**25.** C	**26.** B	**27.** C	**28.** C	**29.** B	**30.** A
31. B	**32.** B	**33.** A	**34.** A	**35.** C					

Hints and Explanations

1. The characteristic equation of *SR* flip flop is:

$Q_{n+1} = S + \bar{R}\,Q_n$

Given (from circuit) $S = A \cdot \bar{Q}_n, R = B \cdot Q_n$

$Q_{n+1} = A\bar{Q}_n + \bar{B} \cdot \bar{Q}_n\,Q_n$

$= A\bar{Q}_n + (\bar{B} + \bar{Q}_n)Q_n$

$Q_{n+1} = A\bar{Q}_n + \bar{B}$

The equation is like JK flip flop equation.

(JK equation $Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$)

So it works like *T* flip flop if $A = B$. Choice (D)

2. If $a \le b$ then

a	b	$a^1 + b$	ab^1
0	0	1	0
0	1	1	0
1	1	1	0

($ab = 10$ is not valid condition for $a \le b$)

We can observe that $a^1 \ge b^1$, so only (*P*) $a^1 + b = 1$, (*R*) $ab^1 = 0$ are true. Choice (B)

3. From given $a = (b + c)(b^1 + c^1)$

$= bc^1 + b^1c$

$= b \oplus c$

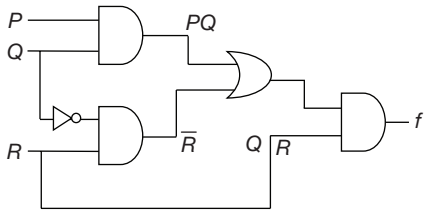
EXOR with *c* both sides

$a \oplus c = b \oplus c \oplus c = b \oplus 0 = b$

So, $b = a \oplus c = a^1c + ac^1$ or $(a + c)(a^1 + c^1)$.

Choice (B)

4.



$f = (PQ + \bar{Q}R)R = PQR + \bar{Q}R$

$= (PQ + \bar{Q})R = (P + \bar{Q})R$

$= PR + \bar{Q}R$ Choice (C)

5. Given circuit is Demultiplexer

Output equation are $Y_0 = I\,\bar{S}_1\,\bar{S}_0$

$Y_1 = I\,\bar{S}_1\,S_0$

$Y_2 = I\,S_1\,\bar{S}_0$

$Y_3 = I\,S_1\,S_0$

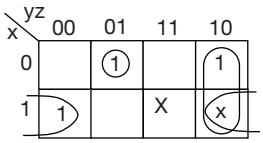
$F(a, b) = \overline{\bar{Y}_0 \cdot \bar{Y}_3} = Y_0 + Y_3 = 1 \cdot a^1b^1 + 1 \cdot ab$

$= a^1\,b^1 + ab = (a^1 + ab)(b^1 + ab)$

By applying $x + yz = (x + y)(x + z) = (a^1 + b)(a + b^1)$

Choice (B)

6. If the output of the circuit is *F* then $F(x, y, z) = \Sigma(1, 2, 4) + d(6, 7)$ in the given range 000 to 101, only for inputs 001, 010, 100 output is 1 (min terms) 110, 111 are unused combinations (don't cares)



$F(x, y, z) = xz^1 + yz^1 + x^1y^1z$

$= (x + y)z^1 + x^1y^1z$

$= (x^1y^1)^1z^1 + (x^1y^1)z = (x + y)z^1 + (x + y)^1z$

$= x^1\,y^1 \odot z = (x + y) \oplus z$ Choice (D)

7. $f = b + cd + ade$

a b c d e

b = - 1 - - - $\rightarrow$ 16 min terms (2^4)

cd = - - 1 1 - $\rightarrow$ 8 min terms (2^3)

in these 8 terms, 4 terms will have $b = 1$,

so 8 – 4 = 4 terms

ade = 1 - - 1 1 $\rightarrow$ 4 min terms (2^2)

these 4 terms are already present in first 16 terms so no need to count them. Total = 16 + 4 = 20 Choice (A)

8. Given functional table is same as JK flipflop with $J = \bar{X}, K = \bar{Y}$, so $Q_{n+1} = \bar{X}\bar{Q}_n + Y$

Q_n Choice (D)

9. Choice (D)

10. Choice (A)

11. Given number: 00001111. The sign is '0', so the number is positive.

∴ Decimal equivalent = +15. Choice (C)

12.

–6 =	1	0	0	0	0	1	1	0

(SM)

In one's complement,

– 6 = 11111001

Arithmetic Right shift of –6 = 11111100

(sign bit must be same). Choice (D)

13. LRU replaces locations that have the lowest probability of being accessed in the cache. Choice (A)

14. Cache memory doesn't extend the size of main memory but useful in faster program execution. Cache memory contains only some replica of main memory. Choice (B)

15. Choice (A)

16. Given circuit is an Asynchronous counter (ripple counter). All flip flops are in toggle mode.

Q_A is LSB (clk input is connected to Q_A)

Negative edge Clk is connected from *Q*, so it works as UP counter.

$Q_C\ Q_B\ Q_A$ is the sequence, UP counter.
The NAND gate connected from $Q_B\ Q_C$
i.e., whenever output $Q_C\ Q_B\ Q_A$ becomes 110 or 111, the NAND gate output is zero.
i.e., the same zero applied to the active low asynchronous inputs pr, clr of Q_A, QB, Q_C.
so initial state is 001

Clk	Q_C	Q_B	Q_A
0	0	0	1
1	0	1	0
2	0	1	1
3	1	0	0
4	1	0	1
5	0	0	1

So total 5 different states.
∴ Given circuit is mod-5 counter. Choice (B)

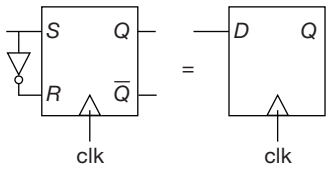
17. Master slave flip flop also works like normal flip flop only, to eliminate race around condition in JK latch, we go for JK master slave flip flop.

From the circuit $J_0 = \bar{Q}_1, K_0 = 1, J_1 = Q_0, K_1 = \bar{Q}_0$

clk	Q_1	Q_0	$J_1 = Q_0$	$K_1 = \bar{Q}_0$	$J_0 = \bar{Q}_1$	$K_0 = 1$
0	0	0	0	1	1	1
1	0	1	1	0	1	1
2	1	0	0	1	0	1
3	0	0				

∴ 3 clk pulses required to reset again. Choice (B)

18.



We can observe that *SR* connected in *D* flip flop mode, *S*, *R* are connected with normal (Q), complemented $(\bar{Q})$ output forms.

We can draw the circuit as follows
From given circuit $D_0 = Q_2$, $D_1 = Q_0$

$$D_2 = (Q_1 + Q_0)(\overline{Q_1 \cdot Q_0}) = (Q_1 + Q_0)(\bar{Q}_1 + \bar{Q}_0) = Q_1 \oplus Q_0$$

clk	Q_2	Q_1	Q_0	$D_2 = Q_1 \oplus Q_0$	$D_1 = Q_0$	$D_0 = Q_2$
0	1	1	1	0	1	1
1	0	1	1	0	1	0
2	0	1	0	1	0	0
3	1	0	0	0	0	1
4	0	0	1	1	1	0
5	1	1	0	1	0	1
6	1	0	1	1	1	1
7	1	1	1			

∴ The state sequences of given circuit are 7, 3, 2, 4, 1, 6, 5, 7 . . . Choice (C)

19. Even function is a Boolean function, which will be equal to 1, if the input variables have an even number of 0's.

(odd function is a Boolean function for which output is 1, for input combinations with odd number of 1's)

So for 4 variables, even number of zeroes occur for input combinations 0000, 0011, 0101, 0110, 1001, 1010, 1100, 1111

For these combinations, even function output is 1.

So remaining terms are max terms.

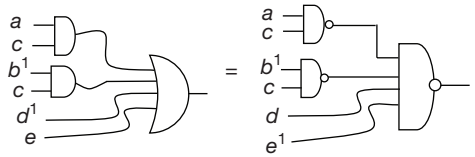
So $f_{even} = \prod M(1, 2, 4, 7, 8, 11, 13, 14)$

Choice (D)

20. 3.5
+ 2.3
?
$5 + 3 = 8$
$(8)_{10} = (12)_6$, so result is 2 and carry is 1.
1
3.5
+2.3
?.2
$1 + 3 + 2 = 6$
$(6)_{10} = (10)_6$, so result is 0 and carry is 1
3.5
+ 2.3
10.2 Choice (B)

21. Given function has to be in SOP form, so it can be implemented by AND-OR gates, same as NAND-NAND gates

$f(a, b, c, d, e) = (a + b^1)c + cd^1 + (d^1 + e)$
$= ac + b^1c + cd^1 + d^1 + e$



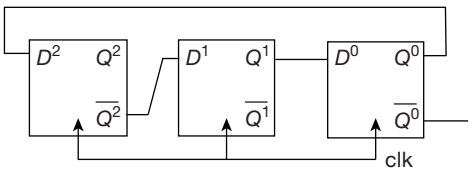
$= ac + b^1\ c + d^1 + e$ Choice (A)

22.

	Present state				Q_2	$Q_1 \oplus Q_0$	Q_0	Q_3
Clk	Q_3	Q_2	Q_1	Q_0	D_3	D_2	D_1	D_0
0	0	1	0	0	1	0	0	0
1	1	0	0	0	0	0	0	1
2	0	0	0	1	0	1	1	0
3	0	1	1	0	1	1	0	0
4	1	1	0	0	1	0	0	1
5	1	0	0	1	0	1	1	1
6	0	1	1	1				

Choice (D)

23. Given circuit can be drawn as



As JK flip flop is used in Data mode $(J = \bar{K})$

Clk	Q_2 Q_1 Q_0
0	1 0 1
1	1 0 0
2	0 0 0
3	0 1 0
4	0 1 1
5	1 1 1

Choice (A)

24. Average access time = 2
Cache access time = 1
Time to handle miss = 5
Let cache hit rate = x
$2 = 1 \times x + 5\,(1 - x)$
$\Rightarrow \quad x + 5 - 5x = 2$
$\Rightarrow \quad -4x = -3$
$\Rightarrow \quad x = \frac{3}{4} = 0.75$
$\therefore$ Hit ratio = 75%. Choice (A)

25. In 2-way set-associative cache,
t(Tag) + s(Set) + w(Word) = 16
For LRU, use 1-bit per set.
For Valid bit, Dirty bit use 1 bit per block for each.
Let tag has t-bits per block.
Number of sets = 2^s
Number of blocks = 2×2^s
Tag store size = $2^s + 2 \times 2^s \times (2 + t)$
Given tag store size = 4608 bits
$2^s + 4 \times 2^s + 2^{s+1} \times t = 4608$
$\Rightarrow \quad 5 \times 2^s + t \times 2^{s+1} = 2^{12} + 2^9$
$\Rightarrow \quad 2^s(2t + 5) = 2^9 \times 9$
$\Rightarrow \quad s = 9, t = 2 \Rightarrow w = 5$
$\therefore$ Block size = 2^5 = 32 bytes. Choice (C)

26. The device generates 10000 interrupts per second i.e., one for every 100 µs.
Each interrupt requires 200 µs, then fraction of processor time consumed $= \frac{200}{100} = 2$. Choice (B)

27. Speed up $= \dfrac{1}{(1 - \text{fraction}) + \dfrac{\text{Fraction}_{enh}}{\text{Speedup}_{enh}}}$

$= \dfrac{1}{(1 - 0.3) + \dfrac{0.3}{4}}$ Choice (C)

28. There are three WAW hazards.
(1) LOAD R_0, $0(R_{10})$
MUL R_0, R_0, R_2
(2) MUL R_0, R_0, R_2
ADD R_0, R_0, R_4
(3) LOAD R_0, $0(R_{10})$
ADD R_0, R_0, R_4. Choice (C)

29. Immediate: Data is present in instruction i.e., $AC = 100$
Direct: Instruction contains effective address of operand i.e., $AC = M[100] = 140$
Indirect: Instruction contains address of address of operand.
i.e., $AC = M[M[100]] = M[140] = 130$
Indexed: Address part of instruction is added with IR.
i.e., $AC = M[IR + 100] = M[20 + 100] = M[120] = 100$.
Choice (B)

30. Memory capacity : $2G \times 32 = 2^{31} \times 2^5$
Byte Addressable requires 36-bits for an address.
Word addressable requires 31-bits. Choice (A)

31. Main memory = 2^{20}
Number of blocks in cache = 32
Block size = 16 words

Tag	Line	Word
11	5	4

Given address $(0DB63)_{16}$

	0000 1101101	10110	0011
=	Tag	line	word

Line = 10110 = $(22)_{10}$. Choice (B)

32. From the given circuit, inputs are
As all flip flops are D flip flops, output (as of input) will be same as D-state.
Given initially $xyz = 011$.
So $D_x = 1, D_y = 0, D_z = 0$
So next state $xyz = 100$. Choice (B)

33.

Clk	x	y	z	$D_x = z$	$D_y = \bar{x}\bar{z}$	$D_z = \bar{z}y$
0	0	0	0	0	1	0
1	0	1	0	0	1	1
2	0	1	1	1	0	0
3	1	0	0	0	0	0
4	0	0	0			

After 4 clk pulses again come back to original state (000) so number of states are 4. Choice (A)

34. I/O device generates 100 requests.
Each request requires an interrupt.
The time taken for one request is
= 2000 + 10000 + 2000 = 14000 (to start handler, execute handler, switch to original program).
Total there are 100 requests so cycles required
= 14000 × 100 = 1400000. Choice (A)

35. The processor polls for every 0.5 ms. In one second there will be $\frac{1}{0.5\times10^{-3}}$ polls i.e., 2000 times.

Each poll requires 1000 cycles.

So it requires 2000000 cycles.

There are 100 requests, each requires 10000 cycles, total 1000000 cycles to complete.

$\therefore$ Total time spent on I/O each second

= 2000000 + 1000000 = 3000000. Choice (C)