Counters

7

Introduction

- It is a sequential circuit forming by the cascading of FFs.
- Counter are basically used for
  (i) Counting of the number of clock pulses applied
  (ii) Frequency division
  (iii) Timers
  (iv) Frequency measurement
  (v) Waveform generation
- Counters are classifed as:
  (i) Asyr chronous counter
  (ii) Synchronous counter

Remember:

- If N = total number of states and 'n' = number of FFs then

$$N \leq 2^n$$

$$n \geq 3.32 \log_{10} N \text{ or } n \geq \log_2 N$$

- If $N = 2^n$, then we get BINARY COUNTER.
- If $N < 2^n$, then we get NON-BINARY COUNTER.

MOD number

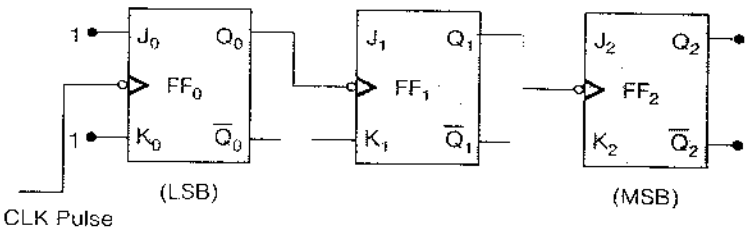
- The "MOD-number" indicates the number of states in counting sequence.
- For n-FFs, counter will have 2^n different states and then this Counter is said to be "MOD-2^n Counter".
- MOD number indicates the frequency division factor obtained from the Last FF.
- It would be capable of counting upto $(2^n - 1)$ before returning to zero state.

Note:

- In "MOD-N Counter", if applied input frequency is "f", then output frequency is f/N.
- If two counters are cascaded with MOD-M followed by MOD-N, then number of overall states of combined counter is (M × N) and counter is called "MOD-MN" counter.

Asynchronous (Series) Counter

Binary Ripple Counter



- In ripple counter with n-FFs there are 2^n possible states.
- With n-FFs the maximum count that can be counted by this counter is $(2^n - 1)$.
- If input frequency is 'f' then output frequency is $\frac{f}{2^n}$.
- It is also known as 2^n : 1 scalar divider.

For proper operation of the ripple counter:

$$T_{CLK} \geq n\, t_{pd(FF)}$$

$$f_{CLK} \leq \frac{1}{n\, t_{pd(FF)}}$$

Maximum CLK frequency:

$$f_{CLK,m} = \frac{1}{n\, t_{pd(FF)}}$$

Disadvantage of Ripple Counter:

Decoding error is present due to propagation delay of FFs i.e. $t_{pd(FF)}$.

Up/Down Counter

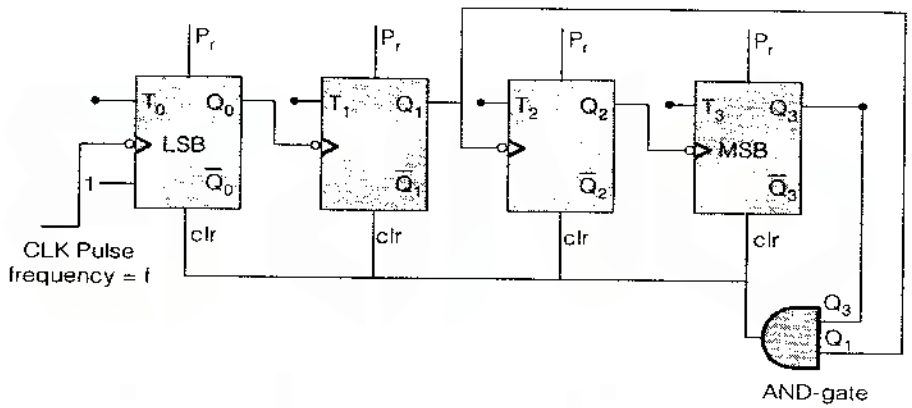
An "Up/Down Counter" can count in any direction depending upon the control input.

For determination of Up/Down Counter:

Triggering with	CLK connection in	Access as
(–ve) edge	Q	UP Counter
(–ve) edge	$\overline{Q}$	Down Counter
(+ve) edge	Q	Down Counter
(+ve) edge	$\overline{Q}$	UP Counter

Non-Binary Ripple Counter

Decade Counter or Mod-10 Counter

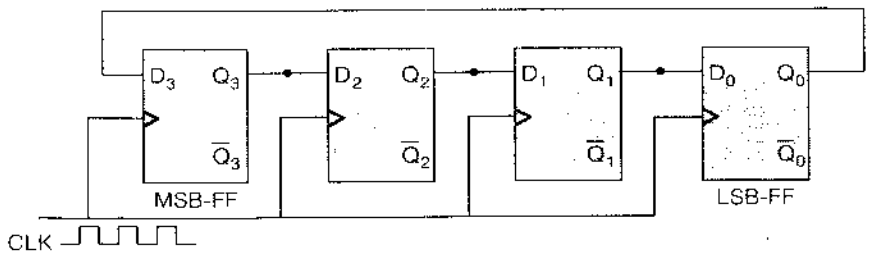


- Used states = 10 and unused states = 6
- For down counter, Mod Number = $2^n - N$.
- Output frequency of MOD-10 counter = f/10.
- Clear and preset is used in non binary ripple counter.
- Clear is used to reset counter without clock.
- Preset is used to set counter.
- When decade counter counts from 0 to 9 then it is known as BCD counter.

Synchronous (Parallel) Counters

Ring Counter

It is SISO shift register.



Remember:

- Ring counter is a non-self starting counter.
- With 'n' FFs, there are n-states present in ring counter.
- With 'n' FFs, maximum count possible in ring counter is $(2^n - 1)$.
- Decoding is very easy in Ring counter, because there is no aid of extra circuit.

In a 4-bit ring counter:

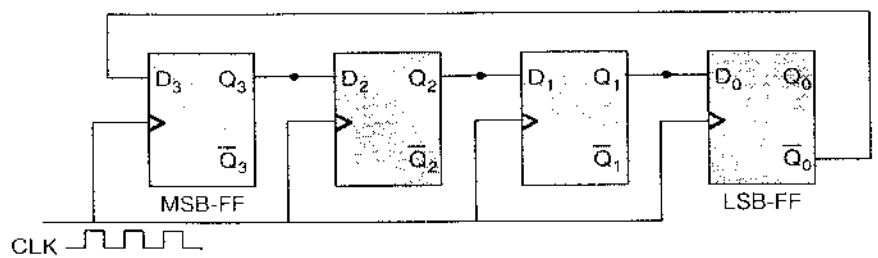
Used states = 4

Unused states = $2^4 - 4 = 12$

- In a ring counter if CLK frequency is "f" the FFs output frequency is "f/N" (where N = Number of states = modulus of the counter).

Twisted-Ring Counter

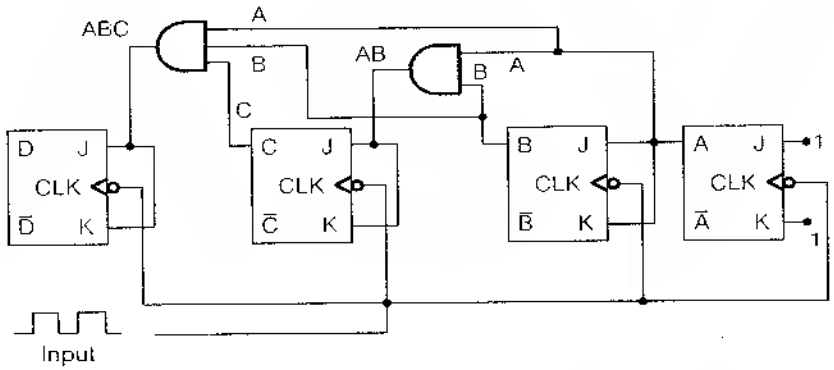
Also known as Johnson Counter or Switch Tail Ring Counter



Remember:

- With 'n' FFs there are '2n' states in this counter.
- With 'n' FFs the maximum count by this counter is $(2^n - 1)$.
- In normal "Johnson Counter" with 'n' FFs and the input frequency is 'f' then output frequency of FFs is "f/2n"
- In a "Counter" if a feedback connection is used the number of possible states will decreases.

Synchronous-Series Carry Counter



❑ Clock frequency

$$f_{CLK} \leq \frac{1}{t_{pd(FF)} + (n-2)\, t_{pd(AND\text{-}gate)}}$$

Remember:

- Total delay of this counter is much lower than an asynchronous counter with same number of FFs.

$$\text{total delay} = FF\, t_{pd(FF)} + t_{pd(AND\ gate)}$$

Synchronous-Parallel Carry Counter

It is the "Fastest Counter".

Clock frequency:

$$f_{CLK} = \frac{1}{t_{pd(FF)} + t_{pd(AND\ gate)}}$$

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