Chapter 11

Sample and Hold, A/D and D/A Circuits

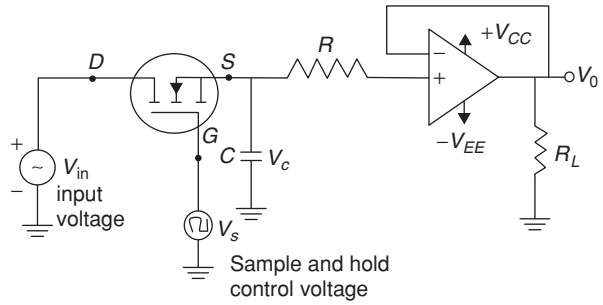
LEARNING OBJECTIVES

After reading this chapter, you will be able to understand:

- Sample and hold circuit
- Digital to analog converter
- Weighted resistor DAC
- R – 2R ladder DAC
- Analog to digital converters
- Parallel comparator (Flash) A/D converter
- The counter type A/D converter
- Servo tracking A/D converter
- Successive approximation converter
- Charge balancing ADC
- Dual scope A/D converter

Sample and Hold Circuit

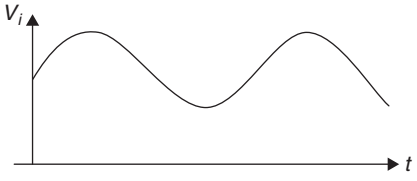
The sample and hold circuit as its name implies, samples an input signal and holds on to its last sampled value until the input is sample again.



The analog signal V_{in} to be sampled is applied to the drain, and sample and hold control voltage (V_s) is applied to the gate of E-MOSFET.

During positive portion of V_s, the MOSFET conducts and acts as a closed switch. This allows the input voltage to charge Capacitor C, i.e., input voltage appears across C and in turn at the output.

When V_s is zero, the E-MOSFET is off (non-conductive) and acts as an open switch, the only discharge path for C is through OP amp. However the input resistance of OP Amp is very high, So voltage across C is retained.



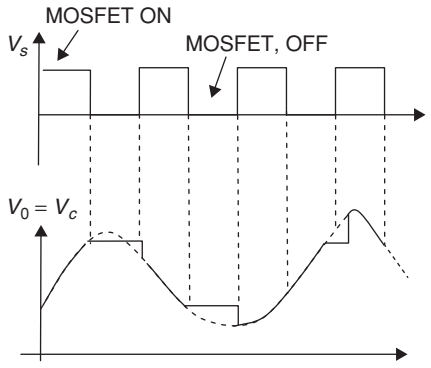
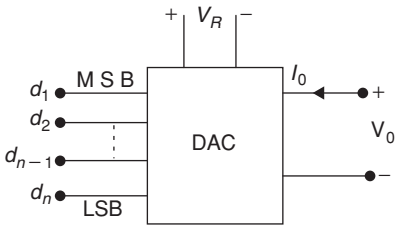


Figure 1 Input and output waveforms

To obtain close approximation of the input wave form, the frequency of the sample and hold control voltage must be significantly higher than that of the input. The sample and hold circuit is commonly used in digital interfacing and communications.

Digital to Analog Converter

The input is an n bit Binary word D and is combined with a reference voltage V_R to give an analog output signal.



For a voltage output (DAC) the D/A converter is mathematically described as

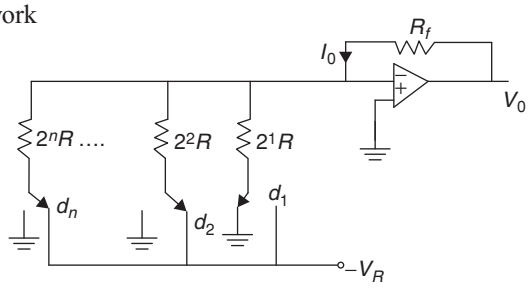
$$V_0 = K.V_{FS}\,(d_1\,2^{-1} + d_2\,2^{-2} + \cdots + d_n\,2^{-n})$$

V_0 – output voltage, V_{FS} – Full scale output voltage and K – Scaling factor,

Binary word $D = d_1\,d_2 \ldots d_n$

Weighted Resistor DAC

It uses a summing amplifier with a binary weighted resistor network

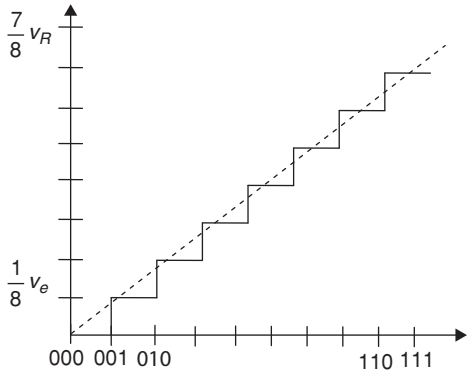


$$V_0 = I_0\,R_f$$

$$= V_R\,\frac{R_f}{R}(d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n})$$

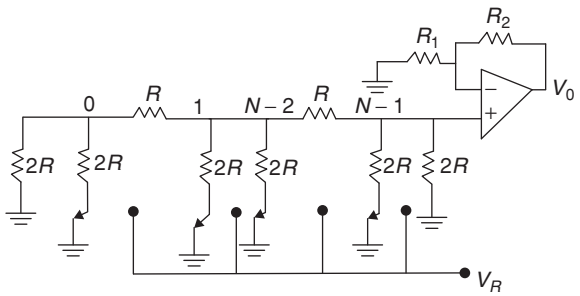
The OP Amp can be connected either in inverting or non inverting mode,

The OP Amp is simply working as a current to voltage converter.



This DAC uses wide range of resistances $2R$–2^nR, so it is not suitable for integrated circuits

R–2R Ladder DAC



This circuit utilizes twice the number of resistors as in binary weighted DAC, for the same number of bits (N) but of values R and $2R$ only.

The ladder used in this circuit is a current splitting device, at any of the ladder nodes the resistance is $2R$ looking, to the left or the right or towards the switch.

Example 1: The basic step of a 8-bit DAC is 12 mV. If 00000000 represents 0 V. What is the output for input 10110101?

Solution: Output is = 12 mV $(1 \times 2^7 + 1 \times 2^5 + 1 \times 2^4 + 1 \times 2^2 + 1 \times 2^0) = 2.172$ V

Example 2: The values of LSB, MSB, and full scale output for an 8-bit DAC for 0 to 10 V range are?

Solution: $\text{LSB} = \frac{1}{2^8} = \frac{1\text{th}}{256}$ of full scale voltage

$$\text{LSB} = \frac{10}{256} = 39.\text{ mV}$$

$$\text{MSB} = \left(\frac{1}{2}\right) \text{full scale voltage} = 5\text{ V}$$

Full scale output = Full scale reading = (full scale voltage – 1 LSB)

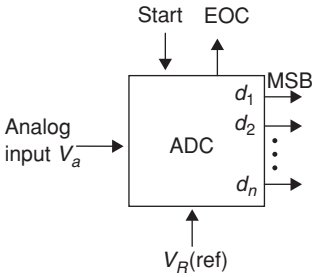
= 10 V – 0.039 V = 9.961 V

1. Resolution $= \frac{\text{FSV}}{2^n} = \frac{\text{FSR}}{2^n - 1}$
2. $\text{MSB} = \frac{\text{FSV}}{2}$

Analog to Digital Converters

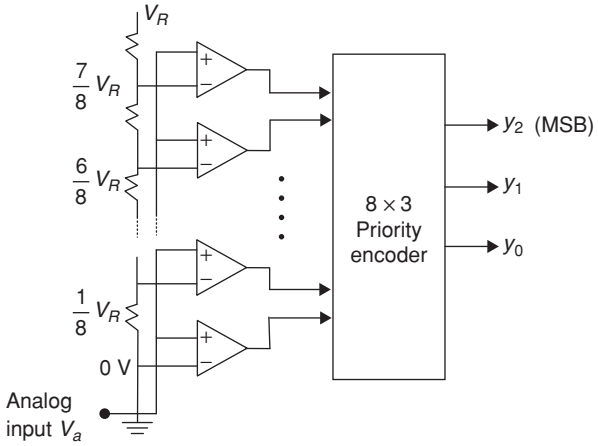
The block schematic of ADC is shown in the figure, it provides the function just opposite to that of a DAC. It accepts an analog input voltage V_a and produces an output binary word $d_1\,d_2 \ldots d_n$. of functional value D

So that



$$D = d_1\,2^{-1} + d_2\,2^{-2} + \cdots + d_n\,2^{-n}$$

Parallel Comparator (Flash) A/ D converter



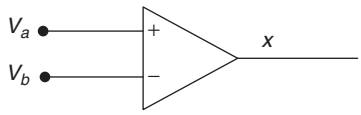


Figure 2 Basic circuit of a flash type A/D converter.

Table 1 *Comparator and its truth table*

Voltage Input	Logic Output
$V_a > V_b$	$X = 1$
$V_a < V_b$	$X = 0$
$V_a = V_b$	Previous value

This is the simplest possible A/D, converter, at the same time, the fastest and most expensive technique. At each node of the resistor divider, a comparison voltage is available, the purpose of this circuit is to compare the analog, input voltage V_a with each of the node voltages. In general the number of comparators required is $2^n - 1$ for n-bit ADC. Hence number of comparators doubles for each added bit.

The Counter Type A/D Converter

The clear pulse resets the counter to zero count, the counter then records in binary form the number of pulses form the clock line.

The principle is to adjust the DAC's input code until the DAC's output comes within $\pm\frac{1}{2}$LSB to the analog input V_a which is to converted to binary digital from the counter frequency must be low enough to give sufficient time for DAC to settle and for the comparator to respond, low speed is the major draw back in this method.

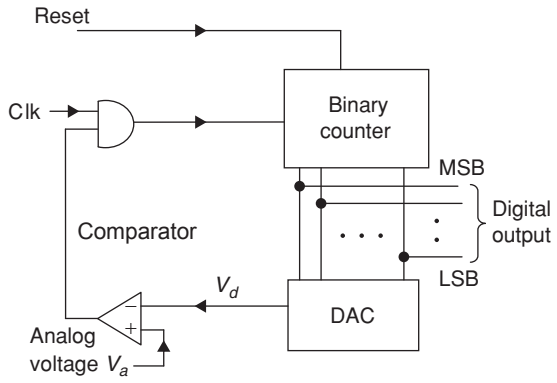


Figure 3 Counter type A/D converter

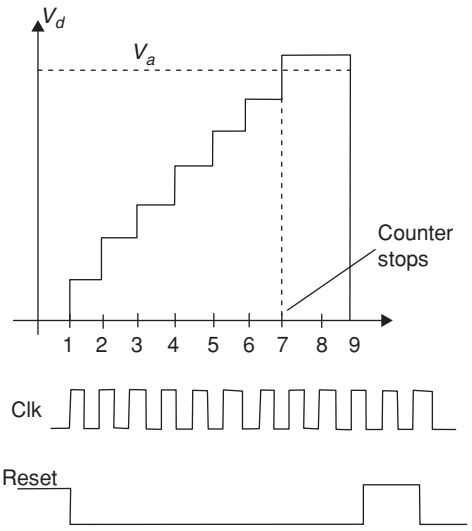


Figure 4 D/A output staircase waveform

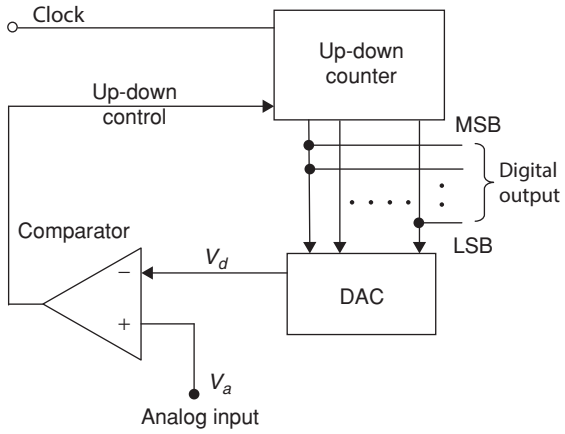
The conversion time can be as long as $(2^n - 1)$ clock periods depending upon the magnitude of the input V_a. For example, 12-bit system with 1MHz clock frequency, the counter will take $(2^{12} - 1)$ μs = 4.095 ms to convert a full scale input.

If the input signal is a sampled signal, the minimum interval between samples must be nT seconds for T – clock period, and maximum value of input voltage is represented by n-pulses.

Servo Tracking A/D Converter

An improved version of counting ADC is the tracking or a servo converter shown in the figure.

The circuit consists of an up/down counter with the comparator controlling the direction of the count



The analog output of the DAC is V_d and is compared with the analog input V_a.

If input $V_a > V_d$, the output of the comparator goes high and the counter is caused to count up.

The DAC output increase with each incoming clock pulse and when it becomes more than V_a, the counter reverses the direction and counts down.

The process goes on being repeated and digital output changes back and forth, by ±1 LSB around the correct value. The disadvantage is, however, the time needed to stabilize as a new conversion value is directly proportional to the rate at which the analog signal changes.

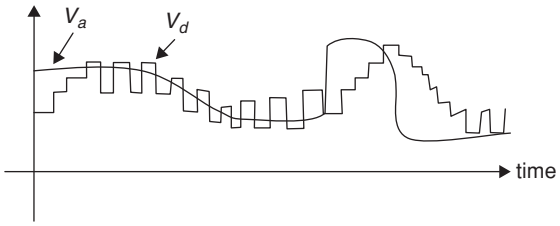
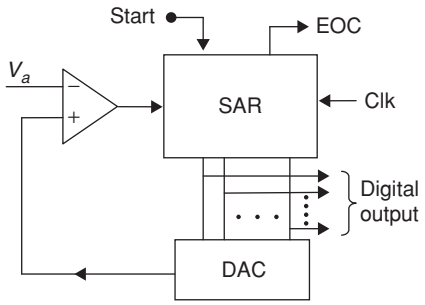


Figure 5 Wave forms associated with tracking ADC.

Successive Approximation Converter

The successive approximation technique uses a very efficient code search strategy to complete *n*-bit conversion in just n clock periods.

This circuit uses a successive approximation register (SAR) to find the required value of each bit by trial and error



Functional diagram of successive approximation ADC

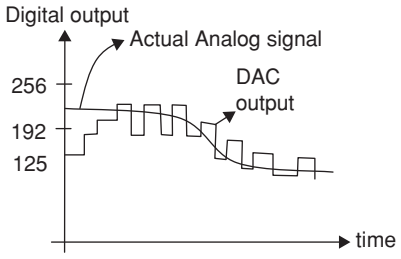


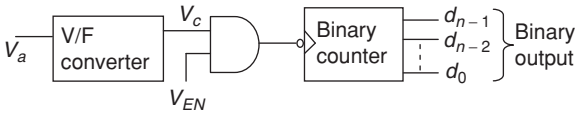
Figure 6 The D/A output voltage and analog input voltage

It can be seen that the D/A output voltage becomes successively closer to the actual analog input voltage. In general the successive approximation ADC technique is more versatile and superior to all other circuits

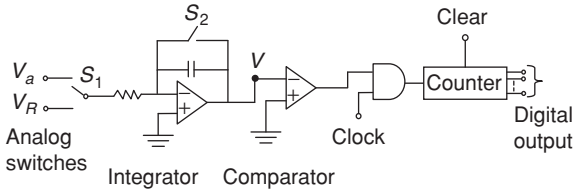
For all the ADCs which use DAC as one of their components, the major drawback is, the resolution of ADC will depend upon resolution of DAC.

Charge Balancing ADC

The principle of charge balancing ADC is to first convert the input signal to a frequency using a voltage to frequency (V/F) converter. This frequency is then measured by a counter and converted to an output code proportional to the analog input.

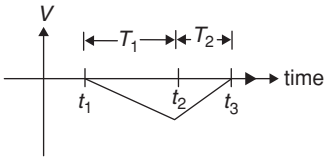


Dual Scope A/D Converter



$$V_a = V_R \cdot \frac{T_2}{T_1} = \frac{n_2 |V_R|}{n_1}$$

$$= n_2 \cdot \frac{|V_R|}{2^N}$$



This is widely used system with $V_a > 0$, $V_R < 0$, Initially counter cleared and at $t = t_1$, S_1 connects V_a and sampled for $n_1 = 2^N$ clock pulses. At the time t_2(at the end of the integration of v_a), all flip flops in the counter read 0.

Now the reference Voltage V_R is automatically connected to the input reference voltage V_R is automatically connected to the input of the integrator, at $t = t_2$, we have assumed that $|V_R| > V_a$, so that the integration time T_2 is less than T_1, as indicated. As long as V is negative the output of the comparator is positive and the AND gate allows clock pulses to be counted. When V falls to zero, at $t = t_3$, the AND gate is inhibited and no further clock pulses enter the counter.

$$V_a = n_2 \cdot \frac{|V_R|}{2^N},$$

V_a is proportional to counter reading n_2.

This technique can be very accurate; six digit digital voltmeters employ such signal processing, the dual scope system is inherently noise–immune because of input signal integration.

Conversion time = 2^{N+1}. Clk cycles

Resolution: the resolution of a converter is the smallest change in voltage which may be produced at the output or input of converter.

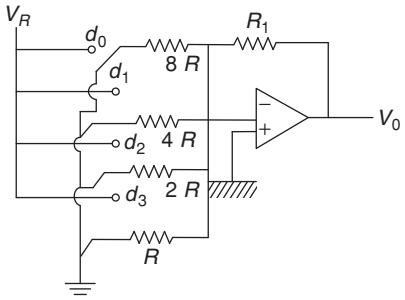
$$\text{Resolution} = \frac{V_{FS}}{2^N - 1} = 1 \text{ LSB} \quad \text{LSB increment}$$

EXERCISES

Practice Problems I

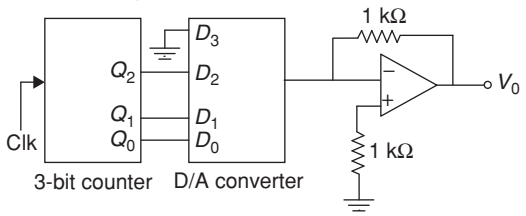
Directions for questions 1 to 10: Select the correct alternative from the given choices.

1. A 4-bit weighted DAC has $V_R = 2$ V and $\frac{R_1}{R} = 2$. For an input of 1000 the output will be

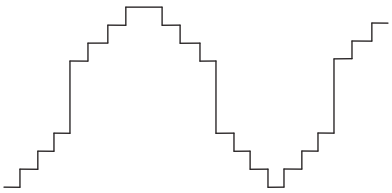


(A) −2 V (B) −4 V
(C) −8 V (D) 8 V

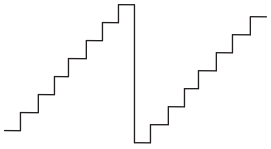
2. A 4-bit D/A converter is connected to free running 3-bit up-counter as shown. What will be the wave form obtained at v_0?



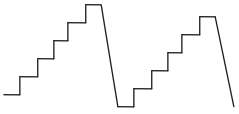
(A)



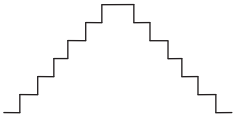
(B)



(C)



(D)



3. A 10-bit A/D converter is used to digitize an analog signal in the range 0 to 10 V. The maximum peak to peak ripple voltage that can be allowed in the dc supply voltage is____

(A) nearly 100 mV (B) nearly 10 mV
(C) nearly 25 mV (D) nearly 5 mV

4. For a dual ADC type $3\frac{1}{2}$ DVM, reference voltage is 200 mV and first integration time is 400 mS. For same input voltage de-integration is 470.2 mS. The DVM will indicate

(A) 200 mV (B) 235.1 mV
(C) 199.9 mV (D) 1.818 mV

5. In the case of a dual slope integrating type A/D converter if the output of 10-bit counter is clocked at 1 MHz, maximum frequency of analog signal that can be converted using A/D converter is

(A) 3 kHz (B) 2 kHz
(C) 20 kHz (D) 1 kHz

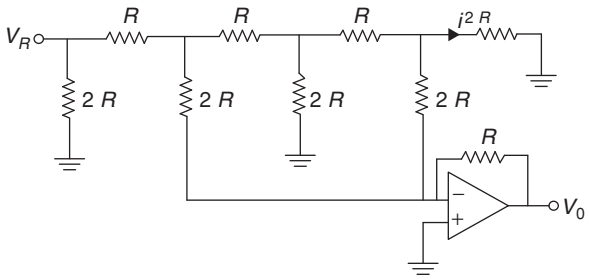
6. An 8-bit digital ramp ADC with a 50-mV resolution uses a clock frequency of 2.5 MHz and a comparator with $V_T = 1$ mV. The digital output for $V_A = 6$ V is

(A) 01111000 (B) 10010110
(C) 01011110 (D) 01011111

7. A sample and hold circuit having a holding capacitor of 0.1 nF is used at the input of a ADC. The conversion time is 1 μs and during this time the capacitor should not lose more than 0.1% of charge put across it during sampling time. The maximum value of the input signal to the *S/H* circuit is 5 V. The leakage current of *S/H* circuit is less than

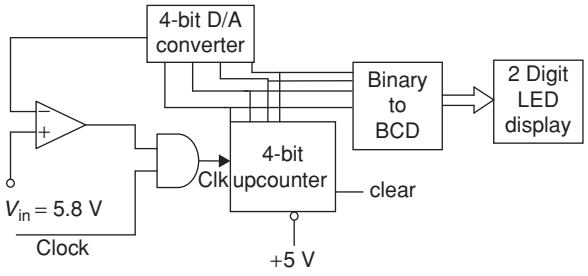
(A) 2.5 mA (B) 0.25 mA
(C) 5 μA (D) 0.5 μA

8. In the D/A converter, $V_R = 10$ V, R = 10 kΩ. Voltage V_0 is



(A) − 0.781 V (B) − 1.562 V
(C) − 3.125 V (D) − 6.250 V

Common Data for Questions 9 and 10: In the circuit comparator output is logic '1', if $V_1 > V_2$, and is logic '0' otherwise. The D/A conversion is done as per the relation. $V_{DAC} = \sum_{n=0}^{3} 2^{n-1} b_n$ V where b_3 (MSB), b_2, b_1 and b_0 are counter outputs. The counter starts from clear state.



9. The stable state of LED displays is
(A) 06 (B) 07
(C) 10 (D) 13

10. The magnitude of error between V_{DAC} and V_{in} at steady state in V.
(A) 0.2 V (B) 0.7 V
(C) 0.5 V (D) 0.1 V

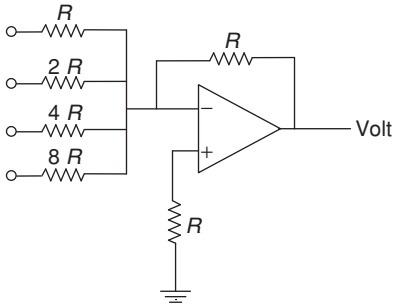
Practice Problems 2

Directions for questions 1 to 10: Select the correct alternative from the given choices.

1. The minimum number of comparators required to build n-bit flash ADC is
(A) 2^{n-1} (B) $2n$
(C) 2^n (D) $2^n - 1$

2. If the resolution of D/A converter is approximately 5% of its full scale range then it is an
(A) 8-bit converter (B) 10-bit converter
(C) 12-bit converter (D) 16-bit converter

3. The circuit shown is a 4-bit DAC. The inputs 0 correspond to 0 V and 1 to 5 V. The OP-AMP is ideal but all the resistances and 5 V input has a tolerance of ±10%. The specification of tolerance for the ADC is



(A) ± 35% (B) ± 20%
(C) ± 10% (D) ± 5%

4. A digital to analog converter with a full scale output voltage of 3.5 V has a resolution close to 20 mV. Its bit size is
(A) 4 (B) 8
(C) 16 (D) 32

5. An 8-bit DAC has a full scale output voltage of 15 V. The output voltage when the input is 10111010 is ____.
(A) 10.89 m V (B) 12 m V
(C) 12 V (D) 10.89 V

6. A 12-bit ADC is employed to convert an analog voltage 0 to 12 V, the resolution of the ADC is
(A) 2.44 mV (B) 83.3 mV
(C) 2.92 mV (D)1.0 mV

7. In A 4-bit weighted–resistor D/A converter the resistor value corresponding to LSB is 4 kΩ, then the resistor value corresponding to the MSB will be?
(A) 32 kΩ (B) 16 kΩ
(C) 1/4 kΩ (D) 1/2 kΩ

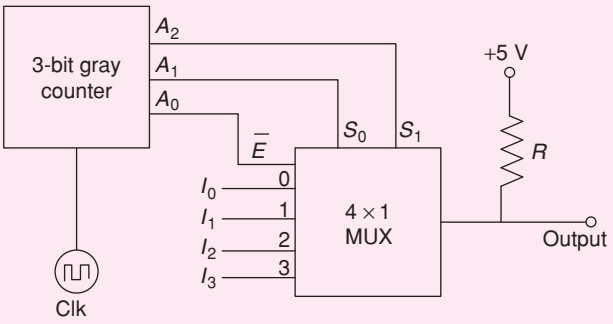
8. 6-bit DAC is having output voltage of 4.2 V for input 101010. The full scale reading of the DAC is?
(A) 6.4 V (B) 6.3 V
(C) 7.2 V (D) 8 V

9. Resolution of 4-bit ADC is 0.2 V, for the input of 2.55 V the output stable state will be?
(A) 1101 (B) 1011
(C) 1100 (D) 1110

10. The correct order for most accurate, fastest, simplest design of ADCs respectively,
(A) Dual scope ADC, Flash type ADC, SAR type ADC
(B) SAR type ADC, Dual scope ADC, Flash type ADC
(C) Flash type ADC, SAR type ADC, Counter type ADC
(D) Dual scope ADC, Flash type ADC, Counter type ADC

Previous Years' Questions

1. A 3-bit gray counter is used to control the output of the multiplexer as shown in the figure. The initial state of the counter is 000_2. The output is pulled high. The output of the circuit follows the sequence **[2014]**



(A) I_0, 1, 1, I_1, I_3, 1, 1, I_2 (B) I_0, 1, I_1, 1, I_2, 1, I_3, 1
(C) 1, I_0, 1, I_1, I_2, 1, I_3, 1 (D) I_0, I_1, I_2, I_3, I_0, I_1, I_2, I_3

2. An 8-bit, unipolar Successive Approximation Register type ADC is used to convert 3.5 V to digital equivalent output. The reference voltage is + 5 V. The output of the ADC, at the end of 3rd clock pulse after the start of conversion, is **[2015]**

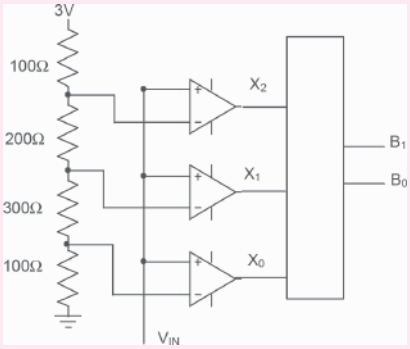
(A) 1010 0000 (B) 1000 0000
(C) 0000 0001 (D) 0000 0011

3. A temperature in the range of −40° C to 55° C is to be measured with a resolution of 0.1° C. the minimum number of ADC bits required to get a matching dynamic range of the temperature sensor is **[2016]**

(A) 8 (B) 10
(C) 12 (D) 14

4. A 2-bit flash Analog to Digital Converter (ADC) is given below. The input is 0 ″ V_{IN} ″ 3 Volts.

The expression for the LSB of the output B_0 as a Boolean function of X_2, X_1, and X_0 is **[2016]**



(A) $X_0\left[\overline{X_1 \oplus X_1}\right]$ (B) $\overline{X_0}\left[\overline{X_2 \oplus X_1}\right]$
(C) $X_0\left[\overline{X_1 \oplus X_1}\right]$ (D) $\overline{X_0}\left[X_2 \oplus X_1\right]$

Answer Keys

Exercises

Practice Problems 1

1. B	**2.** B	**3.** B	**4.** B	**5.** D	**6.** A	**7.** D	**8.** C	**9.** D	**10.** B

Practice Problems 2

1. D	**2.** A	**3.** A	**4.** B	**5.** D	**6.** C	**7.** D	**8.** B	**9.** A	**10.** D

Previous Years' Questions

1. A	**2.** A	**3.** B	**4.** A