COMPUTER ORGANIZATION AND ARCHITECTURE TEST 2

Number of Questions: 25 **Section Marks: 30**

Directions for questions 1 to 25: Select the correct alternative from the given choices.

1. Which of the following memory access methods, will accurately predict the amount of time it will take to receive the data after requesting it?
(A) Sequential access (B) Direct access
(C) Random access (D) Both (B) and (C)

2. In which of the following access method, any location can be accessed in a fixed amount of time after specifying its address?
(A) Sequential access (B) Random access
(C) Direct access (D) None of the above

3. Which of the following statement is TRUE with respect to write-through and write-back techniques?
(A) Write-back scheme is faster than write-through.
(B) Write-through improves performance better than write-back.
(C) Write-through is more complex to implement than write-back
(D) All the above

4. Increasing the degree of associativity of a cache memory will
(A) increases the miss rate.
(B) decreases the miss rate.
(C) increases the number of sets.
(D) decreases the number of elements per set.

5. Which of the following address information is required to identify whether a word in the cache corresponds to the requested word or not?
(A) Tag (B) Index
(C) Line number (D) offset

6. Which of the following factors will be better effected because of larger cache memory?
(i) Hit rate (ii) Cost
(iii) Speed (iv) Power consumption
(v) Reliability
(A) (ii), (iv), (v) (B) (ii), (iii)
(C) (i) only (D) (i), (iii), (iv)

7. If the depth of a pipeline increases, then which of the following is true?
(i) Clock frequency increases
(ii) CPI increases
(iii) Branch mis-prediction penalty reduced.
(A) (i), (ii) only (B) (ii), (iii) only
(C) (i), (iii) only (D) (i), (ii), (iii)

8. Which of the following are the necessary conditions for an n-stage pipeline is n times faster than a non pipelined processor?
(A) Equal cycle time (of the stages).
(B) All instructions take equal number of cycles.
(C) No stalls between instructions.
(D) All of the above

9. Which of the following technique is generally used to avoid WAR and WAW hazards?
(A) By executing an instruction only when the operands are available.
(B) By Register renaming.
(C) Delayed pranching.
(D) All the above

10. Assume a memory access to main memory on a cache miss takes 10 ns and a memory access to the cache on a cache hit takes 1 ns. If 90% of the processors memory requests result in a cache hit, what is the average memory access time?
(A) 2 ns (B) 1 ns
(C) 1.9 ns (D) 1.4 ns

11. Consider the following set of instructions:
I_1: $R_1 \leftarrow R_2 + R_3$
I_2: $R_3 \leftarrow R_1 + R_2$
I_3: $R_1 \leftarrow R_1 * R_3$
The time taken by the 4-stages of the pipeline is given below:

	Fetch	Decode	Execute	Write
I_1	1	2	2	1
I_2	1	2	1	2
I_3	1	1	2	1

What is the number of cycles needed to execute above instructions (use operand forwarding)?
(A) 9 (B) 10
(C) 11 (D) 12

12. Consider the execution of n instructions using k stages of a pipeline, each stage requires 't' time units. Which of the following expression provides the speed up measure of the pipeline?
(A) $\frac{nk}{n+k-1}$ (B) $\frac{nk}{n+k}t$
(C) $\frac{n}{(n+k-1)}$ (D) $\frac{k}{n+k}$

13. Consider 2 MB of RAM and 4 KB of cache with block size of 16 B. What are the sizes of fields used in associative mapping technique?
(A) 16, 5 (B) 8, 9, 4
(C) 9, 8, 4 (D) 17, 4

14. Consider a cache, which requires 2 clock cycles. If there is a cache miss, it will stall the processor for an additional 5 clock cycles. Then what will be the hit rate to achieve an average memory access of 3 clock cycles?

(A) 80% (B) 85%
(C) 90% (D) 95%

15. A digital computer has a memory unit of 64 K × 16 and a cache memory of 1 K words. The cache uses direct mapping with a block size of 4 words. The number of bits present in each line of cache are_____.
(A) 20 bits (B) 22 bits
(C) 26 bits (D) 33 bits

16. Consider a cache of 4 K blocks, a 4 word block size and a 32 bit address main memory. What is the total number of tag bits per set for 4 way set associative cache?
(A) 18 (B) 36
(C) 72 (D) 64

17. A 5-stage pipeline contains IF, ID, FO (fetch operands), EX, WB stages. Each stage takes 1 clock cycle. Consider the execution of the following two instructions on this pipeline:
I_1: ADD *a*, *b*; $a \leftarrow a + b$
I_2: MUL *c*, *a*; $c \leftarrow c * a$
What is the number of clock cycles required for the execution using operand forwarding?
(A) 6 (B) 7
(C) 8 (D) 9

18. Consier a main memory address of *p*-bits and an associated direct-mapped cache of having 2^n blocks. Block size is 2^m bytes. Then the Tag field is of _____ bits.
(A) $p - (n + m + 2)$ (B) $p + n + m$
(C) $p - n + m$ (D) $p - n - m$

19. A 2-way set-associative cache is made up of 32-bit words, has 4 words per line and 4096 sets. Then the cache capacity in bytes is
(A) 32 K (B) 64 K
(C) 128 K (D) 256 K

20. A main memory of a computer has 4096 blocks, each consisting of 128 words. Each word is of 32-bits in size. Then the number of bits present in main memory address is _____ bits.
(A) 18 (B) 19
(C) 20 (D) 21

21. Consider a computer, whose address has *M* bits (using byte addressing), the cache data size is *C* bytes, the block size is $B = 2^b$ bytes and the cache is *k*-way set-associative. Then the number of bits in the set field of the address is given by
(A) $\log_2^c - \log_2^M$ (B) $\log_2^c - \log_2^M - b$
(C) $\log_2^M - b$ (D) $\log_2^B - \log_2^M$

22. Consider a 5-stage pipeline with the stage delays as shown below:

Stage	Delay
Fetch	30 ns
Decode	40 ns
Execute	35 ns
Memory	50 ns
Write	10 ns

Latch delay between the pipeline stages is 2 ns.
What are the cycle time and latency values (in ns) of an instruction respectively?
(A) 50, 50 (B) 52, 260
(C) 50,1 (D) 52, 1

23. Consider the execution of the following program on a 5 stage pipeline with the stages Fetch (*F*), Decode (*D*), Execute (*E*), Memory (*M*) and write (*W*).
ADD R_1, R_2, 10; $R_1 \leftarrow R_2 + 10$
LOAD R_2, 4 (R_1); $R_3 \leftarrow M[R_1 + 4]$
ADD R_4, R_2, R_3,; $R_4 \leftarrow R_2 + R_3$
STORE R_4, 8(R_1); $M[8 + R_1] \leftarrow R_4$
LOAD R_5, 0(R_6); $R_5 \leftarrow M(R_6)$
OR R_5, R_1, R_4,; $R_5 \leftarrow R_1$ or R_4
If each stage requires one clock cycle, the number of stalls required for the program execution with forwarding are
(A) 0 (B) 1
(C) 2 (D) 3

24. The outcome of a branch is given as:
T, *T*, *NT*, *T*
Where *T*: Taken
NT: Not Taken
What is the accuracy of 'always taken' predictor for the above sequence of branch outcomes?
(A) 100% (B) 75%
(C) 50% (D) 25%

25. The outcome of a branch is given as:
T, *T*, *NT*, *T*.
Where *T* : Taken
NT: Not Taken
What is the accuracy of '2-bit predictor' for the above sequence of branch outcome?
(If the 2-bit predictor starts with *T*)
(A) 100% (B) 75%
(C) 50% (D) 25

Answer Keys

1. C	**2.** B	**3.** A	**4.** B	**5.** A	**6.** C	**7.** A	**8.** D	**9.** B	**10.** C
11. B	**12.** A	**13.** D	**14.** A	**15.** B	**16.** C	**17.** A	**18.** D	**19.** C	**20.** D
21. B	**22.** B	**23.** B	**24.** B	**25.** B					

Hints and Explanations

1. Random access uses a decoder to instantly access the location regardless of current state of the memory where as sequential and Direct methods depends on current data read/write position. Choice (C)

2. Choice (B)

3. Write-back scheme is faster than write-through write-back improves performance but is complex to implement. Choice (A)

4. Increasing the degree of associativity of a cache will decrease the miss rate, decreases the number of sets and increases the number of elements per set.
Choice (B)

5. Choice (A)

6. With large cache memories, the hit rate is improved. Cost increases, speed reduced, power consumption is high and reliability is reduced. Choice (C)

7. If there is an increase in pipeline depth then clock frequency, CPI, mis-prediction penalty increases.
Choice (A)

8. Choice (A), (B), (C) are all the necessary conditions for an n stage pipeline to be efficient.
Equal cycle time means no structural hazards. Equal number of cycles means no control hazards.
No stalls means no data hazards. Choice (D)

9. Register renaming is used to avoid WAR and WAW hazards. Choice (B)

10. Miss time = 10 ns
Hit time = 1 ns
90% are hits.
Average memory access time
= 0.9 * 1 + 0.1 * 10
= 0.9 + 1 = 1.9 ns. Choice (C)

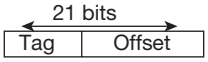
11.

	1	2	3	4	5	6	7	8	9	10
I_1	F	D	D	E	E	W				
I_2		F			D	D	E	W	W	
I_3			F				D	E	E	W

$\therefore$ 10 clock cycles required. Choice (B)

12. Choice (A)

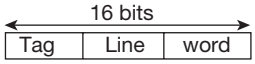
13. RAM size = 2 MB = 2^{21} B



Block size = 16 B = 2^4 B
$\Rightarrow$ offset = 4
$\Rightarrow$ Tag = 21 – 4 = 17. Choice (D)

14. Cache hit requires 2 clock cycles.
Cache miss requires 7 clock cycles.
Average memory access requires 3 clock cycles.
Let hit rate is x, then $3 = x * 2 + (1 - x)7$
$\Rightarrow$ $3 = 2x + 7 - 7x$
$\Rightarrow$ $5x = 4$
$\Rightarrow$ $x = \frac{4}{5} \times 100 = 80\%$ Choice (A)

15. Main memory capacity is 64 K × 16.
It has 16-bit address



Block size = 4 words = 2^2
$\Rightarrow$ word size = 2
Number of lines in cache $= \frac{2^{10}}{2^2} = 2^8$
$\therefore$ line field width = 8
$\Rightarrow$ Tag = 16 – 10 = 6
Each line cache holds
Tag + Data = 6 + 16-bits = 22-bits. Choice (B)

16. Main memory address has 32-bits.

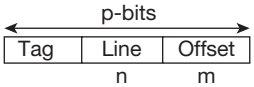
Block size = 4 words = 4 × 4 Bytes = 2^4 B
$\Rightarrow$ offset = 4
Number of blocks in cache = 4 K = 2^{12}
Number of sets $= \frac{2^{12}}{4} = 2^{10}$
$\Rightarrow$ set field width = 10
$\therefore$ Tag = 32 – (10 + 4) = 18
Number of tag bits per set is 18 * 4 = 72 bits.
Choice (C)

17.

	1	2	3	4	5	6	7	8	9
I_1	IF	ID	FO	EX	WB				
I_2		IF	ID	FO	EX	WB			

$\therefore$ number of clock cycles required = 6. Choice (A)

18.



n m
$\Rightarrow$ Tag = $p - (n + m)$ bits. Choice (D)

19. Number of sets = 4096
Number of words = 4 words
Word length = 32-bits = 4 B

$\Rightarrow$ Number of words (in bytes) = 4 * 4 B = 16B
The cache is 2-way set associative.
Cache capacity = 2 * 4096 * 16
$= 2^1 * 2^{12} * 2^4$
$= 2^{17}$ B = 128 KB. Choice (C)

20. Number of blocks = 4096
Number of words per block = 128
Word size = 32 bits = 4 B
Number of words per block
(in bytes) = 128 * 4 B = 512 B
Main memory capacity = 4096 * 512 B
$= 2^{12} * 2^9$B $= 2^{21}$ B
$\therefore$ 21-bits required for main memory address.
Choice (D)

21. Cache size = C bytes
Block size, $B = 2^b$ bytes
The cache is m-way set-associative.

Number of sets in cache $= \frac{C}{M \times B}$

Bits required for set field is $\log_2^{\left(\frac{C}{M} \times 3\right)}$

$= \log_2^C - \log_2^{(M \times B)} = \log_2^C - \log_2^M - \log_2^B$

$= \log_2^C - \log_2^M - \log_2^{2^b}$

$= \log C - \log M - b$. Choice (B)

22. Cycle time = maximum stage delay + latch delay
= 50 + 2 = 52 ns
Latency = number of stages * cycle time
= 5 * 52 = 260 ns. Choice (B)

23.

	1	2	3	4	5	6	7	8	9	10	11
I_1	F	D	E	M	W						
I_2		F	D	E	M	W					
I_3			F		D	E	M	W			
I_4				F		D	E	M	W		
I_5					F		D	E	M	W	
I_6						F		D	E	M	W

One stall caused by 2nd and 3rd instructions.
Choice (B)

24. Given predictor always predicts about the branch 'Taken'.

Prediction	T	T	T	T
Outcome	T	T	NT	T
Result	True	True	False	True

1 out of 4 predictions is wrong.
i.e., Accuracy of predictor $= \frac{3}{4}$
* 100 = 75%. Choice (B)

25. Using 2-bit predictor, the predictor will change its decision with two successive wrong predictions.
Initial prediction: T

Prediction	T	T	T	T
Outcome	T	T	NT	T
Result	True	True	False	True

Accuracy $= \frac{3}{4}$
* 100 = 75%. Choice (B)