Chapter 3

Amplifiers

CHAPTER HIGHLIGHTS

- The r_e Transistor Model
- BJT AC Analysis
- FET as Amplifier
- The Hybrid Equivalent Model
- Frequency Response Analysis of Amplifiers
- Miller's Theorem
- High Frequency Response of an R.C Coupled CE Amplifier
- Multi Stage Amplifiers
- Cascode Connection (CE-CB)
- Darlington Connection
- High Frequency Response of an Amplifier (π model)
- FET Amplifier Stages
- Transconductance
- A.C Equivalent Model of MOS FET

Introduction

The transistors can be employed as an amplifying device, that is, the output AC power is greater than the input power. There is an exchange of DC power to AC domain that power permits by establishing a high output AC power.

The superposition theorem is applicable for the analysis and design of the DC and AC components of a BJT network, permitting the separation of the analysis of the DC and AC responses of the system.

There are three models commonly used in the small signal AC analysis of transistor network:

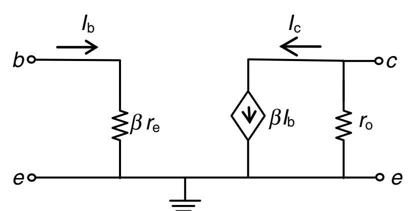
1. r_e model,
2. hybrid π model
3. hybrid equivalent model

The AC equivalent of a network is obtained by:

1. setting all DC sources to zero, and replacing them by a short circuit equivalent.
2. replacing all capacitors by a short circuit equivalent.
3. removing all elements bypassed by short circuit equivalents, introduced in steps 1 and 2.
4. redrawing the network in more convenient and logical form.

r_e Transistor Model

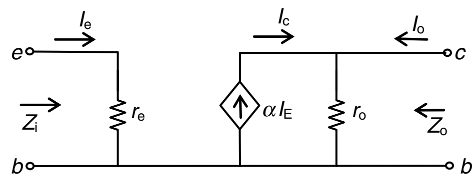
Common Emitter Configuration



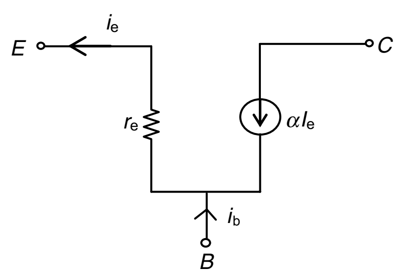
$$r_e = \frac{26\text{mV}}{I_E},\ Z_e = (\beta + 1)\, r_e \simeq \beta r_e$$

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C}$$

Common Base Configuration



$$r_e = \frac{26\text{mV}}{I_E}$$



For common collector configuration, the equivalent is same as common emitter configuration.

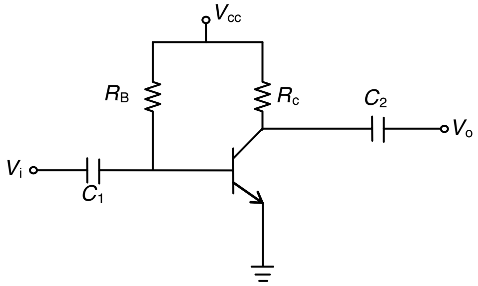
For p–n–p transistor, the direction of currents are reversed:

where r_e is the dynamic emitter resistance $= \frac{26\text{mV}}{I_E}$;

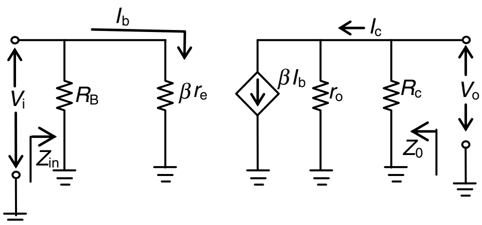
α is the current gain of CB; and β is the current gain of CE

BJT AC Analysis

Common Emitter Fixed Bias Configuration



(1) Common Emitter fixed bias configuration.



$Z_i = R_B \parallel \beta r_e$ Ω input resistance

$Z_i \simeq \beta r_e$ if $R_B \geq 10\beta r_e$

Output Impedance $Z_o = R_C \parallel r_o$

If $r_o \geq 10R_c$ $Z_o \cong R_c$

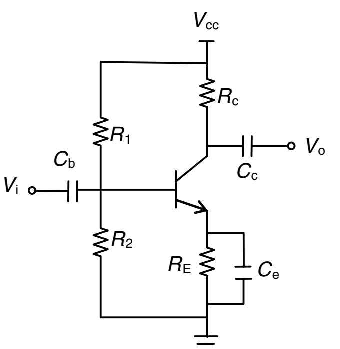
$$V_o = -\beta I_b\,(R_c \parallel r_o),\ I_b = \frac{V_i}{\beta r_e}$$

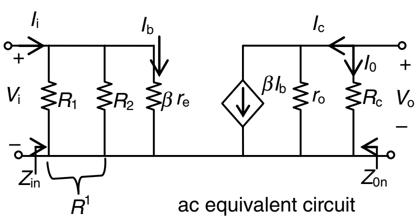
Therefore, $V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_c \parallel r_o)$

$$A_v = \frac{V_o}{V_i} = \frac{-(R_c \parallel r_o)}{r_e} = \frac{-R_c}{r_e};\ r_o \geq 10R_c,\ A_i = \beta$$

The negative sign in the equation A_v reveals that a 180° phase shift occurs between the input and output signals.

Voltage Divider Bias





ac equivalent circuit

For example, $R^1 = \frac{R_1 R_2}{R_1 + R_2} = R_1 \parallel R_2$

Z_i input Impedance $= R^1 \parallel \beta r_e$

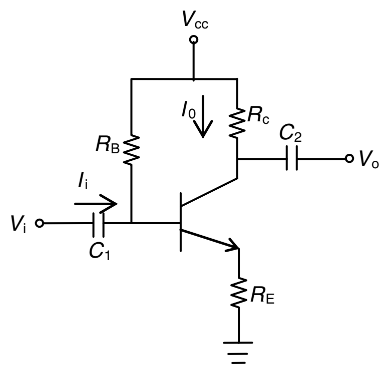
Z_o output Impedance $= R_c \parallel r_o$

$$A_v = \frac{V_o}{V_1} = \frac{-R_c \parallel r_o}{r_e}$$

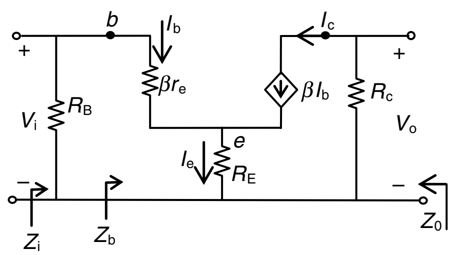
$$\text{if } r_o \geq 10R_c \text{ then } A_v = \frac{-R_c}{r_e}$$

Negative sign reveals a 180° phase shift between V_o and V_i.

Common Emitter, Emitter Bias Configuration



CE, emitter bias configuration



ac equivalent circuit

Applying Kirchhoff's voltage law to the input,

$$V_i = I_B\,\beta\,r_e + I_e R_E = I_B \beta\,r_e + (\beta + 1)\,I_B\,R_E$$

$$Z_b = \frac{V_i}{I_B} = \beta\,r_e + (\beta + 1)\,R_E$$

$$\simeq \beta r_e + \beta R_E = \beta(r_e + R_E)$$

$$\simeq \beta R_E \text{ as } R_E >> r_e$$

Z_i is the input Impedance $(Z_i) = Z_b \parallel R_B = Z_b \parallel R_B$

With V_i set to zero, $I_b = 0$, and βI_b can be replaced by an open circuit equivalent.

Output impedance $Z_o = R_c$

Gain A_v,

$$I_b = \frac{V_i}{Z_b}$$

$$V_o = -I_o R_c = -\beta I_b R_c$$

$$= -\beta\left(\frac{V_i}{Z_b}\right) R_c$$

$$A_v = \frac{V_o}{V_i} = \frac{-\beta R_c}{Z_b}$$

$$Z_b = \beta(r_e + R_E) \text{ gives}$$

$$A_v = \frac{V_o}{V_i} = \frac{-R_c}{r_e + R_E} \simeq \frac{-R_c}{R_E}$$

Effect of r_o:

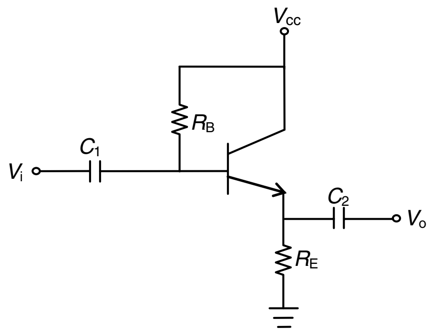
$$Z_b = \beta r_e + (\beta + 1)R_E \simeq \beta(r_e + R_E)$$

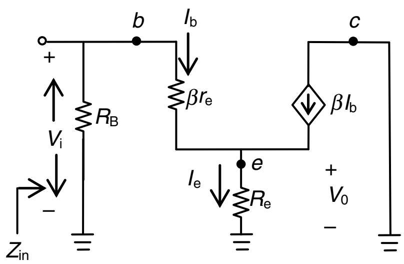
$$r_o \geq 10(R_c + R_E)$$

$$Z_i = Z_b \parallel R_B, \qquad Z_o = R_c, \qquad A_v = \frac{\beta R_c}{Z_b} \qquad r_o \geq 10R_c$$

If R_E is bypassed by a capacitor, the AC circuit will be same as of fixed bias configuration.

Emitter Follower Configuration





AC equivalent circuit

$$Z_i = R_B \parallel Z_b$$

$$Z_b = \beta r_e + (\beta + 1)\, R_E$$

$$Z_b = \beta R_E \qquad\qquad (R_E >> r_e)$$

$$Z_o = R_E \parallel r_e$$

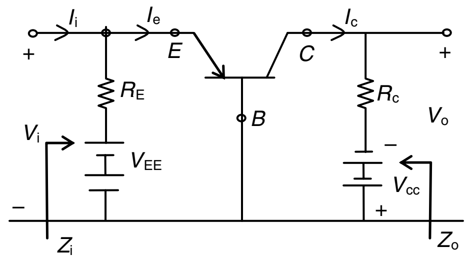
$$Z_o = r_e \qquad\qquad (R_E >> r_e)$$

$$A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e} \simeq \frac{R_E}{R_E} = 1$$

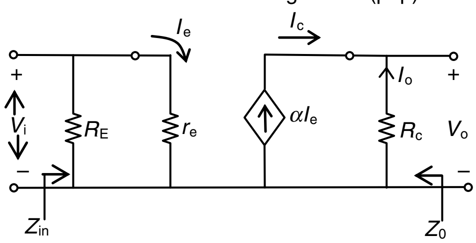
V_o and V_i are in phase for emitter–follower configuration.

Common Base Configuration

The common base configuration is characterized as having relatively low input and a high output impedance and a current gain less than 1. The voltage gain can be quite large.



Common base configuration (pnp)



$$Z_i = R_E \parallel r_e$$

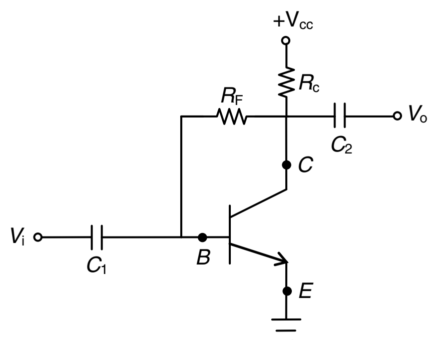
$$Z_o = R_c$$

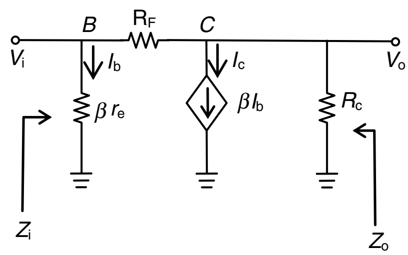
$$A_v = \frac{V_o}{V_i} = \frac{\alpha R_c}{r_e} \simeq \frac{R_c}{r_e}$$

$$A_i = \frac{I_o}{I_i} = -\alpha \simeq -1$$

The fact that A_v is a positive number shows that V_o and V_i are in phase for the common base configuration.

Collector Feedback Configuration





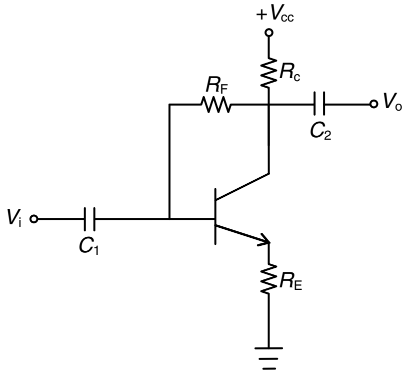
Substituting r_e equivalent circuit into the AC network,

$$Z_i = \frac{r_e}{\frac{1}{\beta} + \frac{R_c}{R_F}}$$

$$Z_o = R_c \parallel R_F$$

$$A_v = \frac{V_o}{V_i} = \frac{-R_c}{r_e}, \qquad A_i = \frac{R_F}{R_c}$$

The negative sign in A_v equation shows 180° phase shift between input V_i and output V_o.



Collector feedback with R_E

$$Z_i = \frac{R_E}{\left[\frac{1}{\beta} + \frac{R_E + R_c}{R_F}\right]}$$

$$Z_o = R_c \parallel R_F$$

$$A_v = \frac{-R_c}{R_E}$$

Determining the Current Gain

$$A_{iL} = -A_{vL} \frac{Z_i}{R_L}$$

Effect of R_L and R_S

The loaded voltage gain of an amplifier is always less than the no-load gain. The gain obtained with a source resistance in place will always be less than that obtained under loaded or unloaded conditions.

For the same configuration,

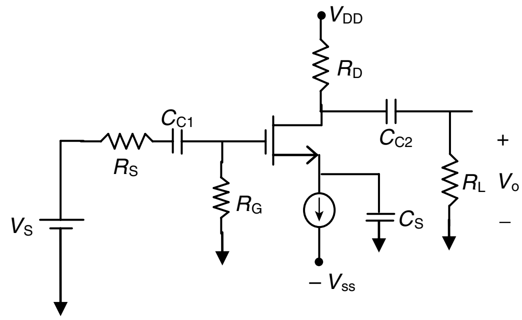
$$A_{v\,\text{noload}} > A_{v\,\text{load}} > A_{v\,\text{Load and Source}}$$

For a particular design, the larger the level of R_L the greater is the level of AC gain.

For a particular amplifier, the smaller the internal resistance of the signal source, the greater is the overall gain.

FET as Amplifier

In most of the MOSFET amplifier circuit application, we use common source configuration.



where C_{C1} and C_{C2} are coupling capacitors and C_S is bypass capacitor

$$R_{in} = R_G,\ R_{out} = (r_o // R_D)$$

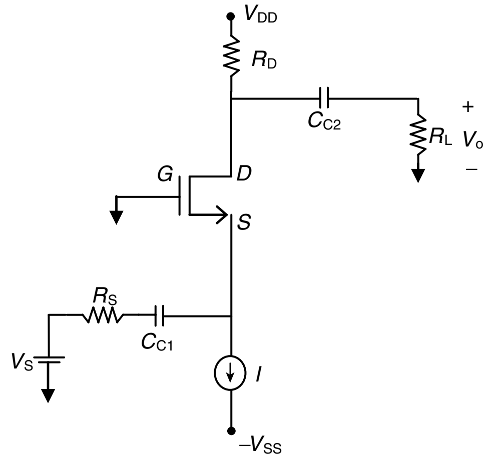
Voltage gain $A_V = -g_m\,(r_o // R_D)$

r_o is the resistance between the drain and the source and g_m is transconductance.

Common source amplifier has moderately high voltage gain and high input and output impedance.

Common Gate Amplifier

In this configuration, gate is grounded, and input is applied to the source and output is taken at drain.



Common-gate amplifier

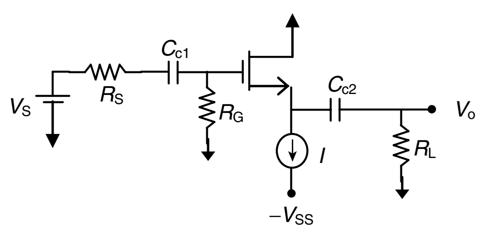
Input resistance $R_{in} = 1/g_m$

Output voltage $R_{out} = R_o$

Voltage gain $A_V = g_m\,(R_D // R_L)$

Input resistance of common gate amplifier is low, while compared with that of the common source amplifier.

Common Drain or Source-Follower Amplifier



Input is applied to gate terminal and output is taken at drain terminal.

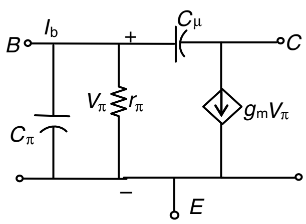
$$\text{Input Impedance } R_{in} = R_G$$

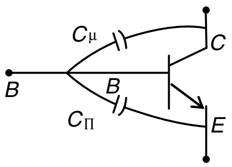
$$\text{Voltage gain } A_v = \frac{R_L // r_0}{(R_L // r_0) + \frac{1}{g_m}}$$

$$\text{Output impedance } R_{out} = \left(\frac{1}{g_m} // r_0\right)$$

1. Source follower amplifier has less than but nearly equal to unity voltage gain and it has very high input resistance and low resistance.
2. This configuration is used as a load in multistage amplifier.

π-Model



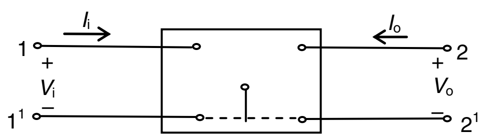


$C\pi$ is the forward-biased diffusion capacitance and C_μ is the reverse-biased diffusion capacitance.

$$r\pi = \beta r_e$$

$$g_m = \frac{1}{r_e}$$

Hybrid Equivalent Model



$$V_i = h_{11} I_i + h_{12} V_o$$

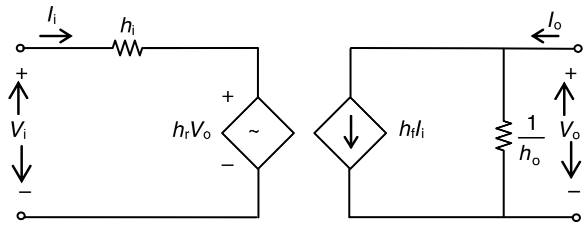
$$I_o = h_{21} I_i + h_{22} V_o$$

h_{11} is the input resistance and $h_i = \left.\frac{V_i}{I_i}\right|_{V_0=0}$ ohm

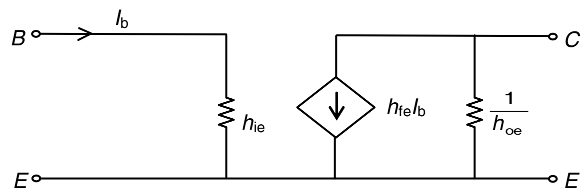
h_{12} is the reverse transfer voltage ratio and $h_r = \left.\frac{V_i}{I_i}\right|^{o}_{V_0=0}$

h_{21} is the forward transfer current ratio and $h_f = \left.\frac{I_o}{I_i}\right|_{V_o=0}$

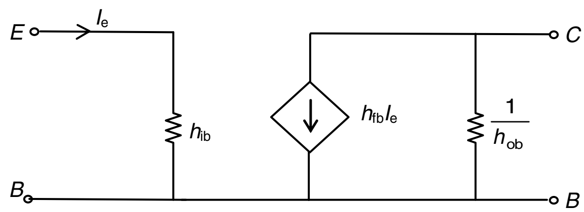
h_{22} is the output conductance and $h_o = \left.\frac{I_o}{V_o}\right|_{I_i=0}$ Siemens



For common emitter circuit $h_{ie} = \beta r_e$, $h_{fe} = \beta_{ac}$
For common base circuit $h_{ib} = r_e$, $h_{fb} = -\alpha \sim -1$

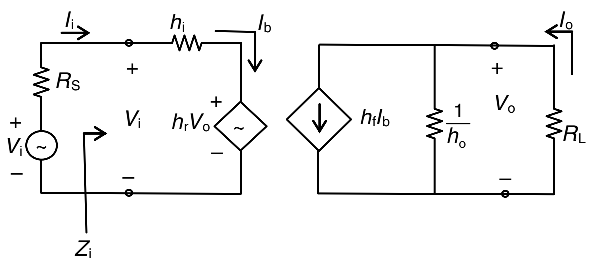


Approximate common emitter hybrid equivalent circuit



Approximate common base hybrid equivalent circuit

h Parameter Model with R_S and R_L

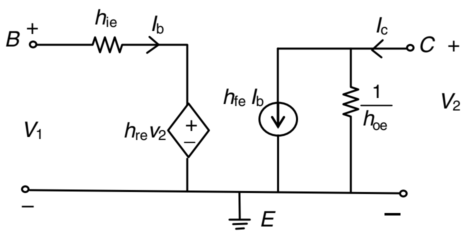


$$\text{Current gain } A_i = \frac{I_o}{I_i} = \frac{h_f}{1 + h_o R_L}$$

$$\text{Voltage gain } A_v = \frac{V_o}{V_i} = \frac{-h_f R_L}{h_i + (h_i h_o - h_f h_r) R_L}$$

$$Z_i = h_i - \frac{h_f h_r R_L}{1 + h_o R_L}, \quad Z_o = \frac{1}{h_o - [h_f h_r / (h_i + R_S)]}$$

Hybrid *h* Parameter Model for Common Emitter



Typical values of h parameters for CE configuration are as follows:

$$h_{ie} = 3.5\ \text{k}\Omega$$

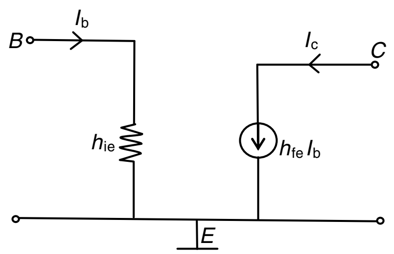
$$h_{re} = 1.3 \times 10^{-4}$$

$$h_{fe} = 120$$

$$h_{oe} = 8.5\ \mu\text{s}$$

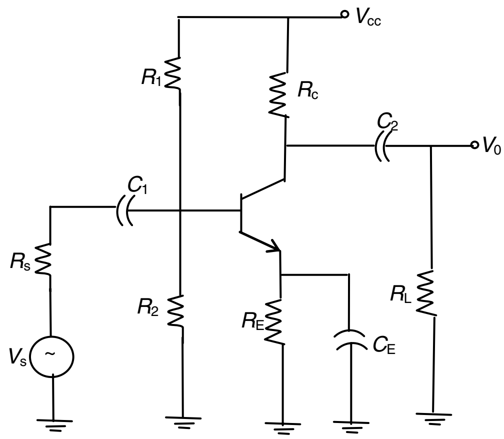
$$\Rightarrow \frac{1}{h_{0e}} = 0.12\ \text{m}\Omega$$

Simplified 'h' parameters model: (CE n–p–n configuration)



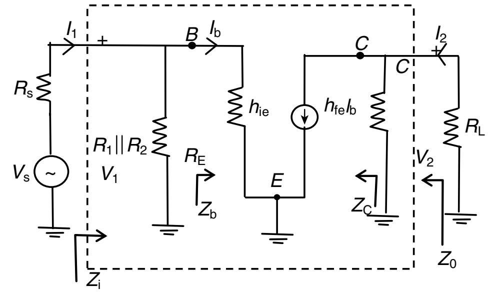
For p–n–p transistor, the direction of current is reversed in the equivalent circuit.

R.C-coupled CE Amplifier



Small signal analysis using simplified h parameter model:

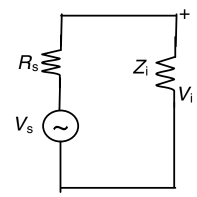
1. Make all the DC sources to zero.
2. Replace the coupling capacitors with short

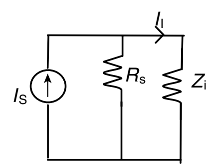


(Equivalent circuit without considering R_E)

Without R_E	Considering R_E
(i) $Z_b = h_{ie}$	(i) $Z_b = h_{ie} + (1 + h_{fe})\,R_E$
(ii) $Z_i = h_{ie}\ \|\|R_1\ \|\|R_2$	(ii) $Z_i = Z_b\ \|\|R_1\ \|\|R_2$
(iii) $Z_c = \frac{1}{h_{oe}}$	(iii) $Z_c = \left(\frac{1}{h_{oe}}\right)$
(iv) $Z_0 = \left(\frac{1}{h_{oe}}\right)$	(iv) $Z_0 = \left(\frac{1}{h_{oe}}\right) \|\| R_c \|\| R_L$
(v) $A_v = \frac{-h_{fe}R_c}{h_{ie}}$	(v) $A_v = \frac{(R_c \|\| R_2)}{r_e}$

Voltage gain and current gain by taking source into consideration:





$$A_{VS} = \frac{V_0}{V_s} = \frac{V_0}{V_1} \times \frac{V_1}{V_s} \qquad A_{IS} = \frac{I_0}{I_S} = \frac{I_0}{I_1} \times \frac{I_1}{I_S}$$

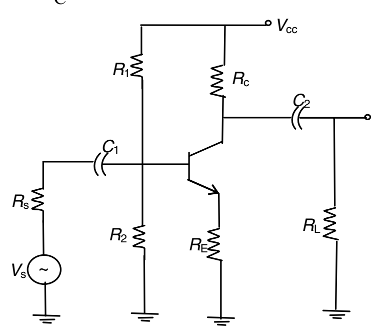
$$A_{VS} = \frac{A_V Z_i}{R_S + Zi} \qquad A_{IS} = \frac{A_I R_S}{R_S + Z_i}$$

Solved Examples

Example 1

Determine A_V, A_I, A_{VS}, A_{IS}, Z_i, Z_0 for the following amplifier circuit

$C_1 = 10\ \mu\text{F}$ $R_1 = 40\ \text{k}\Omega$ $R_L = 2.2\ \text{k}\Omega$
$C_E = 20\ \mu\text{F}$ $R_2 = 10\text{k}\Omega$ $\beta = 100$
$C_C = 1\ \mu\text{F}$ $R_E = 2\ \text{k}\Omega$ $C_{CC} = 20$ v
$R_2 = 1\text{k}\Omega$ $R_C = 4\ \text{k}\Omega$



Solution

(i) $A_V = \dfrac{-(R_C \parallel R_L)}{r_e}$

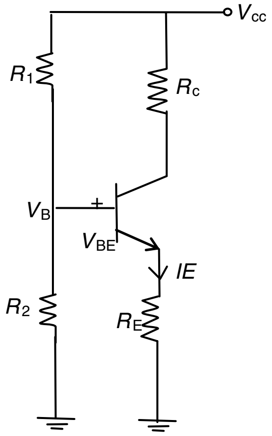
determining 'r_e':

$$r_e = \frac{26\text{mv}}{I_E}$$

Therefore, DC equivalent circuit is needed to calculate I_E.

DC Equivalent Circuit

1. Make AC sources short
2. Replace coupling capacitors with open



By applying KVL at input side gives

$$V_B - V_{BE} - I_E R_E = 0$$

$$I_E = \frac{V_B - V_{BE}}{R_E}$$

$$V_B = \frac{4 - 0.7}{2\text{k}\Omega} = 1.65 \text{ mA}$$

$$r_e = \frac{26\text{mv}}{I_E} = 15.76 \text{ ohms}$$

$$A_V = -\frac{(R_C \parallel R_L)}{r_e} = -90$$

(ii) $A_I = \beta = 100$

(iii) $A_{VS} = \dfrac{A_V Z_i}{R_S + Z_i}$

$$Z_i = Z_b \parallel R_1 \parallel R_2$$

$$Z_b = h_{ie} = \beta r_e = 15.76 \text{ k}\Omega$$

$$Z_i = 1.32 \text{ k}\Omega$$

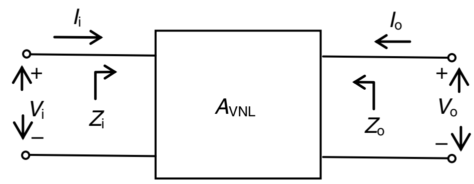
$$A_{VS} = \frac{-90.(1.32\text{k}\Omega)}{(2.32\text{k}\Omega)} = -51.21$$

(iv) $A_{IS} = \dfrac{A_I R_S}{R_S + Z_i} = \dfrac{100 \times 1\text{k}\Omega}{2.32\text{k}\Omega}$

$$A_{IS} = 43.103$$

(v) $Z_0 \times R_C = 4 \text{ k}\Omega$

Two-port Systems Approach

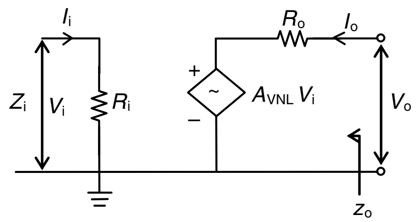


If we take a Thevenin look at the output terminals, we find V_i set to zero:

$$Z_{th} = Z_o = R_o$$

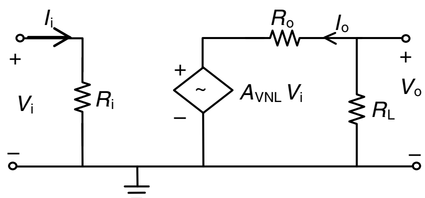
E_{th} is the open circuit voltage between the output terminals identified as V_o.

$$A_{VNL} = \frac{V_o}{V_i}, \quad V_o = A_{VNL} V_i = E_{th}$$



Substituting the internal elements for two-port network.

Applying a Load to the Two-port Network System

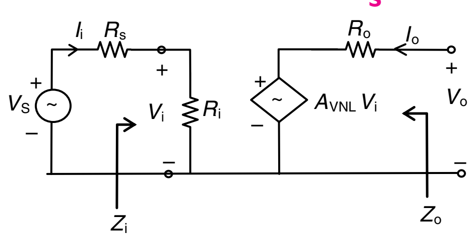


$$V_o = \frac{R_L}{R_L + R_o} \cdot A_{VNL} V_i$$

$$A_{VL} = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o} \cdot A_{VNL}$$

$$A_{iL} = -A_{VL} \cdot \frac{Z_i}{R_L}$$

Effects of Source Resistance R_S



The parameters Z_i and A_{VNL} of a two-port system are unaffected by the internal resistance of the applied source, and the output impedance may be affected by the magnitude of R_S.

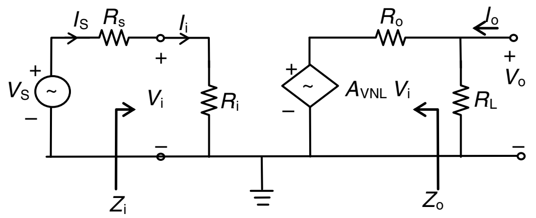
$$V_i = \frac{R_i}{R_i + R_S} \cdot V_S$$

$$V_o = A_{VNL} \cdot V_i$$

$$= A_{VNL} \frac{R_i}{R_i + R_s} . V_S$$

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_i}{R_i + R_S} \cdot A_{VNL}$$

Effects of R_s and R_L



$$V_i = \frac{R_i}{R_i + R_S} \cdot V_S, \qquad V_o = \frac{R_L}{R_L + R_o} A_{VNL} V_i$$

$$A_{VL} = \frac{V_o}{V_i} = \frac{R_L . A_{VNL}}{R_L + R_o}$$

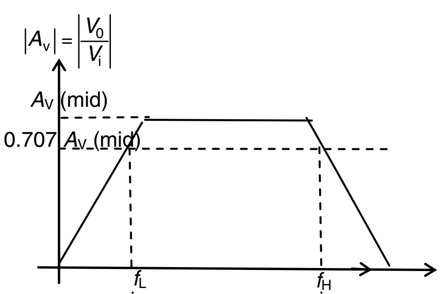
$$A_{VS} = \frac{V_o}{V_S} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_S} = \frac{R_i}{R_i + R_S} \cdot \frac{R_L}{R_L + R_o} \cdot A_{VNL}$$

$$A_{iL} = -A_{VL} \cdot \frac{R_i}{R_L} \text{ as } I_i = \frac{V_i}{R_i}$$

$$I_S = \frac{V_S}{R_S + R_i}$$

$$A_{iS} = -A_{VS} \frac{R_S + R_i}{R_L}$$

Frequency Response Analysis of Amplifiers

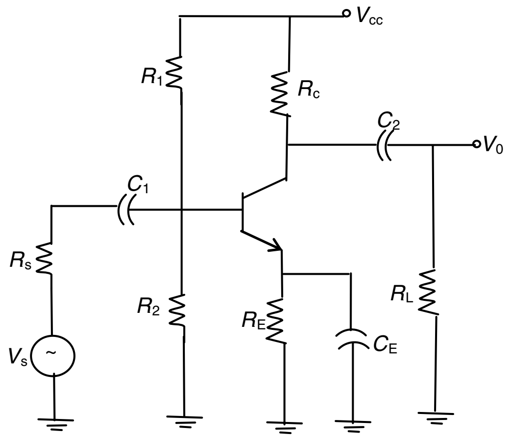


Frequency range	Coupling and bypass capacitor	Parasitic capacitance
Low	Consider	Open
Mid	Short	Open
High	Short	Consider

$A_{V(mid)}$ = mid-band gain of the amplifier

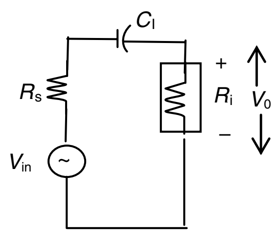
Bandwidth $= f_H - f_L$

Low frequency Response of an R.C-coupled CE Amplifier

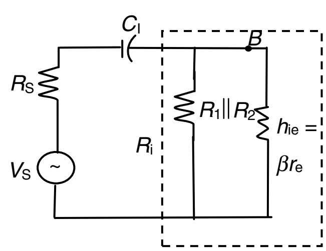


Low frequency response depends on C_1, C_2, and C_E

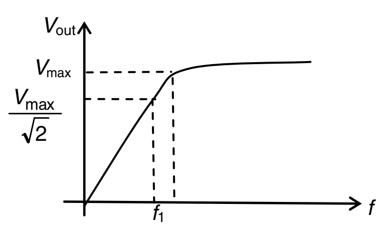
Due to C_1, we get



AC Equivalent Network



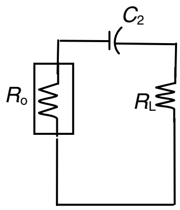
Frequency Response due to C_I

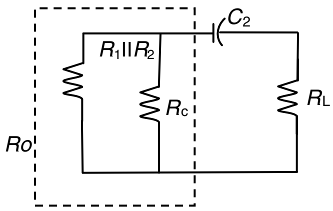


$$f_1 = \frac{1}{2\pi(R_s + R_i)C_1}$$

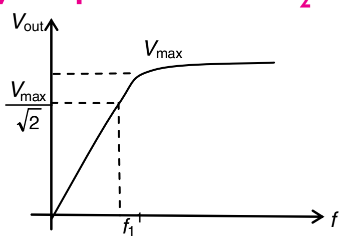
where $R_i = R_1 \,||\, R_2 \,||\, \beta r_e$

Due to C_2, we get





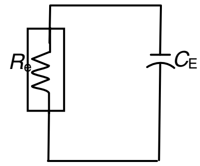
Frequency Response due to C_2



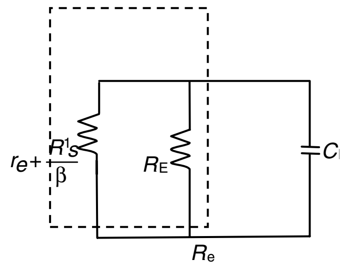
$$f_1^{\,1} = \frac{1}{2\pi(R_s + R_i)C_2}$$

where $R_0 = r_0 \,\alpha\, R_C$

Due to C_E, we get



AC Equivalent Network

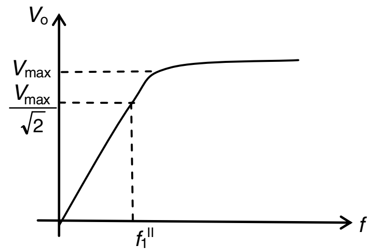


$$f_1^{||} = \frac{1}{2\pi R_e C_E}$$

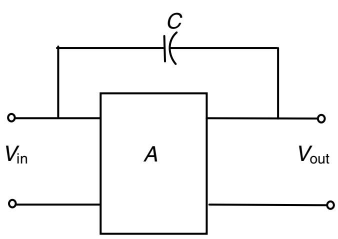
$$\text{where } R_e = R_E \,||\, \left(r_e + \frac{R^1 S}{\beta}\right),$$

$$R_S^{\,1} = R_S \,||\, R_1 \,||\, R_2$$

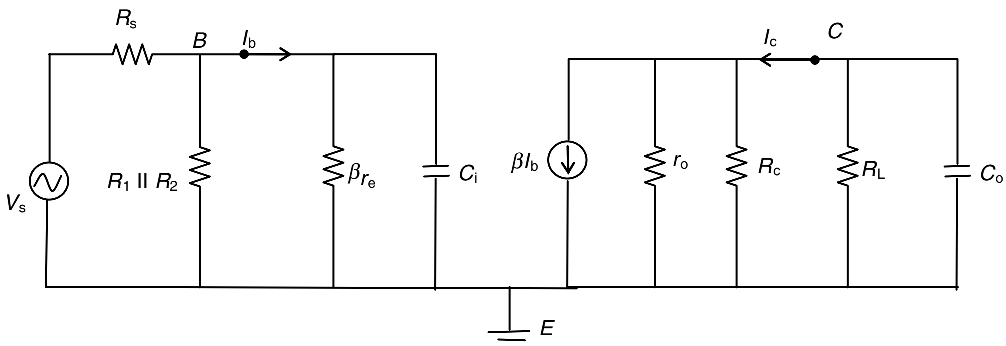
Frequency Response

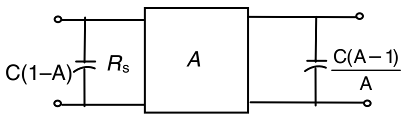


Miller's Theorem



AC equivalent network:



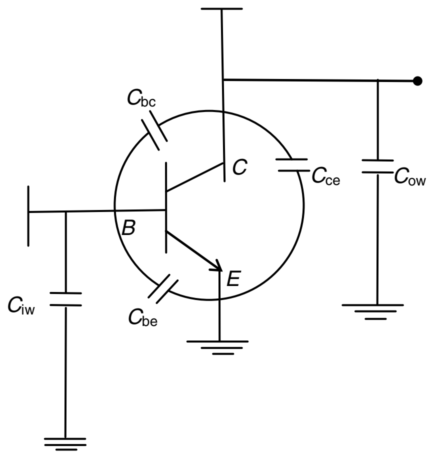


C_{iw} and C_{ow} is the wiring (stray) capacitance; C_{bc} is the miller capacitance; and C_{be}, C_{ce} are the junction capacitance or parasitic capacitance.

$$C_{in}\text{ (miller)} = C(1 - A)$$

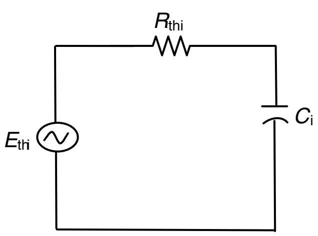
$$C_{out}\text{ (miller)} = \frac{C(A-1)}{A}$$

High Frequency Response of an RC-coupled CE Amplifier



Thevenin's Circuit

Input Side

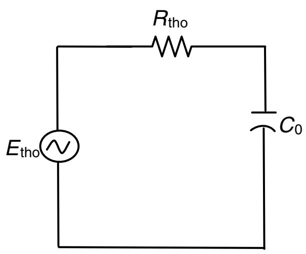


$$f_i = \frac{1}{2\pi R_{thi} C_i}$$

$$R_{thi} = R_S \,||\, R_1 \,||\, R_2 \,||\, \beta r_e$$

$$C_i = C_{wirei} + C_{be} + (1 - A)\, C_{bc}$$

Output Side



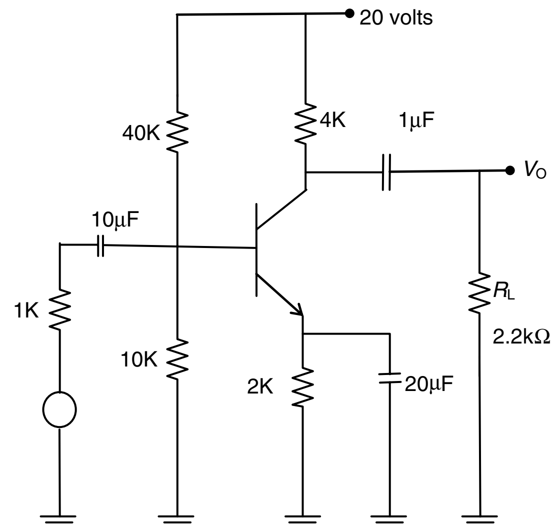
$$F_0 = \frac{1}{2\pi R_{tho} C_0}$$

$$R_{tho} = r_0 \,||\, R_C \,||\, R_L$$

$$C_0 = C_{wireo} + C_{ce} + C_{bc}\frac{(A-1)}{A}$$

Example 2

Determine the lower cut-off frequency for the circuit given $\beta = 100$ and $r_0 = \infty\ \Omega$



(A) 6.86 Hz (B) 25.68 Hz (C) 327 Hz (D) 350 Hz

Solution

Determining 'r_e'

$$r_e = \frac{26\text{mv}}{I_E}$$

$$R_e = 15.76\ \Omega \text{ (refer GE04557)}$$

$$\beta r_e = 1.576\ \text{k}\Omega$$

$$\text{Mid-band gain } A_V = \frac{-(R_C \,||\, R_L)}{r_e}$$

$$A_V = -90$$

$$R_i = R_1 \,||\, R_2 \,||\, \beta r_e = 1.32\ \text{k}\Omega$$

$$R_s^{1} = R_s \,||\, R_1 \,||\, R_2 = 0.889\ \text{k}\Omega$$

$$R_e = R_E \,||\left(\frac{Rs^1}{\beta} + r_e\right) = 24.35\ \Omega$$

$$f_1 = \frac{1}{2\pi(R_s + R_i)C_1} = 6.86\ \text{Hz}$$

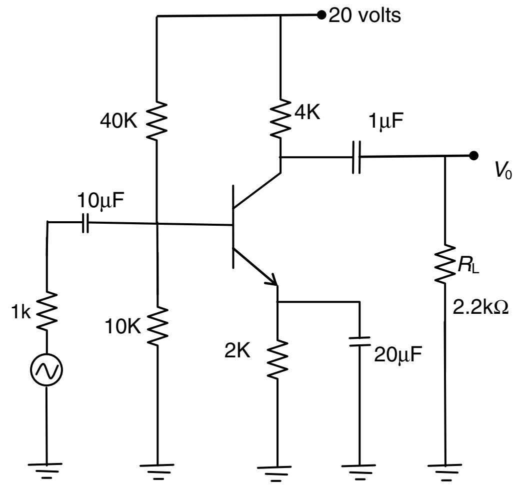
$$f_1^{\,1} = \frac{1}{2\pi(R_C + R_L)C_2} = 25.86\ \text{Hz}$$

$$f_1^{\,\alpha} = \frac{1}{2\pi R_E C_E} = 327\ \text{Hz}$$

∴ Dominant lower – cut-off frequency = 327 Hz (Highest).

Example 3

Determine the higher cut off frequency for the given circuit given $\beta = 100$, $r_0 = \infty\ \Omega$ $V_{cc} = 20$ v, $C_{be} = 36$ pF, $C_{bc} = 4$ pF $C_{ce} = 1$ pF, $C_{wi} = 6$ pF, $C_{wo} = 8$ pF



(A) 738.24 kHz (B) 8.6 MHz
(C) 10 MHz (D) 800 kHz

Solution

$$R_{thi} = R_s \parallel R_1 \parallel R_2 \parallel \beta r_e$$

$$r_e = 1.32\ k\Omega$$

$$R_{thi} = 0.531\ k\Omega$$

$$C_i = C_{wirei} + C_{be} + (1 - A)\, C_{bc}$$

$$A = -90 \text{ (refer GE04557)}$$

$$C_i = 406 \text{ pF}$$

$$R_{tho} = R_c \parallel R_L = 1.419\ k\Omega$$

$$C_0 = C_{wo} + C_{ce} + C_{bc}\frac{(A-1)}{A} = 13.04 \text{ pF}$$

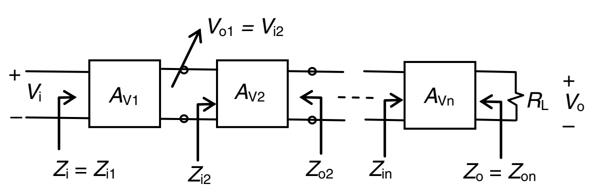
$$f_i = \frac{1}{2\pi R_{thi} RC_i} = 738.24 \text{ kHz}$$

$$f_0 = \frac{1}{2\pi R_{tho} RC_0} = 8.6 \text{ MHz}$$

Higher cut-off frequency is 738.24 kHz (lowest).

Multistage Amplifiers

Cascaded Systems



The two-port systems approach is partially useful for cascaded systems such as that appearing in the figure, where A_{v1}, A_{v2} .... A_{vn} are voltage gains of each stage, under loaded conditions, that is, A_{v1} is determined with the input impedance to A_{v2} acting as load on A_{v1}.

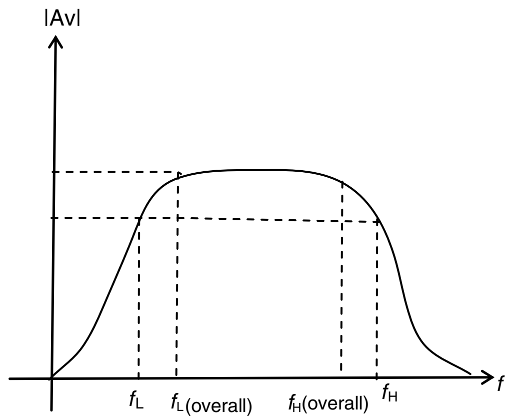
The total gain of the system is the product of individual gains.

$A_v = A_{v1} \cdot A_{v2} \cdot A_{v3}$ ..... A_{vn} and total current gain is $A_i = -A_v \dfrac{Z_i}{R_L}$

Effect of cascading on frequency response:

1. Gain is multiplied.
2. Bandwidth is reduced.

If n' amplifiers having lower cut-off frequency of f_L and the highest cut-off frequency of f_H, then the frequency response is given in the following figure.



$$f_L(\text{overall}) = \frac{f_L}{\sqrt{2^{\frac{1}{n}} - 1}}$$

$$f_h\,(\text{overall}) = f_H\sqrt{2^{\frac{1}{n}} - 1}$$

where f_L and f_H are the lower and higher cut-off frequencies of the individual amplifier stages.

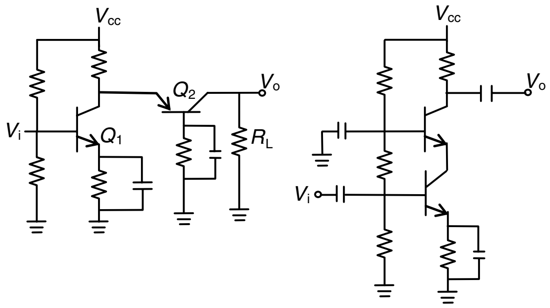
RC-coupled BJT Amplifier

The name is derived from the capacitive coupling (capacitor (C_C)) and the fact that the load on first stage is on RC combination. The coupling capacitor isolates the two stages from a DC point of view, but acts as short circuit equivalent for the AC response. The input impedance of second stage acts as load for the first stage.

Cascode connection (CE–CB)

If the collector of the loading transistor is connected to the emitter of the following transistor, it is called as cascode–connection.

The possible configurations are as follows:

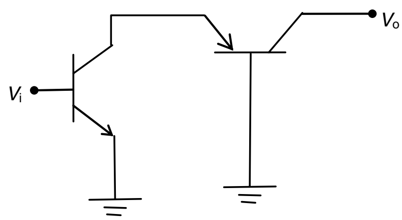


Advantages

1. Larger output impedance
2. Wider bandwidth

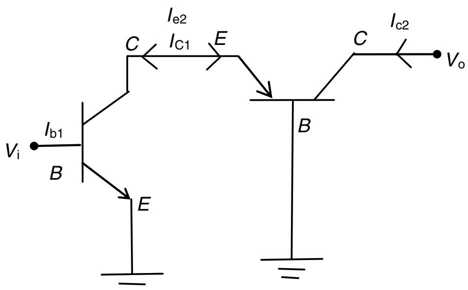
Example 4

For the connection shown in the following figure, find the overall transconductance of the circuit given $g_{m1,}$ is the transconductance of CE amplifier and g_{m2} is the transconductance of CB amplifier.



(A) g_{m2} (2) $g_{m1} \parallel g_{m2}$
(C) g_{m1} (D) $g_{m1} + g_{m2}$

Solution

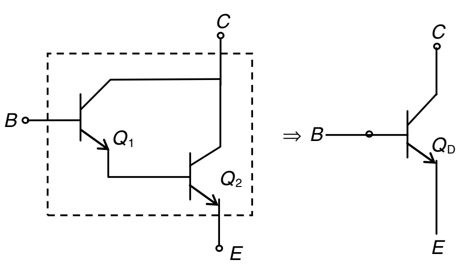


Overall transconductance = $\dfrac{I_{c2}}{V_i}$

$$I_{C2} = I_{e2} = I_{C1}$$

$$\therefore g_m \text{ (overall)} = \frac{I_{c1}}{V_i} = g_{m1}$$

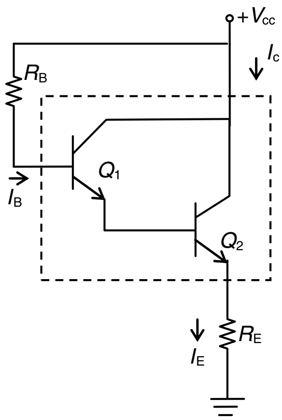
Darlington Connection



The main feature of the Darlington connection is that the composite transistor acts as a single unit with a current gain that is product of the current gains of the individual transistors.

$$\beta_D = \beta_1 \cdot \beta_2$$

A Darlington transistor connection provides a transistor having a very large current gain typically a few thousand and high input resistance.



DC bias

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta_D R_E}$$

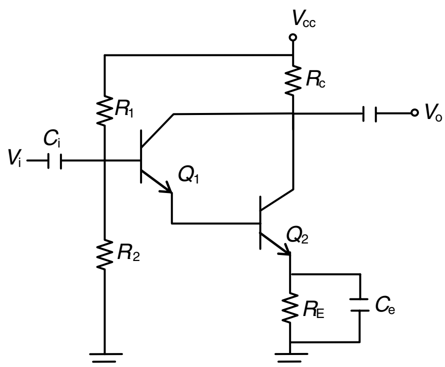
$$I_E = (\beta_D + 1)\, I_B$$

AC analysis

$$Z_i = R_B \parallel \beta_1\, \beta_2\, R_E,\; A_i = \frac{\beta_D R_E}{R_B + \beta_D R_E}$$

$$A_v \cong 1, \qquad Z_o = \frac{r_{e1}}{\beta_2} + r_{e2}$$

where R_E is bypassed and output taken at collector.



$$Z_i = R_1 \parallel R_2 \parallel \beta_1\,(r_{e1} + \beta_D\, r_{e2})$$

$$A_i = \frac{\beta_D (R_1 \parallel R_2)}{R_1 \parallel R_2 + Z_i^1}$$

where $Z_i^1 = \beta(r_{e1} + \beta_2 r_{e2})$

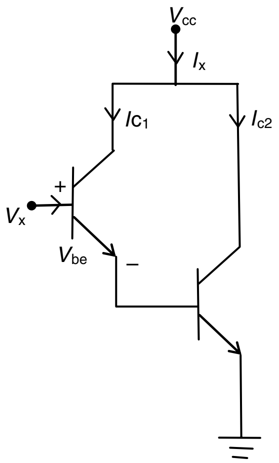
$$Z_o = R_C \parallel r_{o2}$$

$$A_v = \frac{V_o}{V_i} = \frac{\beta_D R_C}{Z_i^1}$$

Example 5

Given the transconductance of Q_1 is g_{m1} and Q_2 is g_{m2}.

Find the overall transconductance $\frac{I_x}{V_x}$ (β is large)



(A) g_{m1} (B) $0.5\ g_{m2}$ (C) $0.5\ g_{m1}$ (D) g_{m2}

Solution

$$I_x = I_{c1} + I_{c2}$$

$$I_{c2} \sim I_{E2} = (\beta + 1)\ I_{E1}$$

$$I_{c2} \sim (\beta + 1)\ I_{c1}$$

$$I_{c2} \sim (\beta + 1)^2\ I_{b1}$$

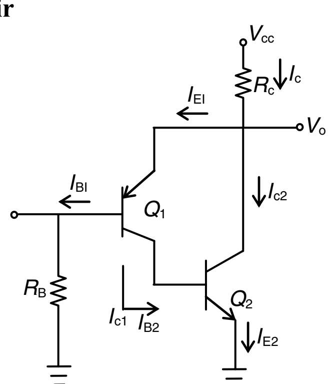
as 'β' is large $I_{c2} >> I_{c1}$

$\therefore I_x \sim I_{c2}$

$$V_x = 2V_{be} \text{ (KVL at input)}$$

$$\frac{I_x}{V_x} = \frac{I_{c2}}{2V_{be}} = 0.5\ g_{m2}$$

Feedback pair



DC analysis

$$I_{BI} = \frac{V_{cc} - V_{BEI}}{R_B + \beta_D R_C}$$

$$I_c \simeq I_{c2}$$

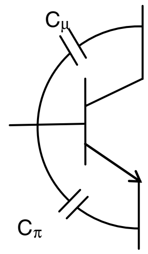
AC analysis

$$Z_i^1 = \beta_1\ \beta_2\ R_c,\ Z_i = R_B \parallel Z_i^1$$

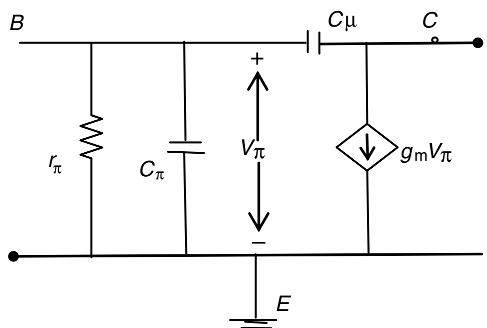
$$A_i = \frac{I_o}{I_i} = \frac{-\beta_1 \beta_2 R_B}{R_B + \beta_1 \beta_2 R_c}$$

$$A_v = \frac{\beta_2 R_c}{r_{e1} + \beta_2 R_c} \simeq 1, \qquad Z_o = \frac{r_{e1}}{\beta_2}$$

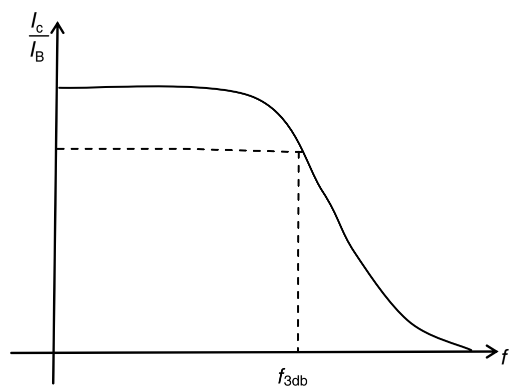
High Frequency Response of an Amplifier (π Model)



AC equivalent Circuit:



Frequency Response:



f_T is the unity gain *f*requency.

$$f_{3dB} = \text{3-dB } f\text{requency}$$

$$f_{3dB} = \frac{1}{2\pi r_\pi (C_\pi + C_\mu)}$$

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$$

$$\frac{f_T}{f_{3dB}} = g_m r_\pi = h_{fe}$$

Example 6

An amplifier has a gain of 60 dB with a bandwidth of 10 MHz. Find the unity gain frequency.

(A) 10 GHz (B) 100 GHz
(C) 10 MHz (D) 100 MHz

Solution

$$\text{Gain} = A_{\text{in}}\ \text{dB} = 60$$

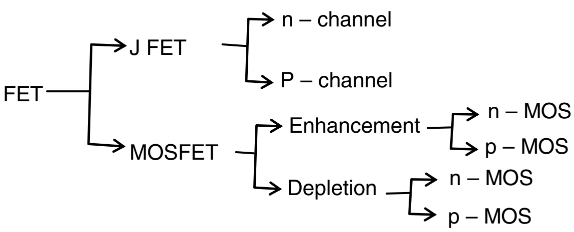
$$20 \log A = 60$$

$$\Rightarrow A = 10^3 = 1{,}000$$

$$f_T = (1{,}000)\ (10 \times 10^6)$$

$$f_T = 10\ \text{GHz}$$

FET Amplifier Stages



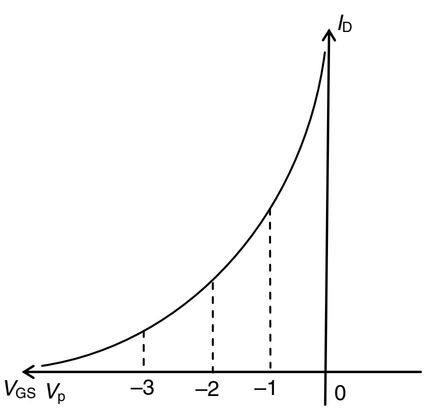
For JFET and depletion mode MOSFET analysis, Shockley's equation holds good

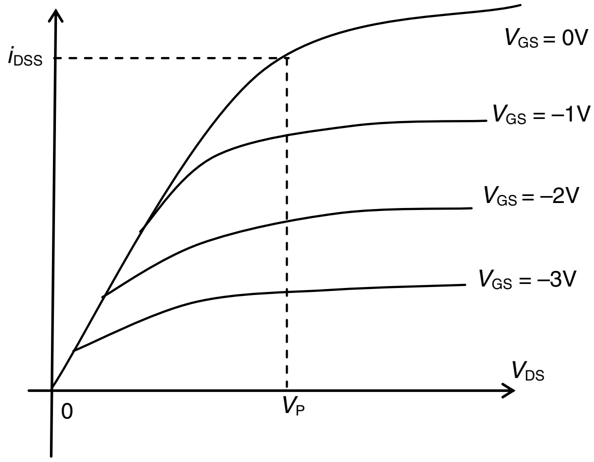
$$\text{i.e., } I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 = \text{Source Current}$$

where I_D is the drain current $= I_S$; I_{DSS} is the drain saturation current; and V_P is the pinch-off voltage where $I_D = 0$ A.

J-FET Transfer characteristics

Output characteristics:





Enhancement Mode MOSFET Analysis

$$i_D = K(V_{GS} - V_T)^2$$

i_D is the instantaneous drain current;
V_{GS} is the instantaneous gate–source voltage;
and V_T is the threshold voltage.

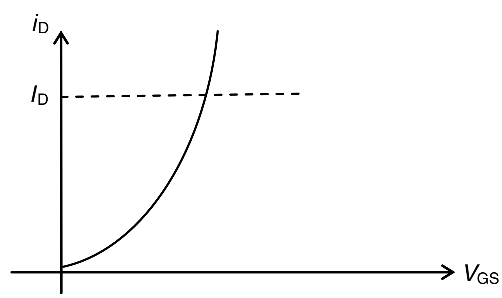
Symbols used to represent DC, AC, and instantaneous values:

1. I_d = AC drain current
2. I_D = DC drain current
3. i_D = instantaneous drain current $= I_D + i_d$

Region of Operation

Case (i): $V_{GS} < V_T$: cut-off region
Case (ii): $V_{GS} > V_T$ and $V_{DS} < (V_{GS} - V_T)$: linear and triode region
Case (iii): $V_{GS} > V_T$ and $V_{DS} \geq (V_{GS} - V_T)$: saturation region
Case (iv): $V_{GS} > V_T$ and $V_{DS} \geq 2(V_{GS} - V_T)$: breakdown region

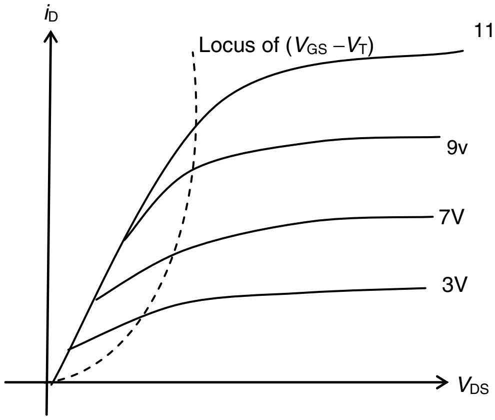
Transfer Characteristics



$$\text{Slope} = g_m = \frac{\Delta i_d}{\Delta V_{gs}}\Big|_{V_{GSQ}}$$

g_m is the transconductance.

Output Characteristics



$$\text{Slope} = r_D = \left(\frac{di_D}{dv_{DS}}\right)^{-1} \Big| V_{GS} = V_{GSQ}$$

where r_D is the drain resistance.

Transconductance (g_m)

(i) $i_D = k(V_{GS} - V_T)^2$

$i_D = I_D + i_d$

$v_{GS} = V_{GS} + V_{gs}$

$i_d = 2k_n (V_{GS} - V_T)$ at V_{GSQ}

where $k_n = \mu_n C_{ox} \left(\frac{W}{L}\right)$ represents MOSFET fabrication constant.

$$g_m = 2k_n \sqrt{\frac{i_D}{k_n}}$$

$$g_m = 2\sqrt{k_n I_{DQ}}$$

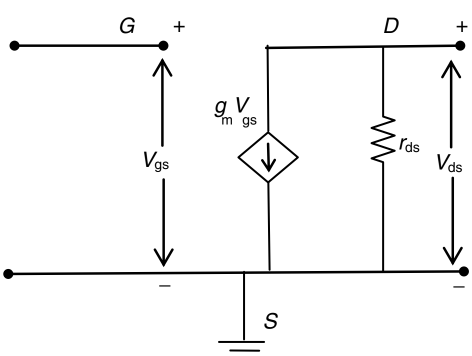
AC Equivalent Model of MOSFET

$$i_d = f(V_{gs}, V_{ds})$$

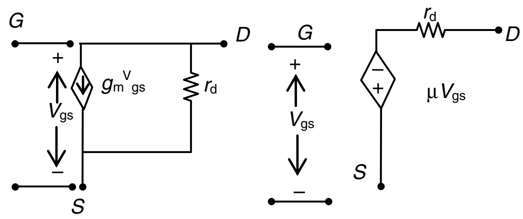
by superposition theorem

$$i_d = g_m V_{gs} + \frac{V_{ds}}{r_{ds}}$$

where g_m is the transconductance and r_{ds} is the drain resistance.



Small Signal Equivalent Circuits



$$\mu = g_m r_d$$

$$g_m = \frac{2}{|V_P|}\sqrt{I_{DQ}\, I_{DSS}} \quad \text{for JFET}_s$$

$$g_m = 2\sqrt{k\frac{W}{L} I_{DQ}} \quad \text{for MOSFET}_S$$

$$r_d = \frac{1}{\lambda I_{DQ}} = \frac{V_A}{I_{DQ}}$$

The values of both g_m and r_d are bias dependent. The output resistance r_d is usually not sufficiently large, and so it may not be neglected (as r_o is often neglected in the BJT model).

The quantity μ is called amplification factor $\mu = g_m r_d$. The open circuit between gate and source in the model makes $I_g = 0$, and so we consider $A_V R_o$ only (A_I and R_i are very high)

Equations for FET Stages

Common source stage

$$A_v = -\frac{\mu R_D}{r_d + R_D} = \frac{-g_m R_D}{1 + R_D/r_d}$$

$$R_o = r_d,\ R_o^1 = R_D \,||\, r_d$$

Common source stage with source resistance

$$A_v = \frac{\mu R_D}{r_d + R_o + (1+\mu) R_S} = \frac{-g_m (r_o \,||\, R_D)}{1 + g_m R_S R_L / R_D}$$

$$R_o = r_d + R_S(1+\mu) = r_d(1 + g_m R_S)$$

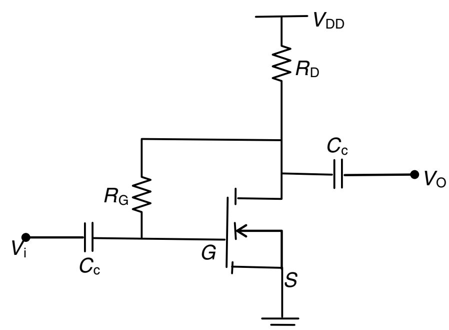
$$R_o^1 = R_o \,||\, R_D$$

Common Drain configuration

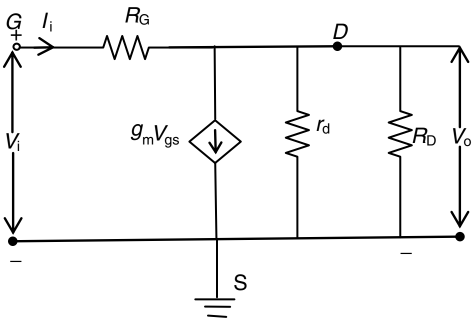
$$A_v = \frac{\mu R_S}{r_d + R_S(1+\mu)} = \frac{g_m R_S}{1 + g_m R_S},\ R_o = \frac{r_d}{1+\mu} = \frac{1}{g_m}$$

$$R_o^1 = R_s \,||\, R_o$$

Enhancement Mode MOSFET Drain Feedback Configuration



AC Equivalent Model:



$r_d = r_{ds}$ = drain resistance

Input Impedance

$$z_i = \frac{R_F + (r_d \,||\, R_D)}{[1 + (r_d \,||\, R_D g_m)]}$$

if $R_F >> (r_d \,||\, R_D)$

$$\Rightarrow z_i = \frac{R_F}{1 + g_m (r_d || R_D)}$$

if $R_F >> (r_d \,||\, R_D)$ and

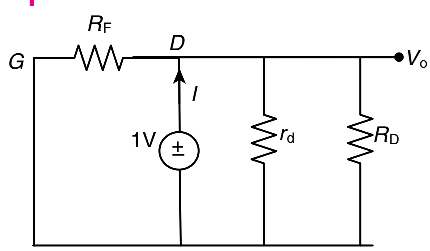
$$\Rightarrow z_i = \frac{R_F}{1 + g_m R_D}$$

$r_d \geq 10R_D$

Output Impedance

1. Make input voltage = 0
2. Connect a voltage source at the output and find $\frac{V}{I}$

AC Equivalent Circuit



$z_0 = R_F \text{ II } r_d \text{ II } R_D$

if $R_F >> (r_d \text{ II } R_D)$ and $r_d \geq 10R_D$

$z_0 \sim R_D$

Voltage Gain

$$A_v = \frac{\left(\frac{1}{R_F}\right) - g_m}{\left(\frac{1}{R_F}\right) + \frac{1}{(r_d \; II \; R_D)}}$$

Approximations:

(i) If $R_F >> (r_d \,||\, R_D)$

$A_V \sim -g_m (r_d \,||\, R_D)$

(ii) if $R_F >> (r_d \,||\, R_D)$ and $r_d \geq 10R_D$

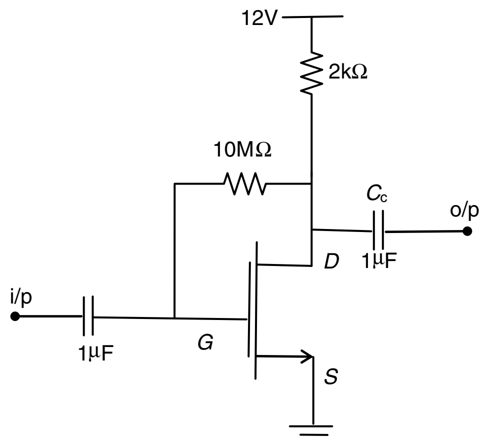
$A_V \sim -g_m R_D$

(iii) $g_m >> \frac{1}{R_F}$, then $A_V = -g_m (r_d \,||\, R_D \,||\, R_F)$

Summary

Without approximation	With approximation
(i) $A_V = -g_m (r_d || R_D)$	(i) $A_V = -g_m R_D$
(ii) $z_i = \frac{R_F}{1 + g_m (r_d || R_D)}$	(ii) $z_i = \frac{R_F}{1 + g_m R_D}$
(iii) $z_0 = r_d \,||\, R_D$	(iii) $z_0 = R_D$

Example 7



Find g_m, r_d, z_i, z_0, A_v.

$K = 0.2 \times 10^{-3}$ A/V^2

$V_T = 3$ v

$Y_d = 20$ μs

$V_{GSQ} = 6.4$ V

$I_{DQ} = 2.75$ mA

Solution

(i) $g_m = 2k(V_{GSQ} - V_T)$

$= 1.632$ mA/V

$g_m = 1.632$ ms

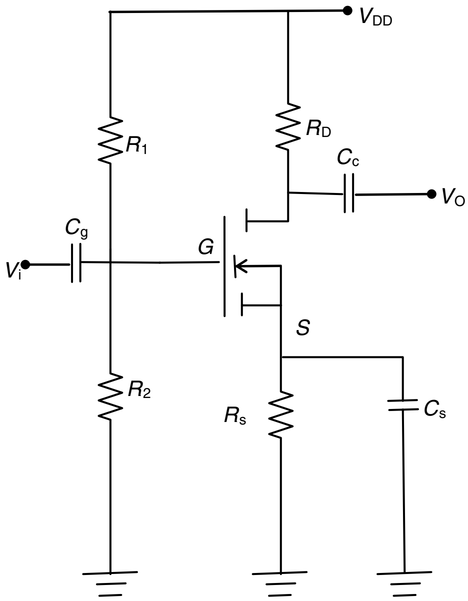
(ii) $r_d = \frac{1}{y_d} = 50$ kΩ

(iii) $z_i = \frac{R_F}{1 + g_m (r_d || R_D)} = 2.42$ mΩ

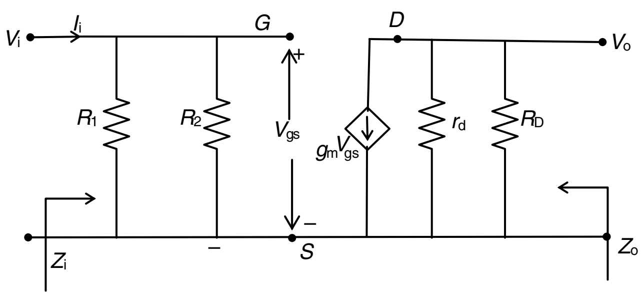
(iv) $z_0 = R_F \,||\, r_d \,||\, R_D = 1.923$ kΩ

(v) $A_v = -g_m(r_d \,||\, R_D \,||\, R_F) = -3.14$

Common Source Amplifier (Voltage Divider Bias)



Amplifier AC Equivalent Model



(i) $z_i = R_1 \parallel R_2$

(ii) $z_0 = r_d \parallel R_D$

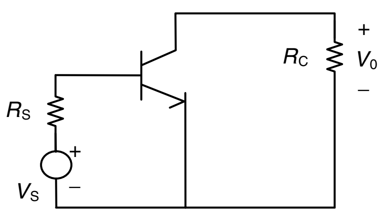
(iii) $A_v = -g_m(r_d \parallel R_D)$

If $r_d >> 10R_D$, then $A_v \simeq -g_m R_D$

Direction for questions 8 to 14: Select the correct alternative from the given choices.

Example 8

The amplifier circuit with $R_S = 500\ \Omega$; $R_C = 1.5\ \text{k}\Omega$ operates at $I_C = 1$ mA, and the parameters are $\beta_0 = 125, f_T = 300$ MHz, and $C_\mu = 0.5$ pF. The mid-band voltage gain is



(A) −51.72 (B) −32.42
(C) −28.34 (D) −13.50

Solution

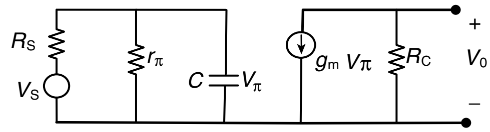
$$g_m = \frac{I_{C(mA)}}{25} = \frac{1}{25}$$

$$\beta_0 = g_m \cdot r_\pi \Rightarrow r_\pi = \frac{\beta_0}{g_m} = \frac{125}{1/25} = 3{,}125\ \Omega$$

$$\omega_T = \frac{g_m}{C_\pi + C\mu} = 2\pi \times 300 \times 10^6$$

$$C_\pi + C_\mu = \frac{g_m}{\omega_T} = \frac{1}{25 \times 2\pi \times 300 \times 10^6} = 21\text{pF}$$

The AC equivalent circuit using unilateral hybrid π.



$$\frac{V_0}{V_1} = g_m R_C$$

$$C = C_x + C_\mu(1 + g_m R_C)$$

$$= C_\pi + C_\mu + C_\mu g_m R_C$$

$$V_\pi = \frac{V_S r_\pi}{R_S + r_\pi} \cdot \frac{1}{1 + \frac{S}{\omega_H}} \quad \text{where } \omega_H = \frac{1}{RC}$$

$$R = R_S \parallel r\pi$$

$$\frac{V_O}{V_S} = \frac{-\beta_0 R_C}{R_S + r_\pi} \cdot \frac{1}{1 + \frac{s}{\omega_H}}$$

$$\text{Mid-band gain } A_0 = \frac{-\beta_0 R_C}{R_S + r_\pi} = \frac{125 \times 1.5}{0.5 + 3.125} = -51.72$$

Example 9

The value of $\omega_H = 2\pi f_H$, which is the upper cut-off frequency in the abovementioned question?

(A) 75.7M rad/s (B) 54.6M rad/s
(C) 39.2M rad/s (D) 32.9M rad/s

Solution

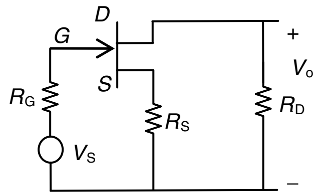
$$C = (C_\pi + C_\mu) + C_\mu g_m R_C$$

$$= 21 + 0.5 \times \frac{1}{25} \times 1500 = 21 + 30 = 51\text{ pF}$$

$$\omega_H = \frac{1}{RC} = \frac{1}{500 \times 51\text{pF}} = 39.2\text{ M rad/s}$$

Example 10

For the common source amplifier with R_S, find the values of $\frac{V_O}{V_S}$ and R_O (output Impedance), given $R_D = 16\ \text{k}\Omega$, $R_S = 1\ \text{k}\Omega$, FET parameters are $r_d = 32\ \text{k}\Omega$ and $\mu = 60$.

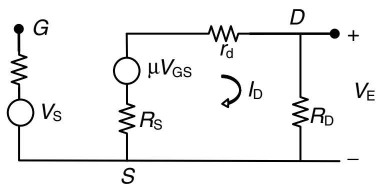


(A) 8.8, 93 kΩ (B) –8.8, 93 kΩ
(C) –4.2, 56 kΩ (D) + 4.2, 56 kΩ

Solution

The equivalent current in the loop equation from KVL

$$I_d\,(R_S + R_D, r_d) = \mu V_{gs}$$
$$V_{gs} = V_s - R_s\, I_d$$
$$V_0 = -\, I_d\, R_D$$



By solving $A_V = \dfrac{V_O}{V_S} = \dfrac{-\mu R_D}{r_d + R_S(1+\mu) + R_D}$

$$R_0 = r_d + R_S\,(1 + \mu)$$

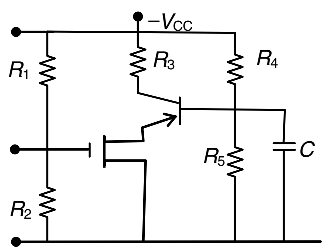
$R_S = 1$ kΩ, $R_D = 16$ kΩ, $r_d = 32$ kΩ, $\mu = 60$

$$A_V = -8.8$$
$$R_O = 32 + 1 \text{ x } 61 = 93 \text{ k}\Omega$$

Example 11

The given figure shows a composite transistor consisting of a MOSFET and a bipolar transistor in cascade.

The MOSFET has transconductance g_m of 3m A/V and bipolar transistor has β of 99. The overall transconductance of the composite transistor is? (If C is very large)



(A) 1.98 mA/V (B) 19.8 mA/V
(C) 29.7 mA/V (D) 2.97 mA/V

Solution

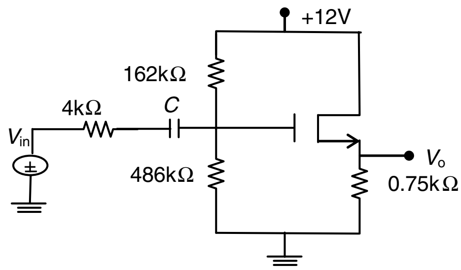
$$g_m \cdot V_{in} = I_E\ (\text{BJT}),\ \alpha = \frac{I_C}{I_E} = (BJT)$$
$$I_c = \alpha I_E = \alpha\, g_m . V_{in},$$
$$\alpha = \frac{\beta}{\beta + 1} = 0.99$$

$$g_m\ (\text{overall}) = \frac{I_c}{V_{in}} = g_m\ \alpha$$
$$= 3 \times 10^{-3} \times 0.99 = 2.97 \times 10^{-3}\ \text{Mho}$$

Direction for questions 12 to 14:

Example 12

The source follower amplifier circuit shown in the following figure. Transistor parameters are $V_{th} = 1.2$ V, $k_n = 4$ mA/V^2, and $\lambda = 0.01$ V^{-1} small signal transconductance and I_D are



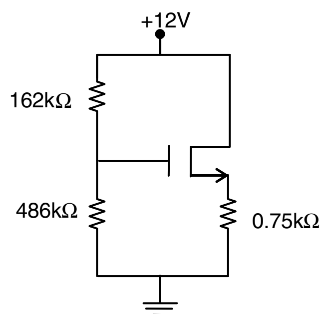
(A) 8.47 mA, 14.8 mA/V (B) 6.47 mA, 14.8 mA/V
(C) 6.47 mA, 11.6 mA/V (D) 8.47 mA, 11.6 mA/V

Solution

DC analysis of the circuit

$$\frac{V_G - 12}{162} + \frac{V_G - 0}{486} = 0\ \Rightarrow V_G = 9V$$

$$I_D = \frac{V_G - V_{GS}}{(0.75\text{k}\Omega)} = k_n\left(V_{GS} - V_{th}\right)^2$$



$$\left(9 - V_{GS}\right) = (0.75)(4)(V_{GS} - 1.2)^2$$
$$\left(9 - V_{GS}\right) = 3(V_{GS} - 1.2)^2$$
$$9 - V_{GS} = 3V_{GS}^{\ 2} - 7.2V_{GS} + 4.32$$
$$3V_{GS}^{\ 2} - 6.2V_{GS} - 4.68 = 0$$
$$V_{GS} = 2.65 \text{ or } -0.58\ \text{(by solving)}$$

V_{GS} should be positive $V_{GS} = 2.65$ V

$$I_D = \frac{V_G - V_{GS}}{0.75\text{k}\Omega} = \frac{6.35}{0.75} = 8.47\text{mA}$$

Small signal transconductance is

$$g_m = \frac{dI_D}{dV_{GS}} = 2k_n(\text{V}_{GS} - \text{V}_{th})$$
$$= 2 \times 4 \times (2.65 - 1.2) = 11.6 \text{ mA/V}$$

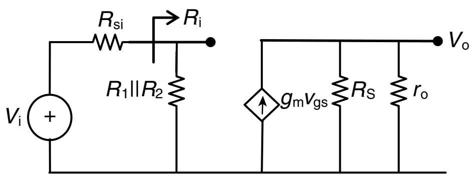
Example 13

Small signal voltage gain $A_\vartheta = \frac{V_o}{V_i}$ is

(A) 1.2 (B) 1.13
(C) 0.98 (D) 0.86

Solution

The small signal equivalent circuit of the given amplifier is



$R_{si} = 4\ k\Omega,\ R_1 = 162\ k\Omega,\ R_2 = 486\ k\Omega,\ R_s = 0.75\ k\Omega$

$r_o \approx [\lambda I_D]^{-1} = 1/0.01 \times 8.47 = 11.8k\Omega$

$R_i = R_1 \parallel R_2 = 121.5\ k\Omega$

$$\text{Voltage gain } A_\vartheta = \frac{g_m(R_S \parallel r_o)}{1 + g_m(R_S \parallel r_o)} \cdot \frac{R_i}{R_i + R_{si}}$$

$$= \frac{11.6(0.75 \parallel 11.8)}{1 + 11.6(0.75 \parallel 11.8)} \times \frac{121.5}{121.5 + 4} = 0.86$$

Example 14

The output resistance of the amplifier circuit is

(A) 87.8 Ω (B) 82.3 Ω
(C) 79.3 Ω (D) 76.6 Ω

Solution

By small signal equivalent circuit, output independence is

$$R_0 = \frac{1}{g_m} \parallel R_s \parallel r_0$$

$$= 0.086 \parallel 0.75 \parallel 11.8\ k\Omega$$

$0.076\ k\Omega \Rightarrow 76.6\ \Omega$

EXERCISES

Practice Problems I

Direction for questions 1 to 30: Select the correct alternative from the given choices.

Direction for questions 1 and 2:

A BJT has $h_{fe} = 220$, $g_m = 40 \times 10^{-3}$ ℧, $C_{cb} = 10$ pF and $C_{be} = 50$ pF.

1. What is unity gain frequency f_T?
(A) 80.6 MHz (B) 106.6 MHz
(C) 20 MHz (D) 100 kHz

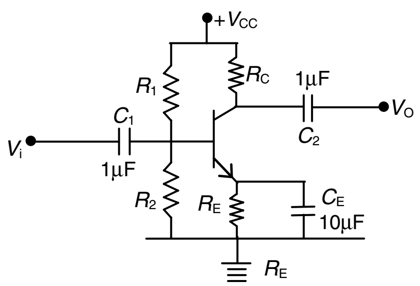
2. What is β cut-off frequency f_β?
(A) 4.84 kHz (B) 0.359 MHz
(C) 3.59 kHz (D) 0.484 MHz

Direction for questions 3 and 4:

A CE amplifier is shown in the following figure with the following specifications.

$R_1 = 40\ k\Omega,\ R_2 = 4.7\ k\Omega$
$R_C = 4\ k\Omega,\ R_E = 1.2\ k\Omega,\ \beta = 100$

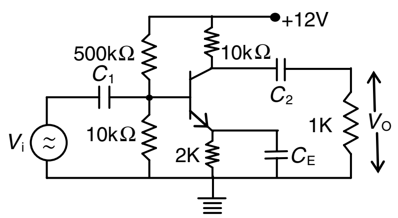
Further, $V_T = 26$ mv and $V_{CC} = 16$ V, $V_{BE} = 0.7$ V.



3. What is the voltage gain A_V of the amplifier?
(A) −132.3 (B) −10 (C) −121.5 (D) −30.6

4. If the bypass capacitor C_E is removed, the voltage gain is ________
(A) −100 (B) −3.33 (C) −2.73 (D) −121.5

5. The transistor shown in the following figure has $r_e = \frac{V_T}{I_E} = 2.6\Omega$.
The mid-band voltage gain of the amplifier is ________



(A) −350 (B) −177 (C) −212 (D) −182

6. A multistage amplifier is to be constructed using four identical stages, each of which has a lower cut-off frequency 60 Hz and upper cut-off frequency 1 MHz. The bandwidth of multistage amplifier is ________
(A) 0.39 MHz (B) 4 MHz
(C) 0.435 MHz (D) 0.51 MHz

7. A multistage amplifier has three stages. The voltage gain of three stages are 30, 50, and 60, respectively. The overall gain in dB is ________
(A) 60 dB (B) 105.2 dB
(C) 140 dB (D) 99.06 dB

8. A multistage amplifier have two identical stages. If each stage has $R_{in} = 2\ k\Omega$, $\beta = 80$ and $R_C = 3.5\ k\Omega$. The overall voltage gain is ________
(A) 2,090 (B) 19,600
(C) 280 (D) 70

9. The following parameters were measures on transistor biased at $I_C = 2$ mA:
$h_{fe} = 80\ h_{re} = 0.5 \times 10^{-4}$

$h_{oe} = 1.4 \times 10^{-6}$ A/V

Calculate g_m and r_π.

(A) $g_m = 0.769$ ℧, $r_\pi = 10.4$ kΩ

(B) $g_m = 76.9$ ℧, $r_\pi = 1.04$ kΩ

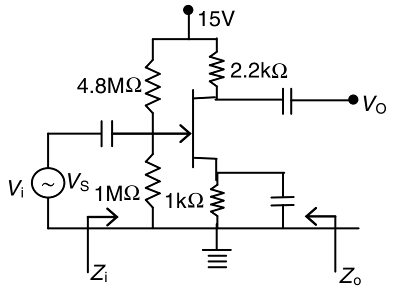
(C) $g_m = 76.9 \times 10^{-3}$ ℧, $r_\pi = 1.04$ kΩ

(D) $g_m = 76.9 \times 10^{-3}$ ℧, $r_\pi = 10$ kΩ

Direction for question 10:

A JFET common source amplifier is given in the following figure. The specifications are

$r_d = 100$ kΩ, $g_m = 3 \times 10^{-3}$ S



10. The input impedance Z_i is

(A) 827 kΩ (B) 82.7 MΩ

(C) 1 MΩ (D) 5 MΩ

11. The output impedance Z_o is

(A) 220 Ω (B) 3.2 kΩ

(C) 2.2 kΩ (D) 2.152 kΩ

12. The voltage gain A_V is–

(A) –6.6 (B) –3 (C) –300 (D) –6.456

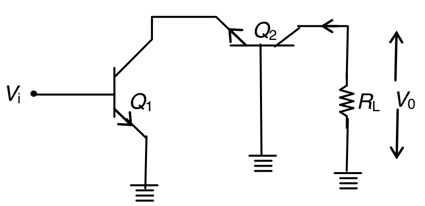
13. In a single-stage amplifier,

$R_C = 10$ kΩ, $R_{in} = 2$ kΩ, $\beta = 50$, and $R_L = 10$ kΩ. A small signal voltage $V_i(t) = 0.5 \sin\omega t$ mV is applied, the output voltage V_o is ________

(A) $-62.5 \sin\omega t$ mV (B) $-125 \sin\omega t$, mV

(C) $-31.5 \sin\omega t$, mV (D) $62.5 \sin\omega t$, v

14. In the cascode amplifier shown in the figure, if the common emitter stage Q_1 has $r_{e1} = 26\,\Omega$ and common base Q_2 has $r_{e2} = 12\,\Omega$, then the output current i_o for $V_i = 0.2$ V is ________



(A) 16 mA (B) 7.7 mA

(C) 6.2 mA (D) None

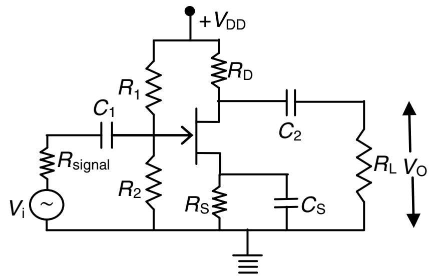
15. A CE amplifier has a unity gain frequency of 305 MHz with a gain of 92 dB. The 3 dB bandwidth is ________

(A) 16.2 MHz (B) 305 MHz

(C) 4 MHz (D) 7.66 kHz

Direction for questions 16 and 17:

An FET amplifier is shown with the following specifications. $R_1 = 1$ MΩ, $R_2 = 200$ kΩ, $R_S = 1$ kΩ, $R_D = 2$ kΩ, $R_L = 1.8$ kΩ, $R_{signal} = 5$ kΩ, $C_1 = C_2 = 0.1$ µF and $v_{DD} = 20$ volts. The other parameters of FET are $r_d = 100$ kΩ, $C_{gs} = 4$ pF, $C_{ds} = 0.5$ pF, $C_{gd} = 1.2$ pF, and $g_m = 4 \times 10^{-3}$ ℧



16. The approximate lower cut-off frequency is ________

(A) 9.35 Hz (B) 60.5 Hz

(C) 21.5 Hz (D) 425.5 Hz

17. The approximate upper cut-off frequency is ________

(A) 84.6 MHz (B) 10 MHz

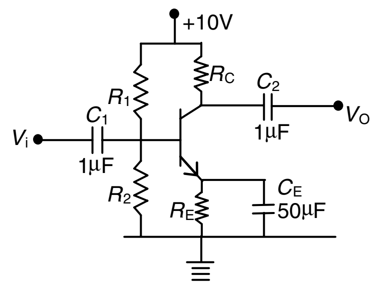
(C) 5.7 MHz (D) 210 MHz

18. An amplifier circuit with $R_C = 2$ kΩ operating at $I_C = 1.2$ mA. If the gain bandwidth product of the amplifier is 125 kHz, then the bandwidth of the same amplifier, assuming $V_T = 26$ mv, is ________

(A) 2.7 kHz (B) 62.5 kHz

(C) 1.35 kHz (D) None of these

19. An RC-coupled CE amplifier is shown in the following figure with following specifications. $R_1 // R_2 = 4$ kΩ, $\beta = 50$, $h_{ie} = 1$ kΩ, $R_C = 2$ kΩ, and $R_E = 0.5$ kΩ. What is the loss in gain, if the bypass capacitor C_E is removed?

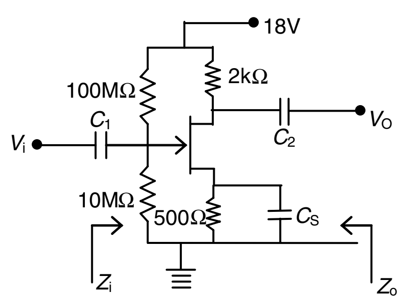


(A) 4% (B) 0% (C) 0.4% (D) 96%

Direction for questions 20 to 22:

AFET amplifier is given in the following figure with following specifications.

$I_{DSS} = 5$ mA, $V_P = -2.5$ V and $r_d = 80$ kΩ



20. The input impedance Z_i is
(A) 100 MΩ (B) 9.09 MΩ
(C) 110 MΩ (D) 10 MΩ

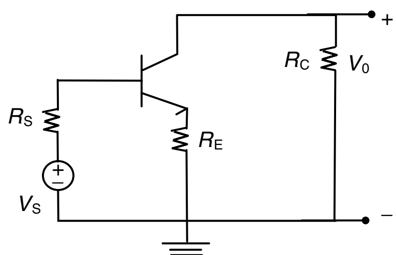
21. The output impedance Z_o is
(A) 1.95 kΩ (B) 80 kΩ
(C) 10 kΩ (D) 2.5 kΩ

22. The output V_o for $V_i = 30$ mV is
(A) –0.95 V (B) –150 mV
(C) –40.5 mV (D) –81.432 mV

23. The emitter follower using a p–n–p transistor with $\beta_0 = 150$ is biased at $I_C = 0.25$ mA, the voltage signal source has $R_S = 3$ kΩ. In order to make the overall $R_0 = 110\ \Omega$, the value of R_E is
(A) 1.42 Ω (B) 2.04 Ω
(C) 0.71 kΩ (D) 1.42 kΩ

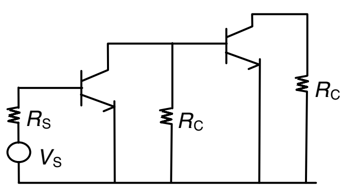
24. For the abovementioned value of R_E, the values of A_V and R_i (input resistance) are
(A) 1, 230 kΩ (B) 2.8, 330 kΩ
(C) 0.92, 230 kΩ (D) 0.92, 330 kΩ

25. In the circuit shown in the following figure, the transistor has $\beta_0 = 125$, and operated $I_C = 0.3$ mA. The element values are $R_S = 2$ kΩ, $R_G = 5$ kΩ, and $R_E = 100\ \Omega$, and the value of V_O/V_S is?



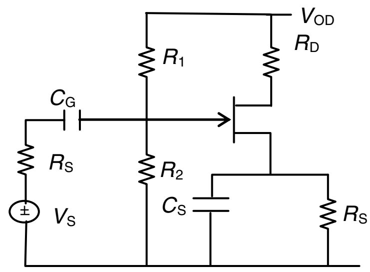
(A) –18.35 (B) 20.46
(C) –24.98 (D) 32.46

26. Both the transistors have $\beta_0 = 120$, and operated at $I_C = 1$ mA, $R_S = 0.5$ kΩ, $R_C = 1.5$ kΩ. Find overall gain.



(A) 91.4 (B) 1,028
(C) 2,056 (D) 3,084

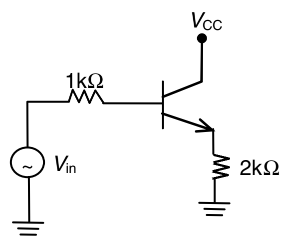
27.



An FET Amplifier shown in the abovementioned figure has parameters $g_m = 2$m Mho, $r_d = 20$ kΩ, what is the value of load R_D for mid-band gain of –20? Assume that R_S, C_S bias is short $R_S = 300\ \Omega$, $R_1 = 160$ kΩ, $R_2 = 40$ kΩ.
(A) 20 kΩ (B) 30 kΩ (C) 40 kΩ (D) 0 Ω

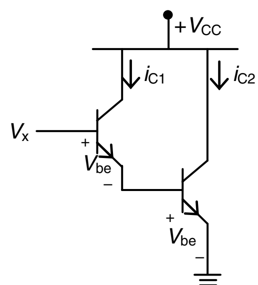
28. The value of input coupling capacitor C_G for lower cut-off frequency $f_L = 300$ Hz in the abovementioned circuit is
(A) 0.025 μF (B) 0.052 μF
(C) 0.016 μF (D) 0.043 μF

29. An amplifier circuit is shown in the figure; assume that the transistor works in active region. The low frequency small signal parameters for the BJT are $g_m = 20$ ms, $\beta = 50$, $r_o = \infty$, and $r_b = 0$; $\frac{V_0}{V_{in}}$ of the amplifier is



(A) 0.967 (B) 0.976
(C) 0.983 (D) 0.998

30. The Darlington pair stage is shown in the following figure. If the transconductance of Q_1 is 8×10^{-3} ℧ and Q_2 is 6×10^{-3} ℧, the overall transconductance g_m is ______.

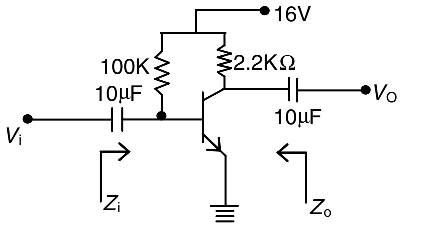


(A) 14×10^{-3} ℧ (B) 2×10^{-3} ℧
(C) 3×10^{-3} ℧ (D) 6×10^{-3} ℧

Practice Problems 2

Direction for questions 1 to 22: Select the correct alternative from the given choices.

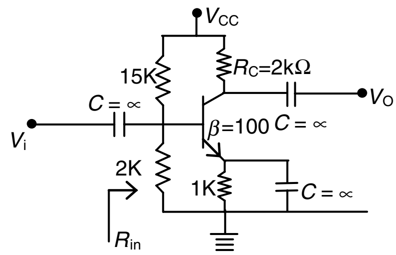
Direction for questions 1 to 3:
The *h* parameters of the transistor are $h_{ie} = 400\ \Omega$ and $h_{fe} = 80$ and the transistor amplifier is given in the following figure.



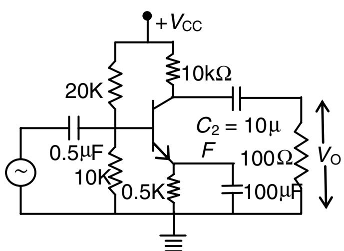
1. What is the input impedance Z_i as seen from source?
   (A) 400 Ω (B) 100 kΩ
   (C) 500 kΩ (D) 398 Ω
2. What is the output Impedance Z_o?
   (A) 2.2 kΩ (B) 10 kΩ
   (C) 6.2 kΩ (D) 6 kΩ
3. What is the voltage gain of the amplifier?
   (A) –80 (B) –440
   (C) –612 (D) 1

Direction for questions 4 and 5:
The typical parameters of the hybrid π-model of transistor at room temperature and for $I_C = 1.8$ mA are $C_\pi = 100$ pF and $f_T = 80$ MHz

4. The value of g_m in mA/V is ________
   (A) 6.9 (B) 0.69 (C) 0.069 (D) 69
5. The capacitance C_μ is ________
   (A) 38 pF (B) 2 pF
   (C) 3.8 pF (D) 0.38 pF
6. The transconductance g_m of the transistor shown is 8 mS. The value of input resistance R_{in} seen from source is ________

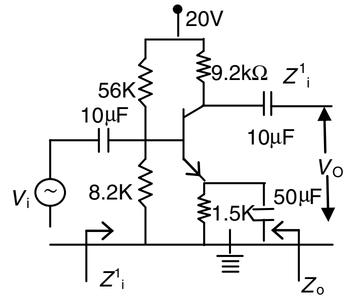


   (A) 1.54 kΩ (B) 12.5 kΩ
   (C) 1.764 kΩ (D) 2.5 kΩ
7. A RC-coupled CE amplifier is shown in the following figure. The lower cut-off frequency f_1 due to coupling capacitor C_2 is ________



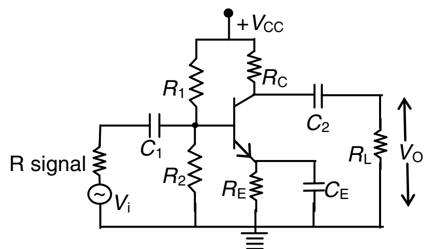
   (A) 29 Hz (B) 145 Hz
   (C) 50 HZ (D) 32 Hz

Direction for questions 8 and 9:
A CE transistor amplifier is shown in the following figure with
$h_{ie} = 2.12$ kΩ, $h_{re} = 0$, $h_{fe} = 50$, and $h_{oe} = 0.2 \times 10^{-3}$ ℧



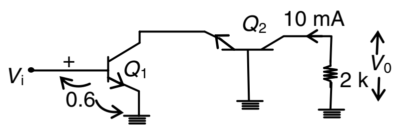
8. The input impedance Z_i^I is ________
   (A) 7.15 kΩ (B) 8.78 kΩ
   (C) 2.12 kΩ (D) 1.63 kΩ
9. The output impedance Z_o is ________
   (A) 7.77 kΩ (B) 9.2 kΩ
   (C) 43.2 kΩ (D) 50 kΩ

Direction for questions 10 to 12:
A RC-coupled CE amplifier is shown in the following figure.



The specifications are
$R_{signal} = 1$ kΩ, $R_1 = 20$ kΩ, $R_2 = 5$ kΩ, $R_C = 1$ kΩ, $R_E = 1$ kΩ, $R_L = 1$ kΩ, $C_1 = 0.5$ μF, $C_2 = 1$ μF, and $C_E = 100$ μF.

10. The lower cut-off frequency due to C_1 is
    (A) 23.4 Hz (B) 64 Hz
    (C) 32 Hz (D) 128 Hz
11. The lower cut-off frequency due to C_2 is
    (A) 0 Hz (B) 100 Hz
    (C) 64 Hz (D) 80 Hz
12. What is the value of C_2 required to have a lower cut-off frequency of 100 Hz?
    (A) 80 μF (B) 8 pF
    (C) 0.8 μF (D) 8 μF
13. A cascode amplifier is given in the following figure. The voltage gain $A_v = \frac{V_o}{V_i}$ *is* ________



    (A) –67 (B) –33.3 (C) –16.6 (D) –1

14. The three amplifier stages are cascoded to provide overall gain of 12,000. The first two stages have a gain of 45 dB and 25.12, respectively, then the gain of third stage in dB is ________

(A) 3 dB (B) 28 dB
(C) 80 dB (D) 8.58 dB

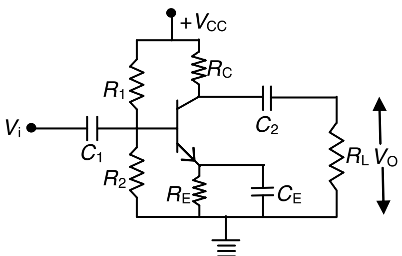
15. The rise time of the amplifier to the input is 70 ns. The bandwidth of the amplifier is ________

(A) 1 MHz (B) 5 MHz
(C) 10 MHz (D) 0.5 MHz

16. The mid-frequency gain of RC-coupled CE amplifier is 200. The lower and upper cut-off frequencies are 50 Hz and 80 kHz. The frequencies at which gain falls to 150 are ________ and ________

(A) 50 Hz, 80 kHz (B) 56.69 Hz, 70.55 kHz
(C) 25 Hz, 40 kHz (D) 10 Hz, 90 kHz

17. A CE transistor amplifier shown in the following figure specified with $h_{fe} = 50$, $h_{ie} = 2$ kΩ, and $R_L = 10$ kΩ. The value of R_C required to maintain a mid-band gain $A_V = -120$ is ________ kΩ

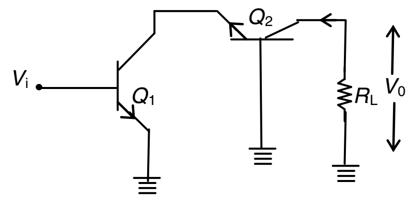


(A) 10 (B) 5 (C) 2.75 (D) 9.23

18. The mid-band gain of the amplifier is 62 dB. The gain at lower (or) upper 3 dB is ________

(A) 59 dB (B) 31 dB
(C) $\frac{62}{\sqrt{2}}$ db (D) 65 dB

19. A cascode amplifier is shown in the following figure. The transistor
Q_1 has $g_{m1} = 5$ mA/V and
Q_2 has $g_{m2} = 1.25$ mA/V.
The overall transconductance g_m of the Cascode amplifier is ________



(A) 5 mA/V (B) 1.25 mA/V
(C) 6.25 mA/V (D) 4 mA/V

Direction for questions 20 to 22:

A multistage amplifier has four identical stages. Each stage is specified with gain $A = 60$ with lower cut-off $f_1 = 30$ Hz and upper cut-off $f_2 = 90$ kHz.

20. The overall gain A^1 in dB is

(A) 47.6 dB (B) 32.55 dB
(C) 142.25 dB (D) 60 dB

21. The overall lower cut-off frequency $f_1^{\,1}$ is ________

(A) 120 Hz (B) 69 Hz
(C) 7.5 Hz (D) 21.2 Hz

22. The overall upper cut-off frequency $f_2^{\,1}$ is ________

(A) 22.5 kHz (B) 45 kHz
(C) 39.13 kHz (D) 360 kHz

Previous Years' Questions

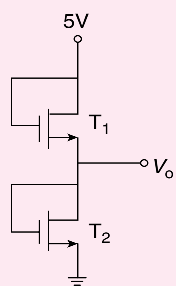
1. A bipolar transistor is operating in the active region with a collector current of 1 mA. Assuming that the β of the transistor is 100 and the thermal voltage (V_T) is 25 mV, the transconductance (g_m), and the input resistance (r_π) of the transistor in the common emitter configuration are **[2004]**

(A) $g_m = 25$ mA/V and $r_\pi = 15.625$ kΩ
(B) $g_m = 40$ mA/V and $r_\pi = 4.0$ kΩ
(C) $g_m = 25$ mA/V and $r_\pi = 2.5$ kΩ
(D) $g_m = 40$ mA/V and $r_\pi = 2.5$ kΩ

2. The cascade amplifier is a multistage configuration of **[2005]**

(A) CC–CB (B) CE–CB
(C) CB–CC (D) CE–CC

3. Both transistors T_1 and T_2 in the figure have a threshold voltage of 1 v. The device parameters k_1 and k_2 of T_1 and T_2 are, respectively, 36 μA/V² and 9 μA/V². The output voltage V_0 is **[2005]**



(A) 1 V (B) 2 V (C) 3 V (D) 4 V

4. An n-channel depletion MOSFET has following two points on its I_D–V_{GS} curve:
(i) $V_{GS} = 0$ at $I_D = 12$ mA and
(ii) $V_{GS} = -6$ v at $I_D = 0$
Which of the following Q points will give the highest transconductance gain for small signals? **[2006]**

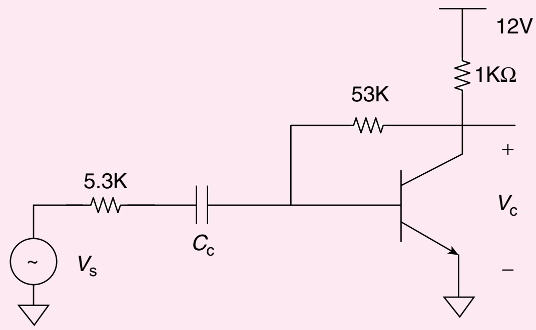
(A) $V_{GS} = -6$ v (B) $V_{GS} = -3$ v
(C) $V_{GS} = 0$ v (D) $V_{GS} = 3$ v

Direction for questions 5 to 7:

In the transistor amplifier circuit shown in the figure, the transistor has the following parameters:

$\beta_{DC} = 60$, $V_{BE} = 0.7$ V, $h_{ie} \to \infty$ $h_{fe} \to \infty$

The capacitance C_c can be assumed to be infinite.



In the figure, the ground has been shown by the symbol Ñ.

5. Under the DC conditions, the collector-to-emitter voltage drop is: **[2006]**

(A) 4.8 v (B) 5.3 v (C) 6.0 v (D) 6.6 v

6. If β_{DC} is increased by 10% the collector-to-emitter voltage drop **[2006]**

(A) increased by less than or equal to 10%
(B) decreases by less than or equal to 10%
(C) increase by more than 10%
(D) decreases by more than 10%

7. The small signal gain of the amplifier v_c/v_s is: **[2006]**

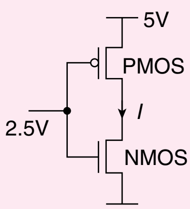
(A) –10 (B) –5.3 (C) 5.3 (D) 10

8. In the CMOS inverter circuit shown, if the transconductance parameters of the NMOS and PMOS transistors are k_n =

$$k_p = \mu_n C_0 \times \frac{W_n}{L_n} = \mu_P C_0 \times \frac{W_p}{L_p} = 40\,\mu A / V^2$$

and their threshold voltages are

$V_{THn} = \left|V_{TH_p}\right| = 1$, the current I is **[2007]**



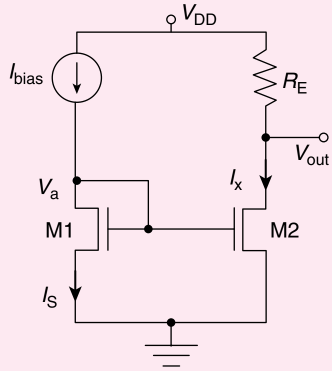
(A) 0 A (B) 25 μA
(C) 45 μA (D) 90 μA

9. The drain current of an MOSFET in saturation is given by $I_D = K(V_{GS} - V_T)^2$, where K is a constant. The magnitude of the transconductance g_m is **[2008]**

(A) $\frac{K(V_{GS} - V_T)^2}{V_{DS}}$ (B) $2K(V_{GS} - V_T)$

(C) $\frac{I_D}{V_{GS} - V_{DS}}$ (D) $\frac{K(V_{GS} - V_T)^2}{V_{GS}}$

10. For the circuit shown in the following figure, transistors $M1$ and $M2$ are identical NMOS transistors. Assume that $M2$ is in saturation and the output is unloaded.

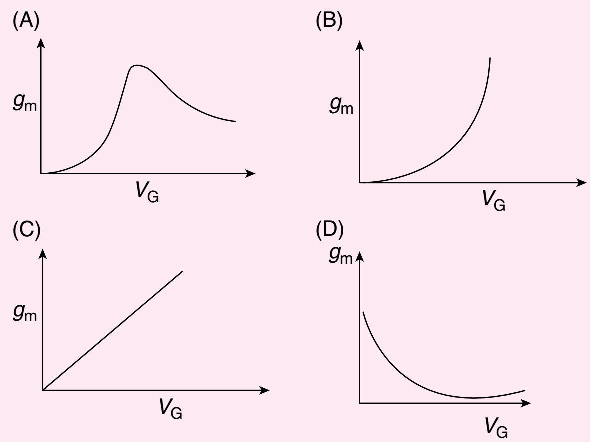


The current I_x is related to I_{bias} as **[2008]**

(A) $I_x = I_{bias} + I_s$ (B) $I_x = I_{bias}$

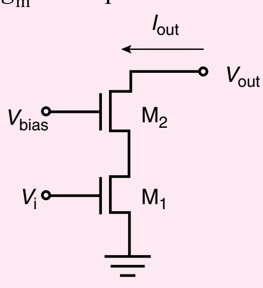
(C) $I_x = I_{bias} - I_s$ (D) $I_x = I_{bias} - \left(V_{DD} - \frac{V_{out}}{R_E}\right)$

11. The measured transconductance g_m of an NMOS transistor operating in the linear region is plotted against the gate voltage V_G at constant drain voltage V_D. Which of the following figures represent the expected dependence of g_m on V_G? **[2008]**



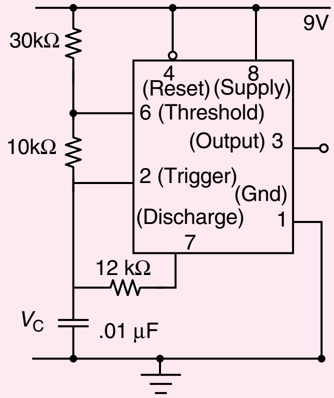
12. Two identical NMOS transistors $M1$ and $M2$ are connected as shown in the following figure. V_{bias} is chosen so that both transistors are in saturation. The equivalent g_m of the pair is defined to be $\frac{\partial I_{out}}{\partial V_1}$ at constant V_{out}.

The equivalent g_m of the pair is **[2008]**



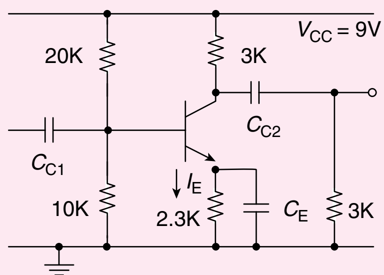
(A) The sum of individual g_ms of the transistors
(B) The product of individual g_ms of the transistors
(C) Nearly equal to the g_m of $m1$
(D) Nearly equal to g_m/g_0 of $m2$

13. An astable multivibrator circuit using IC 555 timer is shown in the following figure. Assume that the circuit is oscillating steadily **[2008]**



The voltage V_c across the capacitor varies between
(A) 3 V to 5 V (B) 3 V to 6 V
(C) 3.6 V to 6 V (D) 3.6 V to 5 V

Direction for questions 14 and 15:
In the following transistor circuit, $V_{BE} = 0.7$ V, $r_e = 25$ mV/I_E, β and all the capacitances are very large.

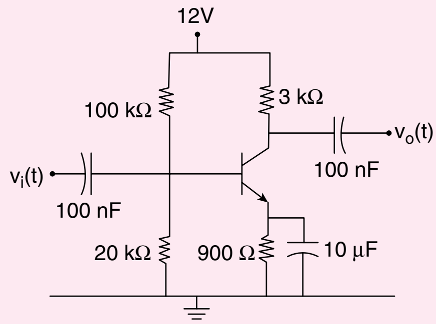


14. The value of DC current I_E is **[2008]**
(A) 1 mA (B) 2 mA
(C) 5 mA (D) 10 mA

15. The mid-band voltage gain of the amplifier is approximately **[2008]**
(A) −180 (B) −120 (C) −90 (D) −60

16. Consider the following two statements about the internal conditions in an n-channel MOSFET operating in the active region
S_1: The inversion charge decreases from source to drain.
S_2: The channel potential increases from source to drain.
Which of the following is correct? **[2009]**
(A) Only S_2 is true
(B) Both S_1 and S_2 are false.
(C) Both S_1 and S_2 are true, but S_2 is not a reason for S_1.
(D) Both S_1 and S_2 are true, and S_2 is a reason for S_1.

17. A small signal source $V_i(t) = A\cos 20t + B\sin 10^6 t$ is applied to a transistor amplifier as shown in the following figure. The transistor has $\beta = 150$ and $h_{ie} = 3$ kΩ. Which expression best approximates $V_o(t)$? **[2009]**



(A) $V_o(t) = -1{,}500\ (A\cos 20t + B\sin 10^6 t)$
(B) $V_o(t) = -150\ (A\cos 20t + B\sin 10^6 t)$
(C) $V_o(t) = -1{,}500\ B\sin 10^6 t$
(D) $V_o(t) = -150\ B\sin 10^6 t$

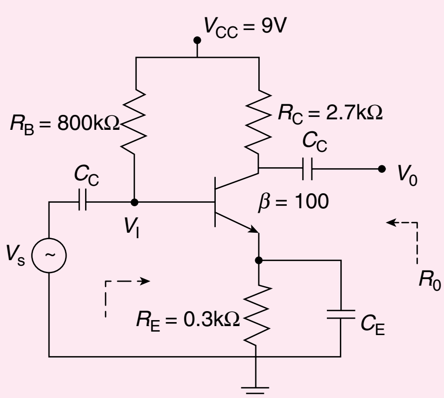
18. For small increase in V_G beyond 1 V, which of the following gives the correct description of the region of operation of each MOSFET? **[2009]**
(A) Both the MOSFETs are in saturation region.
(B) Both the MOSFETs are in triode region.
(C) n-MOSFET is in triode and p-MOSFET is in saturation region.
(D) n-MOSFET is in saturation and p-MOSFET is in triode region.

19. Estimate the output voltage V_0 for $V_G = 1.5$ V. [Hint: use the appropriate current voltage equation for each MOSFET, based on the answer to Q.57] **[2009]**

(A) $4 - \frac{1}{\sqrt{2}}$ V (B) $4 + \frac{1}{\sqrt{2}}$ V

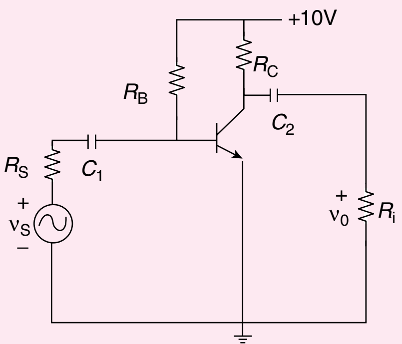
(C) $4 - \frac{\sqrt{3}}{2}$ V (D) $4 + \frac{\sqrt{3}}{2}$ V

20. The amplifier circuit shown in the following figure uses a silicon transistor. The capacitors C_C and C_E can be assumed to be short at signal frequency and the effect of output resistance r_0 can be ignored. If C_E is disconnected from the circuit, which one of the following statements is true? **[2010]**



(A) The input resistance R_i increases and the magnitude of voltage gain A_V decreases.
(B) The input resistance R_i decreases and the magnitude of voltage gain A_V decreases.
(C) Both input resistance R_i and the magnitude of voltage gain A_V decreases.
(D) Both input resistance R_i and the magnitude of voltage gain A_V increases.

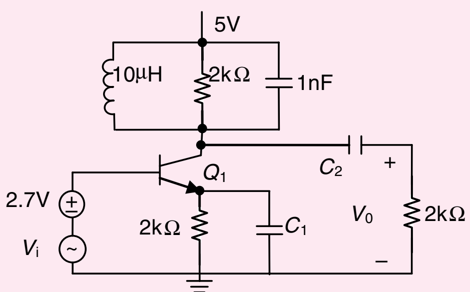
Direction for questions 21 and 22:
Consider the common emitter amplifier shown in the following figure with the following circuit parameters:
$\beta = 100$, $g_m = 0.3861$ A/V, $r_0 = \infty$, $r_p = 259\ \Omega$, $R_S = 1$ kΩ, $R_B = 93$ kΩ, $R_C = 250\ \Omega$, $R_L = 1$ kΩ, $C_1 = \infty$, and $C_2 = 4.7$ mF.



21. The resistance seen by the source V_s is **[2010]**
(A) 258 Ω (B) 1,258 Ω
(C) 93 kΩ (D) ∞

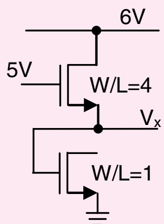
22. The lower cut-off frequency due to C_2 is **[2010]**
(A) 33.9 Hz (B) 27.1 Hz
(C) 13.6 Hz (D) 16.9 Hz

23. In the following circuit, capacitors C_1 and C_2 are very large and are shorts at the input frequency. V_1 is a small signal input. The gain magnitude $|V_o/V_i|$ at 10 Mrad/s is **[2011]**



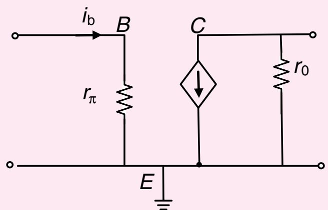
(A) Maximum (B) minimum
(C) unity (D) zero

24. In the following circuit, for the MOS transistors, $\mu_n C_{ox} = 100\ \mu A/V^2$ and the threshold voltage $V_T = 1$ V. The voltage V_x at the source of the upper transistor is **[2011]**



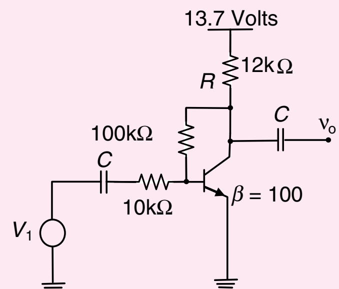
(A) 1 V (B) 2 V
(C) 3 V (D) 3.67 V

25. The current i_b through the base of a silicon npn transistor is $1 + 0.1\cos(10{,}000\pi t)$ mA. At 300 K, the $r\pi$ in the small model of the transistor is **[2012]**



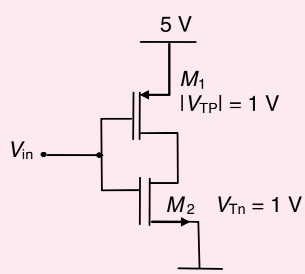
(A) 250 Ω (B) 27.5 Ω
(C) 25 Ω (D) 22.5 Ω

26. The voltage gain A of the following circuit is **[2012]**



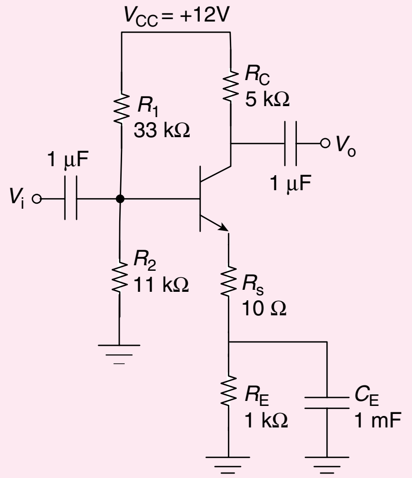
(A) $|A_V| \approx 200$ (B) $|A_V| \approx 100$
(C) $|A_V| \approx 20$ (D) $|A_V| \approx 10$

27. In the CMOS circuit shown, electron and hole mobilities are equal, and M_1 and M_2 are equally sized. The device M_1 is in the linear region if **[2012]**



(A) $V_{in} < 1.875$ V
(B) $1.875\ V < V_{in} < 3.125$ V
(C) $V_{in} > 3.125$ V
(D) $0 < V_{in} < 5$ V

28. For the amplifier shown in the figure, the BJT parameters are $V_{BE} = 0.7$ V, $\beta = 200$, and thermal voltage V_T = 25 mV. The voltage gain (v_o/v_i) of the amplifier is ________. **[2014]**

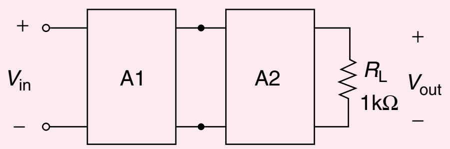


29. A cascade connection of two voltage amplifiers $A1$ and $A2$ is shown in the figure. The open-loop gain A_{v0}, input resistance R_{in}, and output resistance R_o for $A1$ and $A2$ are as follows:

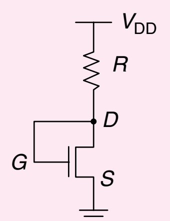
$A1$: $A_{v0} = 10$, $R_{in} = 10$ kΩ, $R_o = 1$ kΩ

$A2$: $A_{v0} = 5$, $R_{in} = 5$ kΩ, $R_o = 200$ Ω

The approximate overall voltage gain v_{out}/v_{in} is ________ **[2014]**



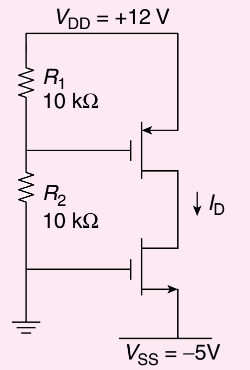
30. For the n-channel MOS transistor shown in the figure, the threshold voltage V_{Th} is 0.8 V. Neglect channel length modulation effects. When the drain voltage V_D = 1.6 V, the drain current I_D was found to be 0.5 mA. If V_D is adjusted to be 2 V by changing the values of R and V_{DD}, the new value of I_D (in mA) is **[2014]**



(A) 0.625 (B) 0.75 (C) 1.125 (D) 1.5

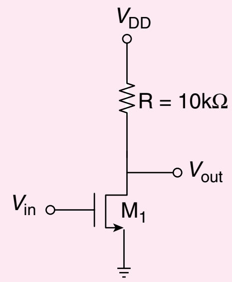
31. For the MOSFETs shown in the figure, the threshold voltage $|V_t| = 2$ V and $K = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right) = 0.1\,\text{mA/V}^2$

The value of I_D (in mA) is ________. **[2014]**



32. For the MOSFET M_1 shown in the figure, assume $W/L = 2$, $V_{DD} = 2.0$ V, $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, and $V_{TH} = 0.5$ V. The transistor M_1 switches from saturation region to linear region when V_{in} (in Volts) is ________.

[2014]



33. Consider the common-collector amplifier in the figure (bias circuitry ensures that the transistor operates in forward active region, but has been omitted for simplicity). Let I_C be the collector current, V_{BE} be the base-emitter voltage, and V_T be the thermal voltage. Further, g_m and r_o are the small-signal transconductance and output resistance of the transistor, respectively. Which one of the following conditions ensures a nearly constant small signal voltage gain for a wide range of values of R_E? **[2014]**

(A) $g_m R_E << 1$ (B) $I_C R_E >> V_T$
(C) $g_m r_o >> 1$ (D) $V_{BE} >> V_T$

34. A MOSFET in saturation has a drain current of 1 mA for $V_{DS} = 0.5$ V. If the channel length modulation coefficient is 0.05 V^{-1}, the output resistance (in kΩ) of the MOSFET is _____. **[2015]**

35. Which one of the following statements is correct about an ac coupled common emitter amplifier operating in the mid band region? **[2016]**

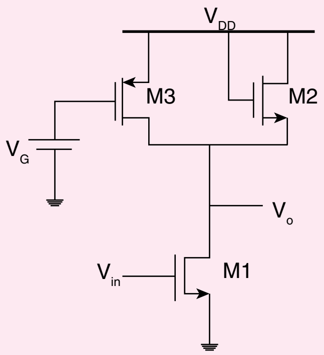
(A) The device parasitic capacitances behave like open circuits, whereas coupling and bypass capacitances behave like short circuits.

(B) The device parasitic capacitances, coupling capacitances and bypass capacitances behave like open circuits.

(C) The device parasitic capacitances, coupling capacitances and bypass capacitances behave like short circuits.

(D) The device parasitic capacitances behave like short circuits, whereas coupling and bypass capacitances behave like open circuits.

36. In the circuit shown in the figure, the channel length modulation of all transistors is non zero $(l \neq 0)$. Also, all transistors operate in saturation and have negligible body effect. The ac small signal voltage gain (V_0/V_{in}) of the circuit is: **[2016]**



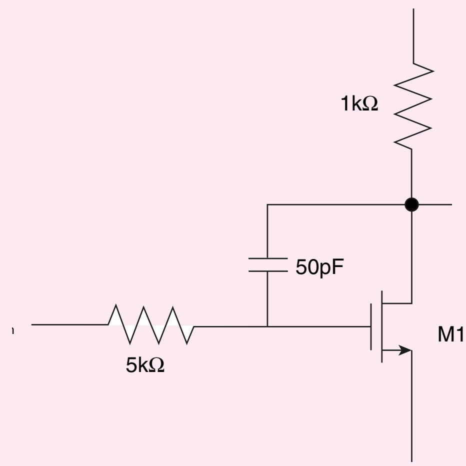
(A) $-g_{m1}(r_{01}||r_{02}||r_{03})$

(B) $-g_{m1}\left(r_{01} \,||\, \frac{1}{g_{m3}} \,||\, r_{03}\right)$

(C) $-g_{m1}\left(r_{01} \,||\left(\frac{1}{gm_2} \,||\, r_{02}\right)||\, r_{03}\right)$

(D) $-g_{m1}\left(r_{01} \,||\left(\frac{1}{gm_3} \,||\, r_{03}\right)||\, r_{02}\right)$

37. In the circuit shown in the figure, transistor M1 is in saturation and has transconductance $g_m = 0.01$ siemens. Ignoring internal parastitic capacitances and assuming the channel length modulation l to be zero, the small input pole frequency (in kHz) is ________ . **[2016]**



Answer Keys

Exercises

Practice Problems 1

1. B	**2.** D	**3.** C	**4.** B	**5.** A	**6.** C	**7.** D	**8.** B	**9.** C	**10.** A
11. D	**12.** D	**13.** A	**14.** B	**15.** D	**16.** D	**17.** C	**18.** C	**19.** D	**20.** B
21. A	**22.** D	**23.** D	**24.** C	**25.** C	**26.** C	**27.** A	**28.** C	**29.** A	**30.** C

Practice Problems 2

1. D	**2.** A	**3.** B	**4.** C	**5.** A	**6.** A	**7.** B	**8.** D	**9.** A	**10.** B
11. D	**12.** C	**13.** B	**14.** D	**15.** B	**16.** B	**17.** D	**18.** A	**19.** A	**20.** C
21. B	**22.** C								

Previous Years' Questions

1. D	**2.** B	**3.** C	**4.** D	**5.** C	**6.** B	**7.** A	**8.** D	**9.** B	**10.** B
11. A	**12.** C	**13.** B	**14.** A	**15.** D	**16.** D	**17.** B	**18.** D	**19.** D	**20.** A
21. B	**22.** B	**23.** A	**24.** C	**25.** C	**26.** D	**27.** A	**28.** −240 to −230		
29. 34 to 35.3		**30.** C	**31.** 0.88 to 0.92		**32.** 1.5	**33.** B	**34.** 19 to 21		
35. A		**36.** C	**37.** 57.88 kHZ						