CHAPTER 4.4

DIGITAL LOGIC FAMILIES

Statement for Q.1–2:

Consider the DL circuit of fig. P4.4.1–2.

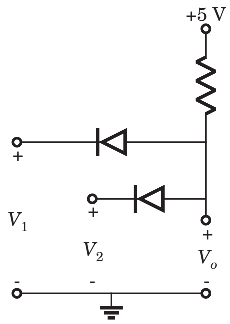

Fig. P4.4.1-2

1. For positive logic the circuit is a

(A) AND (B) OR

(C) NAND (D) NOR

2. For negative logic the circuit is a

(A) AND (B) OR

(C) NAND (D) NOR

3. The diode logic circuit of fig. P4.4.3 is a

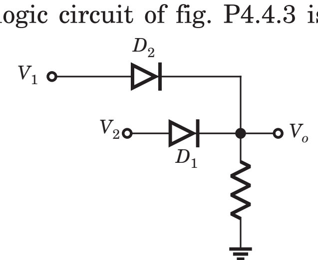

Fig. P4.4.3

(A) AND (B) OR

(C) NAND (D) NOR

4. In the circuit shown in fig. P.4.4.4. the output Z is

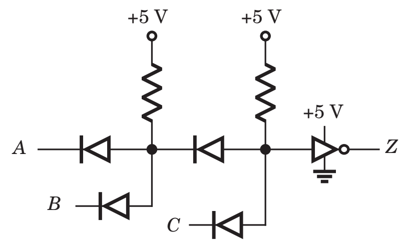

Fig. P4.4.4

(A) $AB + \overline{C}$ (B) $\overline{AB}C$

(C) $\overline{ABC}$ (D) ABC

Statement for Q.5–7:

Consider the AND circuit shown in fig. P4.4.5–7. The binary input levels are $V(0) = 0$ V and $V(1) = 25$ V. Assume ideal diodes. If $V_1 = V(0)$ and $V_2 = V(1)$, then V_o is to be at 5 V. However, if $V_1 = V_2 = V(1)$, then V_o is to rise above 5 V.

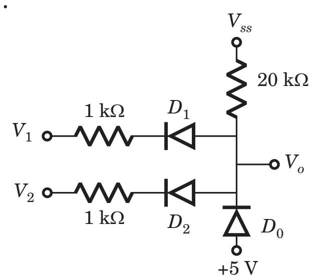

Fig. P4.4.5-7

5. If $V_{ss} = 20$ V and $V_1 = V_2 = V(1)$, the diode current I_{D1}, I_{D2}, and I_{D0} are

(A) 1 mA, 1 mA, 4 mA (B) 1 mA, 1 mA, 5 mA

(C) 5 mA, 5mA, 1 mA (D) 0, 0, 0

6. If $V_{ss} = 40$ V and both input are at HIGH level then, diode current I_{D1}, I_{D2} and I_{D0} are respectively

(A) 0.4 mA, 0.4 mA, 0 (B) 0, 0, 1 mA

(C) 0.4 mA, 0.4 mA, 1 mA (D) 0, 0, 0

7. The maximum value of V_{ss} which may be used is

(A) 30 V (B) 25 V

(C) 125 V (D) 20 V

8. The ideal inverter in fig. P4.4.8 has a reference voltage of 2.5 V. The forward voltage of the diode is 0.75 V. The maximum number of diode logic circuit, that may be cascaded ahead of the inverter without producing logic error, is

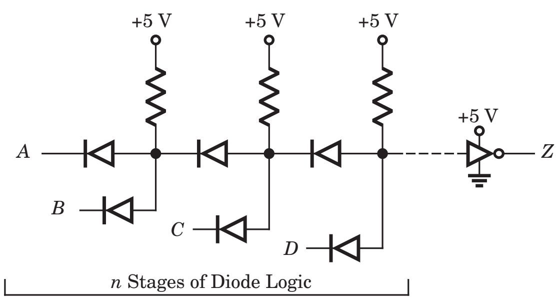

Fig. P4.4.8

(A) 3 (B) 4

(C) 5 (D) 9

9. Consider the TTL circuit in fig. P4.4.9. The value of V_H and V_L are respectively

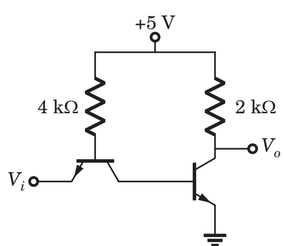

Fig. P4.4.9

(A) 5 V, 0 V (B) 4.8 V, 0 V

(C) 4.8 V, 0.2 V (D) 5 V, 0.2 V

Statement Q.10–11:

Consider the resistor transistor logic gate of fig. P4.4.10-11.

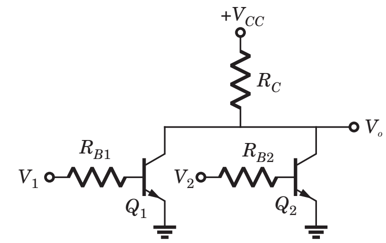

Fig. P4.4.10-11

10. For positive logic the gate is

(A) AND (B) OR

(C) NAND (D) NOR

11. For negative logic the gate is

(A) AND (B) OR

(C) NAND (D) NOR

Statement for Q.12–13:

Consider the RTL circuit of fig. P4.4.12–13.

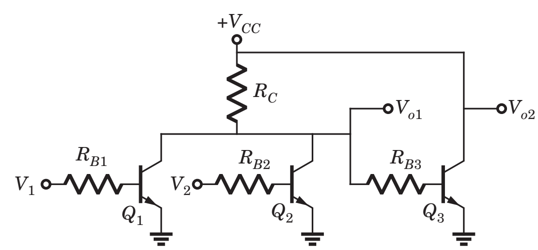

Fig. P4.4.12-13

12. If V_{o1} is taken as the output, then circuit is a

(A) AND (B) OR

(C) NAND (D) NOR

13. If V_{o2} is taken as output, then circuit is a

(A) AND (B) OR

(C) NAND (D) NOR

Statement for Q.14–15:

Consider the TTL circuit of fig. P4.4.14. If either or both V_1 and V_2 are logic LOW, Q_1 is driven to saturation.

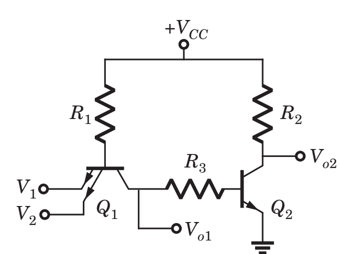

Fig. P4.4.14-15

22. The circuit shown in fig. P4.4.22 is

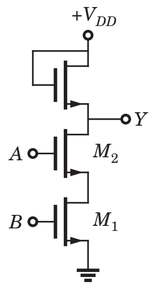

Fig. P4.4.22

(A) NAND (B) NOR

(C) AND (D) OR

23. The circuit shown in fig. P4.4.23 acts as a

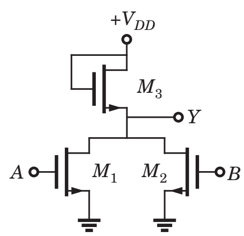

Fig. P4.4.23

(A) NAND (B) NOR

(C) AND (D) OR

24. The circuit shown in fig. P4.4.24 implements the function

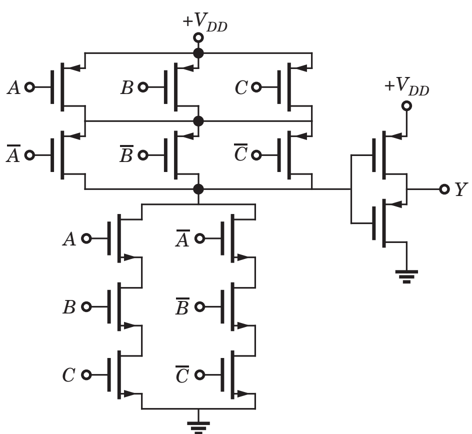

Fig. P4.4.24

(A) $ABC + \overline{ABC}$ (B $ABC + \overline{(A + B + C)}$

(C) $\overline{ABC} + \overline{(A + B + C)}$ (D) None of the above

25. The circuit shown in fig. P4.4.25. implements the function

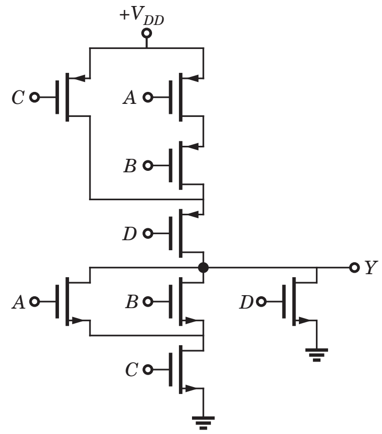

Fig. P4.4.25

(A) $(A + B)C + D$ (B) $\overline{(AB + C)D}$

(C) $\overline{(A + B)C + D}$ (D) $(AB + C)D$

26. Consider the CMOS circuit shown in fig. P4.4.26. The output Y is

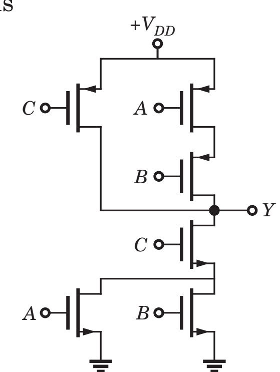

Fig. P4.4.26

(A) $\overline{(A + C)B}$ (B) $\overline{(A + B)C}$

(C) $AB + C$ (D) $AB + \overline{C}$

27. The CMOS circuit shown in fig. P4.4.27 implement

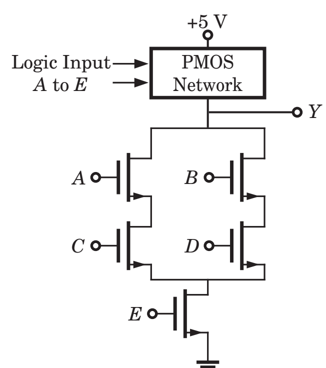

Fig. P4.4.27

(A) $\overline{AB + CD + E}$ (B) $\overline{(A + B)(C + D)E}$

(C) $AB + CD + E$ (D) $(A + B)(C + D)E$

V_1		V_2		V_o	
Actual	Logic	Actual	Logic	Actual	Logic
V_H	1	V_H	1	$V_{CE(sat)}$	0
V_L	0	V_L	0	V_{CE}	1
V_H	1	V_L	0	$V_{CE(sat)}$	0
V_L	0	V_H	1	$V_{CE(sat)}$	0

13. (B) The Q_3 stage is simply an inverter (a NOT gate). Thus output V_{o2} is the logic complement of V_{o1}. Therefore this is a OR gate.

14. (A) When Q_1 is saturated, V_{o1} is logic LOW otherwise V_{o1} is logic HIGH. The following truth table shows AND logic

V_1	V_2	V_{o1}
1	1	1
0	1	0
1	0	0
0	0	0

15. (C) The Q_2 stage is simply an inverter. Thus output V_{o2} is the logic complement of V_{o1}.

16. (C) If $V_1 = V_2 \le V_L$, $V_{o1} \approx V_{CC}$. If $V_1(V_2) > V_H$, while $V_2(V_1) \le V_L$, $Q_1(Q_2)$ is ON and $Q_2(Q_1)$ is OFF and $V_{o1} \approx V_{CC}$. If $V_1 = V_2 > V_H$, both Q_1 and Q_2 are ON and $V_{o1} \approx 2V_{CE(sat)}$. The truth table shows NAND logic

V_1		V_2		V_o	
Actual	Logic	Actual	Logic	Actual	Logic
V_L	0	V_L	0	V_{CC}	1
V_H	1	V_L	0	V_{CC}	1
V_L	0	V_H	1	V_{CC}	1
V_H	1	V_H	1	$2V_{CE(sat)}$	0

17. (A) The Q_3 stage is simple an inverter. Hence AND logic.

18. (C) For each successive gate, that has a transistor in saturation, the current required is

$$I_{B(sat)} = \frac{I_{C(sat)}}{\beta} = \frac{V_{CC} - V_{CE(sat)}}{\beta R_C} = \frac{5 - 0.2}{50(640)} = 0.15 \text{ mA}$$

For n attached gate $I_o = nI_{B(sat)}$.

To assure no logic error $V_o = V_{CC} - I_o R_C > V_H = 3.5$ V

$$n \le \frac{V_{CC} - 3.5}{R_C I_{B(sat)}} = \frac{5 - 3.5}{640(0.15\text{m})} = 15.6 \quad \Rightarrow \quad n \le 15$$

19. (A) Let $V_1 = V_2 = 0$ V, then M_3 will be ON, M_1 and M_2 OFF and M_4 ON, hence $V_o = -V_{DD}$. Let $V_1 = 0$ V and $V_2 = -V_{DD}$ then M_3 will be ON, M_1 OFF M_4 OFF, M_2 ON, hence $V_o = -V_{DD}$. Let $V_1 = -V_{DD}$ and $V_2 = 0$ V, then M_3 OFF, M_4 ON, M_2 OFF hence $V_o = -V_{DD}$. Finally if $V_1 = V_2 = -V_{DD}$, M_3 and M_4 will be OFF and M_1, M_2 will be ON, hence $V_o = 0$ V. Thus the given CMOS gate satisfies the function of a negative NAND gate.

20. (C) If $V_A = -V_{DD}$ then M_1 is ON and $V_Y = 0$ V. If $V_B = V_C = -V_{DD}$ and $V_A = 0$ V then M_3 and M_2 are ON but M_1 is OFF hence $V_Y = 0$ V. If $V_A = 0$ V and either or both V_B, V_C are 0 V then M_1 is OFF and either or both M_2 and M_3 will be OFF, which implies no current flowing through M_4 hence $V_Y = -V_{DD}$. Thus given circuit satisfies the logic equation $\overline{A + BC}$.

21. (A) Let $V_1 = V_2 = 0$ V $= V(0)$ then M_4 and M_3 will be ON and M_2, M_1 OFF hence $V_o = V_{DD} = V(1)$. Let $V_1 = 0$ V, $V_2 = V_{DD}$ then M_4 and M_2 will be ON but M_3 and M_1 will be OFF hence $V_o = 0 = V(0)$. Let $V_1 = V_{DD}$, $V_2 = 0$ V, then M_4 and M_3 will be OFF and M_1 ON hence $V_o = 0$ V $= V(0)$. Finally if $V_1 = V_2 = V_{DD}$, M_1 and M_2 will be ON but M_4 will be OFF hence $V_o = 0$ V $= V(0)$. Thus the given CMOS satisfy the function of a positive NOR gate.

22. (A) If either one or both the inputs are $V(0) = 0$ V the corresponding FET will be OFF, the voltage across the load FET will be 0 V, hence the output is V_{DD}. If boths inputs are $V(1) = V_{DD}$, both M_1 and M_2 are ON and the output is $V(0) = 0$ V. It satisfy NAND gate.

23. (B) If both the inputs are at $V(0) = 0$ V, the transistor M_1 and M_2 are OFF, hence the output is $V(1) = V_{DD}$. If either one or both of the inputs are at $V(1) = V_{DD}$, the corresponding FET will be ON and the output will be $V(0) = 0$ V. Hence it is a NOR gate.

24. (B) If all inputs A, B and C are HIGH, then input to invertor is LOW and output Y is HIGH. If all inputs are LOW, then input to inverter is also LOW and output Y is HIGH. In all other case the input to inverter is HIGH and output Y is LOW.

Hence $Y = ABC + \overline{A}\overline{B}\overline{C} = ABC + \overline{(A + B + C)}$

25. (C) The operation of circuit is given below

A B C D	P_A P_B P_C P_D	N_A N_B N_C N_D	Y
× × × 1	× × × OFF	× × × ON	LOW
× × 0 0	× × ON ON	× × OFF OFF	HIGH
0 0 1 0	ON ON OFF ON	OFF OFF ON OFF	HIGH
0 1 1 0	ON OFF OFF ON	OFF ON ON OFF	LOW
1 0 1 0	OFF ON OFF ON	ON OFF ON OFF	LOW
1 1 1 0	OFF OFF OFF ON	ON ON ON OFF	LOW

$Y = \overline{(A + B)C + D}$

26. (B) The operation of this circuit is given below :

A B C	P_A P_B P_C	N_A N_B N_C	Y
× × 0	× × ON	× × OFF	HIGH
0 0 1	ON ON OFF	OFF OFF ON	HIGH
× 1 1	× OFF OFF	× ON ON	LOW
1 × 1	OFF × OFF	ON × ON	LOW

$Y = \overline{(A + B)C}$

27. (B) If input E is LOW, output will not be LOW. It must be HIGH. Option (B) satisfy this condition.

28. (A) In this circuit parallel combination are OR gate and series combination are AND gate.

Hence $Y = \overline{(A + B)(C + D)(E + F)}$

29. (A) When an output is HIGH, it may be as low as $V_{OH(min)} = 2.4$ V. The minimum voltage that an input will respond to as a HIGH is $V_{IH(min)} = 2.0$ V. A negative noise spike that can drive the actual voltage below 2.0 V if its amplitude is greater than

$V_{NH} = V_{OH(min)} - V_{IH(min)} = 2.4 - 2.0 = 0.4$ V

30. (A) When an output is LOW, it may be as high as $V_{OL(max)} = 0.4$ V. The maximum voltage that an input will respond to as a LOW is $V_{IL(max)} = 0.8$ V. A positive noise spike can drive the actual voltage above the 0.8 V level if its amplitude is greater than

$V_{NL} = V_{IL(max)} - V_{OL(max)} = 0.8 - 0.4 = 0.4$ V

31. (B) A positive noise spike can drive the voltage above 1.0 V level if the amplitude is greater than

$V_{NL} = V_{IL(max)} - V_{OL(max)} = 1 - 0.1 = 0.9$ V,

A negative noise spike can drive the voltage below 3.5 V if the amplitude is greater than

$V_{NH} = V_{OH(min)} - V_{IH(min)} = 4.9 - 3.5 = 1.4$ V

32. (B) $V_{IH(min)} = V_{OH(min)} - V_{NH} = -0.8 - 0.5 = -1.3$ V

$V_{IL(max)} = V_{OL(max)} + V_{NL} = 0.5 + (-2) = -1.5$ V

33. (C) $V_{NH} = V_{OH(min)} - V_{IH(min)}$, $V_{NL} = V_{IL(max)} - V_{OL(max)}$

$V_{NH} = 2.7$ (for LS) -2.0 (for ALS) $= 0.7$ V

$V_{NL} = 0.8$ (for ALS) -0.5 (for LS) $= 0.3$ V

34. (B) $V_{NH} = 2.5$ (for ALS) $- 2.0$ (for LS) $= 0.5$ V

$V_{NL} = 0.8$ (for LS) $- 0.4$ (for ALS) $= 0.4$ V

35. (D) $V_{NH(min)} = 0.5$ V , $V_{NL(min)} = 0.3$ V

36. (B) fanout (LOW) $= \dfrac{I_{OL(max)}}{I_{IL(max)}} = \dfrac{8m}{0.1m} = 80$

fanout (HIGH) $= \dfrac{I_{OH(max)}}{I_{IH(max)}} = \dfrac{400\mu}{20\mu} = 20$

The fanout is chosen the smaller of the two.

37. (B) In HIGH state the loading on the output of gate 1 is equivalent to six 74LS input load.

Hence load $= 6 \times I_{IH} = 6 \times 20\mu = 120\ \mu A$

38. (C) The NAND gate represent only a single input load in the LOW state. Hence only five loads in the LOW state.

load $= 5I_{IL} = 5 \times 0.4 = 2$ mA

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