CHAPTER

4.1

NUMBER SYSTEMS & BOOLEAN ALGEBRA

1. The 100110_2 is numerically equivalent to

1. 26_{16} 2. 36_{10} 3. 46_8 4. 212_4

The correct answer are

(A) 1, 2, and 3 (B) 2, 3, and 4

(C) 1, 2, and 4 (D) 1, 3, and 4

2. If $(211)_x = (152)_8$, then the value of base x is

(A) 6 (B) 5

(C) 7 (D) 9

3. 11001, 1001 and 111001 correspond to the 2's complement representation of the following set of numbers

(A) 25, 9 and 57 respectively

(B) –6, –6 and –6 respectively

(C) –7, –7 and –7 respectively

(D) –25, –9 and –57 respectively

4. A signed integer has been stored in a byte using 2's complement format. We wish to store the same integer in 16-bit word. We should copy the original byte to the less significant byte of the word and fill the more significant byte with

(A) 0

(B) 1

(C) equal to the MSB of the original byte

(D) complement of the MSB of the original byte.

5. A computer has the following negative numbers stored in binary form as shown. The wrongly stored number is

(A) –37 as 1101 1011 (B) –89 as 1010 0111

(C) –48 as 1110 1000 (D) –32 as 1110 0000

6. Consider the signed binary number $A = 01010110$ and $B = 1110\,1100$ where B is the 1's complement and MSB is the sign bit. In list-I operation is given, and in list-II resultant binary number is given.

List–I	List-II
P. $A + B$	1. 0 1 0 0 0 0 1 1
Q. $B - A$	2. 0 1 1 0 1 0 0 1
R. $A - B$	3. 0 1 0 0 0 0 1 0
S. $-A - B$	4. 1 0 0 1 0 1 0 1
	5. 1 0 1 1 1 1 0 0
	6. 1 0 0 1 0 1 1 0
	7. 1 0 1 1 1 1 0 1
	8. 0 1 1 0 1 0 1 0

The correct match is

	P	Q	R	S
(A)	3	4	2	5
(B)	3	6	8	7
(C)	1	4	8	7
(D)	1	6	2	5

28. The simplified form of a logic function $Y = A(B + C(\overline{AB + AC}))$ is

(A) $\overline{A}\,\overline{B}$ (B) AB

(C) $\overline{A}B$ (D) $A\overline{B}$

29. The reduced form of the Boolean expression of $Y = (\overline{A\overline{B}}) \cdot (\overline{\overline{A}B})$ is

(A) $A + B$ (B) $\overline{A} + \overline{B}$

(C) $A\overline{B} + \overline{A}B$ (D) $\overline{A}\,\overline{B} + AB$

30. If $X\overline{Y} + \overline{X}Y = Z$ then $X\overline{Z} + \overline{X}Z$ is equal to

(A) $\overline{Y}$ (B) Y

(C) 0 (D) 1

31. If $XY = 0$ then $X \oplus Y$ is equal to

(A) $X + Y$ (B) $\overline{X} + \overline{Y}$

(C) XY (D) $\overline{X}\,\overline{Y}$

32. From a four-input OR gate the number of input condition, that will produce HIGH output are

(A) 1 (B) 3

(C) 15 (D) 0

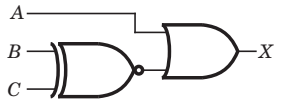
33. A logic circuit control the passage of a signal according to the following requirements :

1. Output X will equal A when control input B and C are the same.

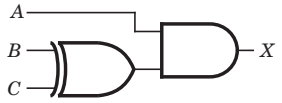
2. X will remain HIGH when B and C are different.

The logic circuit would be

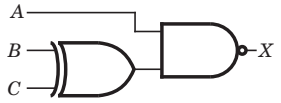
(A)



(B)

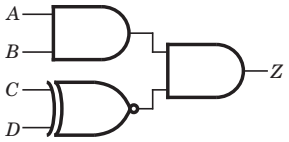


(C)

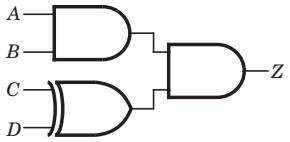


(D)

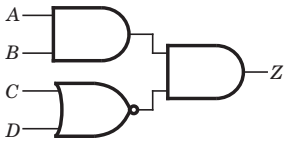
34. The output of logic circuit is HIGH whenever A and B are both HIGH as long as C and D are either both LOW or both HIGH. The logic circuit is



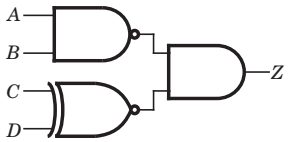
(A)



(B)



(C)



(D)

35. In fig. P.4.1.35 the input condition, needed to produce $X = 1$, is

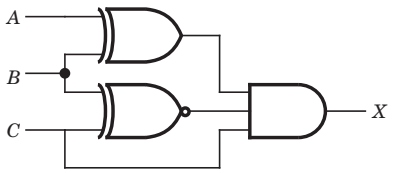


Fig. P4.1.34

(A) $A = 1,\ B = 1,\ C = 0$ (B) $A = 1,\ B = 1,\ C = 1$

(C) $A = 0,\ B = 1,\ C = 1$ (D) $A = 1,\ B = 0,\ C = 0$

36. Consider the statements below:

1. If the output waveform from an OR gate is the same as the waveform at one of its inputs, the other input is being held permanently LOW.

2. If the output waveform from an OR gate is always HIGH, one of its input is being held permanently HIGH.

The statement, which is always true, is

(A) Both 1 and 2 (B) Only 1

(C) Only 2 (D) None of the above

37. To implement $y = ABCD$ using only two-input NAND gates, minimum number of requirement of gate is

(A) 3 (B) 4

(C) 5 (D) 6

38. If the X and Y logic inputs are available and their complements $\overline{X}$ and $\overline{Y}$ are not available, the minimum number of two-input NAND required to implement $X \oplus Y$ is

(A) 4 (B) 5

(C) 6 (D) 7

Statement for Q.39–40:

A Boolean function $Z = A\overline{B}C$ is to be implement using NAND and NOR gate. Each gate has unit cost. Only A, B and C are available.

39. If both gate are available then minimum cost is

(A) 2 units (B) 3 units

(C) 4 units (D) 6 units

40. If NAND gate are available then minimum cost is

(A) 2 units (B) 3 units

(C) 4 units (D) 6 units

41. In fig. P4.1.41 the LED emits light when

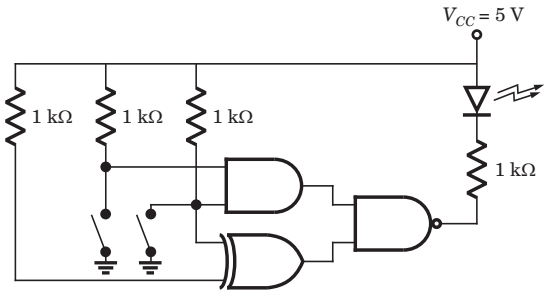


Fig. P4.1.41

(A) both switch are closed

(B) both switch are open

(C) only one switch is closed

(D) LED does not emit light irrespective of the switch positions

42. If the input to the digital circuit shown in fig. P.4.1.42 consisting of a cascade of 20 XOR gates is X, then the output Y is equal to

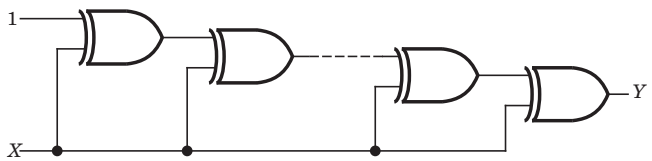


Fig. P4.1.42

(A) X (B) $\overline{X}$

(C) 0 (D) 1

43. A Boolean function of two variables x and y is defined as follows :

$$f(0, 0) = f(0, 1) = f(1, 1) = 1;\ f(1, 0) = 0$$

Assuming complements of x and y are not available, a minimum cost solution for realizing f using 2-input NOR gates and 2-input OR gates (each having unit cost) would have a total cost of

(A) 1 units (B) 2 units

(C) 3 units (D) 4 units

44. The gates G_1 and G_2 in Fig. P.4.2.44 have propagation delays of 10 ns and 20 ns respectively.

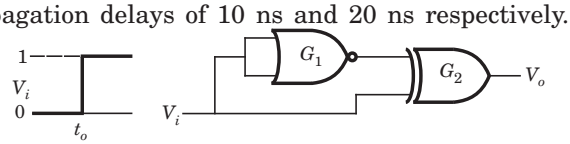
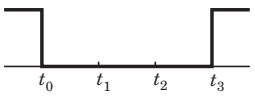


Fig. P4.1.44

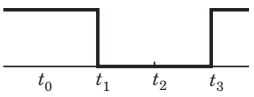
If the input V_i makes an abrupt change from logic 0 to 1 at $t = t_0$ then the output waveform V_o is

$[t_1 = t_0 + 10 \text{ ns},\ t_2 = t_1 + 10 \text{ ns},\ t_3 = t_2 + 10 \text{ ns}]$

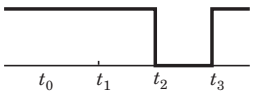
(A)



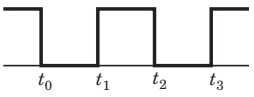
(B)



(C)



(D)



45. In the network of fig. P4.1.45 f can be written as

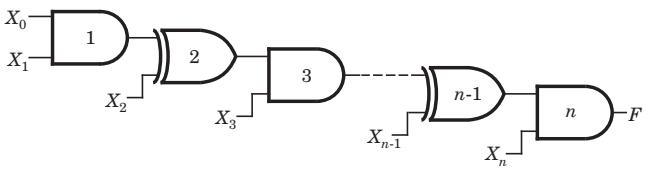


Fig. P4.1.45

(A) $X_0X_1X_3X_5 + X_2X_4X_5 \ldots X_{n-1} + \ldots X_{n-1}X_n$

(B) $X_0X_1X_3X_5 + X_2X_3X_4 \ldots X_n + \ldots X_{n-1}X_n$

(C) $X_0X_1X_3X_5 \ldots X_n + X_2X_3X_5 \ldots X_n + \ldots + X_{n-1}X_n$

(D) $X_0X_1X_3X_5 \ldots X_{n-1} + X_2X_3X_5 \ldots X_n + \ldots + X_{n-1}X_{n-2} + X_n$

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SOLUTIONS

1. (D) $100110_2 = 2^5 + 2^2 + 2^1 = 38_{10}$

$26_{16} = 2 \times 16 + 6 = 38_{10}$

$46_8 = 4 \times 8 + 6 = 38_{10}$

$212_4 = 2 \times 4^2 + 4^1 = 38_{10}$

So 36_{10} is not equivalent.

2. (C) $2x^2 + x + 1 = 64 + 5 \times 8 + 2 \quad \Rightarrow \quad x = 7$

3. (C) All are 2's complement of 7

$$\begin{array}{lcrl} 11001 & \Rightarrow & 00110 & \\ & & +\ \ 1 & \\ \hline & & 00111 & = 7_{10} \\ 1001 & \Rightarrow & 0110 & \\ & & +\ \ 1 & \\ \hline & & 0111 & = 7_{10} \\ 111001 & \Rightarrow & 000110 & \\ & & +\ \ 1 & \\ \hline & & 000111 & = 7_{10} \end{array}$$

4. (C) See a example

42 in a byte 0 0 1 0 1 0 1 0

42in a word 0 0 0 0 0 0 0 0 0 0 1 0 1 0 1 0

–42 in a byte 1 1 0 1 0 1 1 0

–42 in a word 1 1 1 1 1 1 1 1 1 1 0 1 0 1 1 0

Therefore (C) is correct.

5. (C) $48_{10} = 00110000_2$

$$\begin{array}{rr} -48_{10} = & 1100\,1111 \\ & +\ \ \ \ \ 1 \\ \hline & 11010000 \end{array}$$

6. (D) Here $\overline{A}$, $\overline{B}$ are 1's complement

$$A + B, \quad \begin{array}{rr} A & 01010110 \\ B & +\ 1110\,1100 \\ \hline & 10100\,0010, \\ & +\ \ \ \ \ \ 1 \\ \hline & 0100\,0011 \end{array}$$

$$B - A = B + \overline{A}, \quad \begin{array}{rr} B & 1110\,1100 \\ \overline{A} & +\ 1010\,1001 \\ \hline & 110010101 \\ & +\ \ \ \ \ \ 1 \\ \hline & 10010110 \end{array}$$

$$A - B = A + \overline{B}, \quad \begin{array}{rr} A & 010\,10110 \\ \overline{B} & +\ 00010011 \\ \hline & 0110\,1001 \end{array}$$

$$-A - B = \overline{A} + \overline{B}, \quad \begin{array}{rr} \overline{A} & 1010\,1001 \\ \overline{B} & +\ 00010011 \\ \hline & 10111100 \end{array}$$

7. (B) Here $\overline{A}$, $\overline{B}$ are 2's complement

$$A + B, \quad \begin{array}{rr} A & 01000110 \\ B & +\ 11010011 \\ \hline & 1\ 0001\,1001 \end{array}$$

Discard the carry 1

$$A - B = A + \overline{B}, \quad \begin{array}{rr} A & 01000110 \\ \overline{B} & +\ 0010\,1101 \\ \hline & 0111\,0011 \end{array}$$

$$B - A, \quad \begin{array}{rr} B & 1101\,0011 \\ \overline{A} & +\ 1011\,1010 \\ \hline & 1\ 1000\,1101 \end{array}$$

Discard the carry 1

$$-A - B = \overline{A} + \overline{B}, \quad \begin{array}{rr} \overline{A} & 1011\,1010 \\ \overline{B} & +\ 0010\,1101 \\ \hline & 1110\,0111 \end{array}$$

8. (B) $11_{10} = 1011_2$

0.3	$2F_{i-1}$	B_i	F_i
	0.6	0	0.6
	1.2	1	0.2
	0.4	0	0.4
	0.8	0	0.8
	1.6	1	0.6

Repeat from the second line $0.3_{10} = 0.\overline{01001}_2$

9. (C)

	b_4	b_3	b_2	p_3	b_1	p_2	p_1
Received	1	1	0	1	1	0	0

$C_1^* = b_4 \oplus b_2 \oplus b_1 \oplus p_1 = 0$

$C_2^* = b_4 \oplus b_3 \oplus b_1 \oplus p_2 = 1$

$C_3^* = b_4 \oplus b_3 \oplus b_2 \oplus p_3 = 1$

$C_3^* C_2^* C_1^* =$ 110 which indicate position 6 in error Transmitted code 1001100.

10. (D) $X = MNQ + M\overline{N}Q + \overline{M}NQ$

$= MQ + \overline{M}NQ = Q(M + \overline{M}N) = Q(M + N)$

11. (A) The logic circuit can be modified as shown in fig. S. 4.1.11

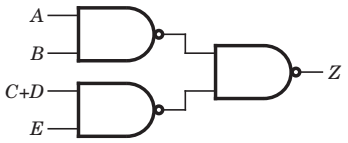


Fig. S4.1.11

Now $Z = AB + (C + D)E$

12. (D) You can see that input to last XNOR gate is same. So output will be HIGH.

13. (D) $Z = \overline{A} + (\overline{AB} + \overline{BC}) + \overline{C}$

$= \overline{A} + (\overline{A} + \overline{B} + \overline{B} + \overline{C}) + \overline{C} = \overline{A} + \overline{B} + \overline{C}$

$\overline{ABC} = \overline{A} + \overline{B} + \overline{C}$

$\overline{AB} + \overline{BC} + \overline{AC} = \overline{A} + \overline{B} + \overline{B} + \overline{C} + \overline{A} + \overline{C} = \overline{A} + \overline{B} + \overline{C}$

14. (C) $(X + \overline{Y})(\overline{X} + Y) = XY + \overline{X}\,\overline{Y}$

$(X + Y)(X + \overline{Y})(\overline{X} + Y) = (X + Y)(XY + \overline{X}\,\overline{Y})$

$= XY + XY = XY$

15. (B) Using duality

$(A + B)(\overline{A} + C)(B + C) = (A + B)(\overline{A} + C)$

Thus (B) is correct option.

16. (B) $Z = \overline{(\overline{AB})(\overline{CD})(\overline{EF})} = AB + CD + EF$

17. (A) $X = (A\,\overline{B} + \overline{A}B)\overline{(A + \overline{B})} = (A\overline{B} + \overline{A}\,B)(\overline{A}B) = \overline{A}B$

18. (B) $Y = \overline{(A \oplus B) \cdot C} = \overline{(A\overline{B} + \overline{A}C) \cdot C}$

$= \overline{(A\overline{B} + \overline{A}B)} + \overline{C} = \overline{A}\,\overline{B} + AB + \overline{C}$

19. (C) $Z = A(A + \overline{A})BC = ABC$

20. (A) $Z = AB(\overline{B} + C) = ABC$

21. (A) $Z = \overline{(\overline{A} + \overline{B})} \cdot BC = (AB) \cdot BC = ABC$

22. (A) $A(A + \overline{B})(A + \overline{B} + C)$

$= (AA + A\overline{B})(A + \overline{B} + C) = A(A + \overline{B} + C) = A$

Therefore No gate is required to implement this function.

23. (A)

A	B	C	$(A + BC)$	$(A + B)(A + C)$
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1

Fig. S 4.1.23

24. (B) $\overline{X} = \overline{A}\,\overline{B}C + A\overline{B}C + AB\overline{C} = \overline{B}C + AB\overline{C}$

25. (B) $\overline{(A + B)}\,\overline{(B + \overline{C})} = (\overline{A}\,\overline{B})(\overline{B}C) = \overline{A}\,\overline{B}C$

$\overline{(A + B)}\,\overline{(B + \overline{C})} = (A + B) + (B + \overline{C}) = A + B + \overline{C}$

$\overline{(\overline{A} + B)}\,\overline{(B + \overline{C})} = \overline{(\overline{A} + B)} + (B + C)$

$= A\overline{B} + B + C = A + B + C$

From truth table $Z = A + B + \overline{C}$

Thus (B) is correct.

26. (D) $AC + B\overline{C} = AC(B + \overline{B}) + (A + \overline{A})B\overline{C}$

$= ABC + A\overline{B}C + AB\overline{C} + \overline{A}B\overline{C}$

27. (D) $F = A + \overline{A}B + \overline{A}\,\overline{B}C + \overline{A}\,\overline{B}\,\overline{C}(D + \overline{D}E)$

$= A + \overline{A}B + \overline{A}\,\overline{B}(C + \overline{C}(D + E))$

$= A + \overline{A}(B + \overline{B}(C + D + E)) = A + B + C + D + E$

28. (B) $A(B + C\,\overline{(AB + AC)}) = AB + AC\,(\overline{AB} \cdot \overline{AC})$

$= AB + AC[(\overline{A} + \overline{B})(\overline{A} + \overline{C})]$

$= AB + AC\,(\overline{A} + \overline{A}\,\overline{C} + \overline{A}\overline{B} + \overline{B}\,\overline{C}) = AB$

29. (C) $\overline{\overline{(A\overline{B})} \cdot \overline{(\overline{A}B)}} = \overline{\overline{A\overline{B}}} + \overline{\overline{\overline{A}B}} = A\overline{B} + \overline{A}B$

30. (B) $X\overline{Z} + \overline{X}Z = X\overline{(X\overline{Y} + \overline{X}Y)} + \overline{X}(X\overline{Y} + \overline{X}Y)$

$= X(XY + \overline{X}\,\overline{Y}) + \overline{X}Y = XY + \overline{X}Y = Y$

31. (A) $X \oplus Y = X\overline{Y} + \overline{X}Y = \overline{(XY + \overline{X}\overline{Y})} = \overline{(\overline{X}\overline{Y})} = X + Y$

(A) $(\overline{w} + y)(x + \overline{y} + z)(w + x + z)$

(B) $(w + \overline{x})(w + \overline{z})(\overline{x} + \overline{y})(\overline{y} + \overline{z})$

(C) $(x + z)(\overline{w} + y)$

(D) $(\overline{x} + \overline{z})(w + \overline{y})$

7. A function with don't care condition is as follows

$$f(a, b, c, d) = \Sigma m(0, 2, 3, 5, 7, 8, 9, 10, 11) + \Sigma dc(4, 15)$$

The minimized expression for this function is

(A) $a\overline{b} + \overline{b}\,\overline{d} + cd + \overline{a}b\overline{c}$ (B) $a\overline{b} + \overline{b}\,\overline{d} + cd + \overline{a}b\overline{d}$

(C) $a\overline{b} + \overline{b}\,\overline{d} + \overline{b}\,c + \overline{a}bd$ (D) Above all

8. A function with don't cares is as follows :

$$g(X, Y, Z) = \Sigma m(5, 6) + \Sigma dc(1, 2, 4)$$

For above function consider following expression

1. $XY\overline{Z} + X\overline{Y}Z$ 2. $X\overline{Y} + X\overline{Z}$

3. $X\overline{Z} + \overline{X}Z + \overline{Y}Z$ 4. $Y\overline{Z} + \overline{Y}Z$

The solution for g are

(A) 1, 2, and 3 (B) 1, 2, and 4

(C) 1, and 4 (D) 1, and 3

9. A logical function of four variable is given as

$$f(A, B, C, D) = (\overline{A} + B\,C)(B + CD)$$

The function as a sum of product is

(A) $\overline{A} + BC + A\overline{C}D + BCD$

(B) $\overline{A} + BC + \overline{A}CD + BCD$

(C) $\overline{A}B + BC + \overline{A}CD + BCD$

(D) $AB + A\overline{B} + A\overline{C}D + BCD$

10. A combinational circuit has input $A, B,$ and C and its K-map is as shown in fig. P4.2.10. The output of the circuit is given by

		CD			
		00	01	11	10
A	00		1		1
	01	1		1	

Fig. P4.2.1

(A) $(\overline{A}B + A\overline{B})\overline{C}$ (B) $(AB + \overline{A}\overline{B})\overline{C}$

(C) $\overline{A}\overline{B}\overline{C}$ (D) $A \oplus B \oplus C$

11. The Boolean Expression $Y = (A + B)(\overline{A} + C)$ is equal to

(A) $AC + \overline{A}B$ (B) $AC + \overline{A}B + BC$

(C) $\overline{A}B + BC + A\overline{B}C$ (D) Above all

12. In the logic circuit of fig. P4.2.12 the redundant gate is

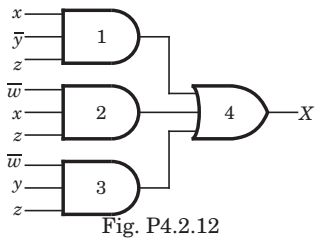


Fig. P4.2.12

(A) 1 (B) 2

(C) 3 (D) 4

13. If function W, X, Y, and Z are as follow

$$W = R + \overline{P}Q + \overline{R}S$$

$$X = PQ\overline{R}\overline{S} + \overline{P}\,\overline{Q}\,\overline{R}\overline{S} + P\overline{Q}\,\overline{R}\,\overline{S}$$

$$Y = RS + \overline{PR + P\overline{Q} + \overline{P}\,\overline{Q}}$$

$$Z = R + S + \overline{PQ + \overline{P}\overline{Q}\,\overline{R} + P\overline{Q}\,\overline{S}}$$

Then

(A) $W = Z,\ X = \overline{Z}$ (B) $W = Z,\ X = Y$

(C) $W = Y$ (D) $W = Y = \overline{Z}$

14. In a certain application four inputs A, B, C, D are fed to logic circuit, producing an output which operates a relay. The relay turns on when $f(A, B, C, D) = 1$ for the following states of the inputs ($ABCD$) : 0000, 0010, 0101, 0110, 1101 and 1110. States 1000 and 1001 do not occur, and for the remaining states the relay is off. The minimized Boolean expression f is

(A) $\overline{A}C\overline{D} + BC\overline{D} + B\overline{C}D$ (B) $\overline{B}\overline{C}D + BC\overline{D} + \overline{A}C\overline{D}$

(C) $ABD + \overline{B}C\overline{D} + \overline{B}\overline{C}D$ (D) $\overline{A}\overline{B}\overline{D} + B\overline{C}D + BC\overline{D}$

15. There are four Boolean variables x_1, x_2, x_3 and x_4. The following function are defined on sets of them

$$f(x_3, x_2, x_1) = \Sigma m(3, 4, 5)$$

$$g(x_4, x_3, x_2) = \Sigma m(1, 6, 7)$$

$$h(x_4, x_3, x_2, x_1) = fg$$

Then $h(x_4, x_3, x_2, x_1)$ is

(A) $\Sigma m(3, 12, 13)$ (B) $\Sigma m(3, 6)$

(C) $\Sigma m(3, 12)$ (D) 0

Statement for Q.16–17:

A switching function of four variable, $f(w, x\ y, z)$ is to equal the product of two other function f_1 and f_2, of the same variable $f = f_1 f_2$. The function f and f_1 are as follows :

$f = \Sigma m(4, 7, 15)$

$f_1 = \Sigma m(0, 1, 2, 3, 4, 7, 8, 9, 10, 11, 15)$

16. The number of full specified function, that will satisfy the given condition, is

(A) 32 (B) 16

(C) 4 (D) 1

17. The simplest function for f_2 is

(A) x (B) $\bar{x}$

(C) y (D) $\bar{y}$

18. A four-variable switching function has minterms m_6 and m_9. If the literals in these minterms are complemented, the corresponding minterm numbers are

(A) m_3 and m_0 (B) m_9 and m_6

(C) m_2 and m_0 (D) m_6 and m_9

19. The minimum function that can detect a "divisible by 3" 8421 BCD code digit (representation $D_8D_4D_2D_1$) is given by

(A) $D_8D_1 + D_4D_2 + D_8D_2D_1$

(B) $D_8D_1 + D_4D_2\overline{D}_1 + \overline{D}_4D_2D_1 + \overline{D}_8\overline{D}_4\overline{D}_2\overline{D}_1$

(C) $D_4D_1 + D_4D_2 + D_8\overline{D}_1\overline{D}_2D_1$

(D) $D_4D_2\overline{D}_1 + \overline{D}_4D_2D_1 + D_8D_4D_2D_1$

20. $f(x_2\ ,\ x_1\ ,\ x_0) = ?$

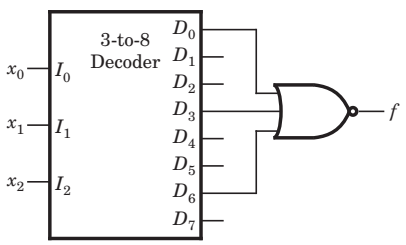


Fig. P4.2.21

(A) $\Pi(1, 2, 4, 5, 7)$ (B) $\Sigma(1, 2, 4, 5, 7)$

(C) $\Sigma(0, 3, 6)$ (D) None of Above

21. For a binary half subtractor having two input A and B, the correct set of logical expressions for the outputs $D = (A - B)$ and X (borrow) are

(A) $D = AB + \overline{A}\overline{B}$, $X = \overline{A}B$

(B) $D = \overline{A}B + A\overline{B}$, $X = A\overline{B}$

(C) $D = \overline{A}B + A\overline{B}$, $X = \overline{A}B$

(D) $D = AB + \overline{A}\overline{B}$, $X = A\overline{B}$

22. $f_1 f_2 = ?$

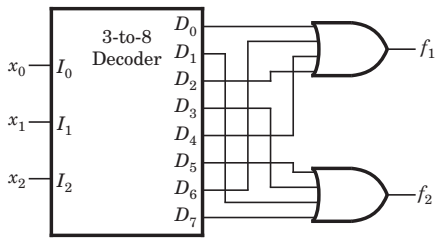


Fig. P4.2.22

(A) $x_0x_1x_2$ (B) $x_0 \oplus x_1 \oplus x_2$

(C) 1 (D) 0

23. The logic circuit shown in fig. P4.2.23 implements

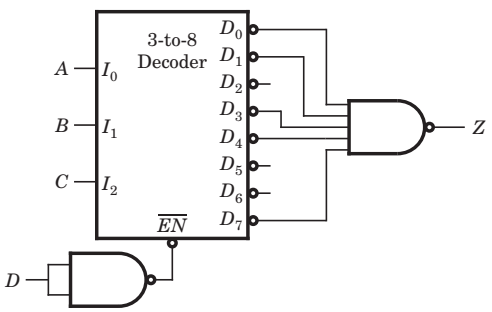


Fig. P4.2.23

(A) $D(A \cup C + \overline{A}\overline{C})$ (B) $D(B \oplus C + \overline{A}\overline{C})$

(C) $D(B \oplus C + \overline{A}\overline{B})$ (D) $D(B \cup C + \overline{A}\overline{B})$

Statement for Q.24–25:

The building block shown in fig. P4.2.24–25 is a active high output decoder.

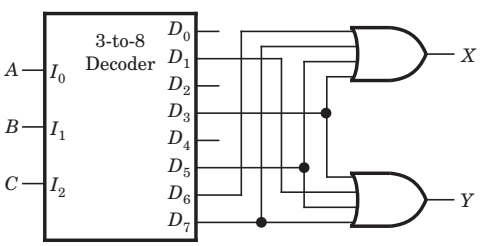


Fig. P4.2.24-25

24. The output X is

(A) $AB + BC + CA$ (B) $A + B + C$

(C) ABC (D) None of the above

25. The output Y is

(A) $A + B$ (B) $B + C$

(C) $C + A$ (D) None of the above

26. A logic circuit consist of two 2×4 decoder as shown in fig. P4.2.26.

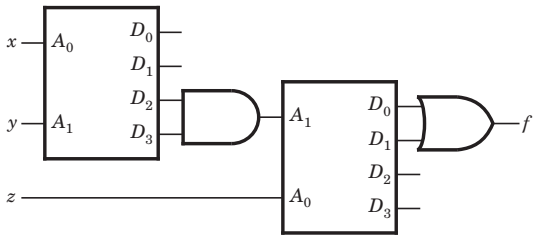


Fig. P4.2.26

The output of decoder are as follow

$D_0 = 1$ when $A_0 = 0, \quad A_1 = 0$

$D_1 = 1$ when $A_0 = 1, \quad A_1 = 0$

$D_2 = 1$ when $A_0 = 0, \quad A_1 = 1$

$D_3 = 1$ when $A_0 = 1, \quad A_1 = 1$

The value of $f(x,\ y,\ z)$ is

(A) 0 (B) z

(C) $\bar{z}$ (D) 1

Statement for Q.27-29:

A MUX network is shown in fig. P4.2.27-29.

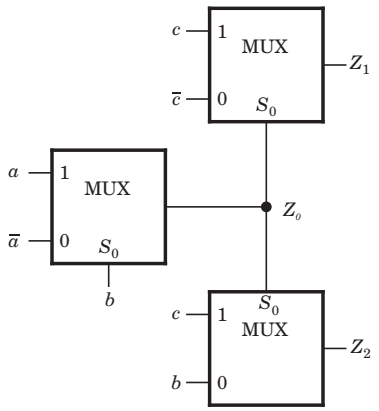


Fig. P4.2.27-29

27. $Z_1 = ?$

(A) $a + b + c$ (B) $ab + ac + bc$

(C) $a \cup b \cup c$ (D) $a \oplus b \oplus c$

28. $Z_2 = ?$

(A) $ab + bc + ca$ (B) $a + b + c$

(C) abc (D) $a \cup b \cup c$

29. This circuit act as a

(A) Full adder (B) Half adder

(C) Full subtractor (D) Half subtractor

30. The network shown in fig. P4.2.30 implements

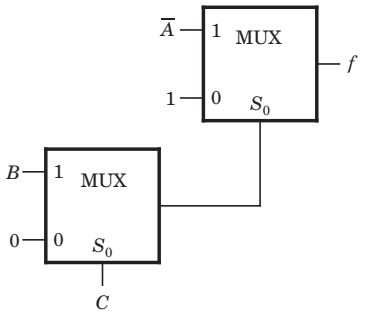


Fig. P4.2.30

(A) NOR gate (B) NAND gate

(C) XOR gate (D) XNOR gate

31. The MUX shown in fig. P4.2.31 is 4×1 multiplexer. The output Z is

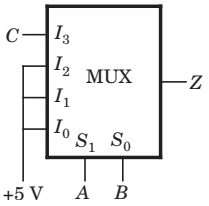


Fig. P4.2.31

(A) ABC B) $A \oplus B \oplus C$

(C) $A \cup B \cup C$ (D) $A + B + C$

32. The output of the 4×1 multiplexer shown in fig. P4.2.32 is

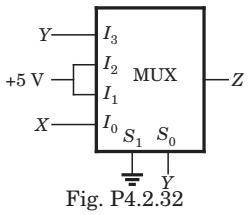


Fig. P4.2.32

(A) $X + Y$ (B) $\overline{X} + \overline{Y}$

(C) $\overline{XY} + X$ (D) $X\overline{Y}$

33. The MUX shown in fig. P4.2.33 is a 4×1 multiplexer. The output Z is

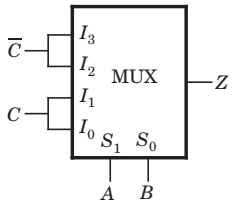


Fig. P4.2.33

(A) $A \oplus C$ (B) $A \cup C$

(C) $B \oplus C$ (D) $B \cup C$

34. f =?

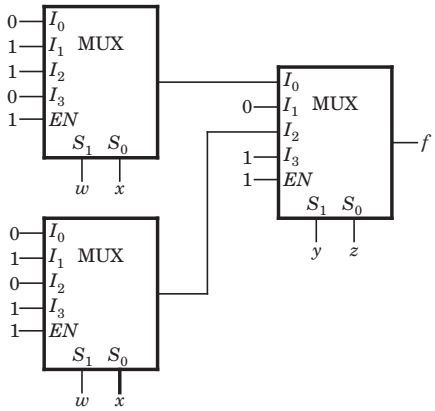


Fig. P4.2.34

(A) $\overline{w}x\overline{y}\overline{z} + w\overline{x}\overline{y}\overline{z} + xy + yz$

(B) $w\overline{x}yz + \overline{w}xyz + \overline{x}\,\overline{y} + \overline{y}\overline{z}$

(C) $w\overline{x}\,\overline{y}\overline{z} + \overline{w}\,\overline{x}\,\overline{y}z + y\overline{z} + zx$

(D) $\overline{w}xyz + wxy\overline{z} + gz + \overline{z}\overline{x}$

35. For the logic circuit shown in fig. P4.2.35 the output Y is

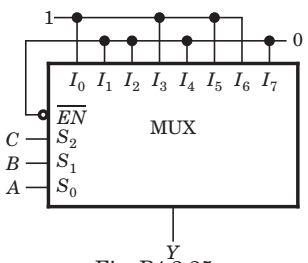


Fig. P4.2.35

(A) $A \oplus B$ (B) $\overline{A \oplus B}$

(C) $A \oplus B \oplus C$ (D) $\overline{A \oplus B \oplus C}$

36. The 4–to–1 multiplexer shown in fig. P4.2.36 implements the Boolean expression

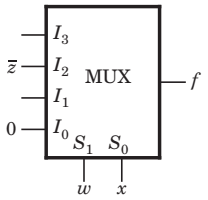


Fig. P4.2.36

$f(w, x, y, z) = \Sigma m(4, 5, 7, 8, 10, 12, 15)$

The input to I_1 and I_3 will be

(A) $y\overline{z}$, $\overline{y} + \overline{z}$ (B) $\overline{y} + z$, $y \cup z$

(C) $\overline{y} + z$, $y \oplus z$ (D) $x + \overline{y}$, $y \oplus z$

37. The 8-to-1 multiplexer shown in fig. P4.2.37 realize the following Boolean expression

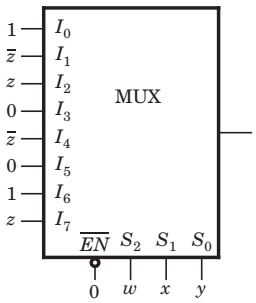


Fig. P4.2.37

(A) $w\overline{x}z + \overline{w}\,\overline{x}\,\overline{z} + wyz + x\overline{y}\,\overline{z}$

(B) $wxz + \overline{w}yz + wy\overline{z} + \overline{w}\,\overline{x}\,\overline{y}$

(C) $\overline{w}\,\overline{x}\,\overline{z} + w\overline{y}\,\overline{z} + \overline{w}\,\overline{y}z + wxz$

(D) MUX is not enable

Statement for Q.38-40:

A PLA realization is shown in fig. P4.2.38–40

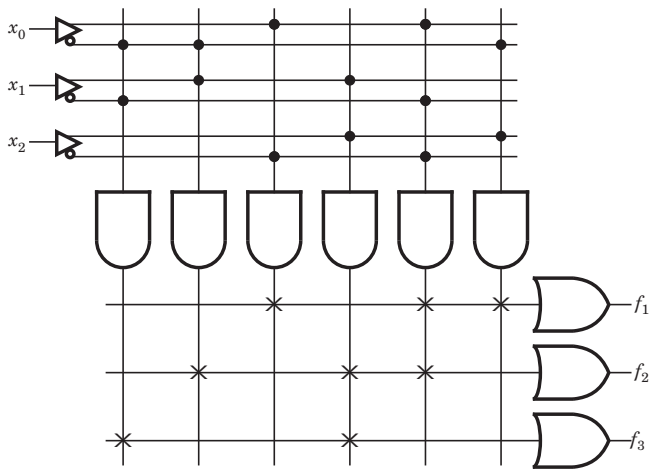


Fig. P.4.2.38-40

38. $f_1(x_2, x_1, x_0) = ?$

(A) $x_2\bar{x}_0 + x_1x_0$ (B) $x_2x_0 + x_1\bar{x}_2$

(C) $x_2 \oplus x_0$ (D) $x_2 \cup x_0$

39. $f_2(x_2, x_1, x_0) = ?$

(A) $\Sigma m(1, 2, 5, 6)$ (B) $\Sigma m(1, 2, 6, 7)$

(C) $\Sigma m(2, 3, 4)$ (D) None of the above

40. $f_3(x_2, x_1, x_0) = ?$

(A) $\Pi M(0, 4, 6, 7)$ (B) $\Pi M(2, 4, 5,7)$

(C) $\Pi M(1, 2, 3, 5)$ (D) $\Pi M(2, 3, 4, 7)$

41. If the input $X_3X_2X_1X_0$ to the ROM in fig. P4.2.41 are 8–4–2–1 BCD numbers, then output $Y_3Y_2Y_1Y_0$ are

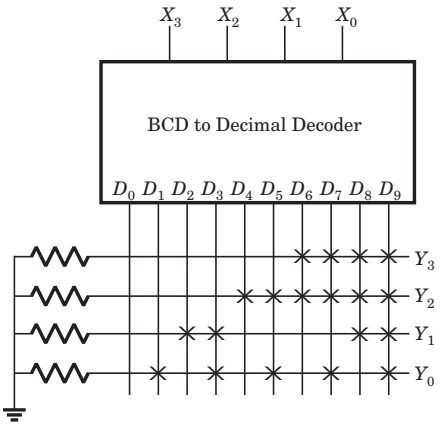


Fig. P4.2.41

(A) 2–4–2–1 BCD number (B) gray code number

(C) excess 3 code converter (D) none of the above

42. It is desired to generate the following three Boolean function

$$f_1 = a\bar{b}c + \bar{a}b\bar{c} + bc$$
$$f_2 = a\bar{b}c + ab + \bar{a}b\bar{c},$$
$$f_3 = \bar{a}\bar{b}\bar{c} + abc + \bar{a}c$$

by using an OR gate array as shown in fig. P4.2.42 where P_1 and P_5 are the product terms in one or more of the variable $a, \bar{a}, b, \bar{b}, c$ and $\bar{c}$.

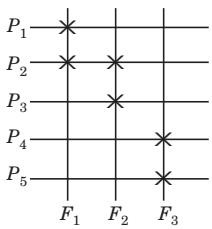


Fig. P4.2.42

The terms P_1, P_2, P_3, P_4 and P_5 are

(A) $\bar{a}b, ac, b\bar{c}, bc, \bar{a}\bar{b}$ (B) $a\bar{b}, b\bar{c}, ac, \bar{a}\bar{b}, bc$

(C) $ac, \bar{a}b, b\bar{c}, \bar{a}\bar{b}, bc$ (D) Above all

43. The circuit shown in fig. P.4.2.43 has 4 boxes each described by input P, Q, R and output Y, Z with $Y = P \oplus Q \oplus R$ and $Z = RQ + \bar{P}R + Q\bar{P}$.

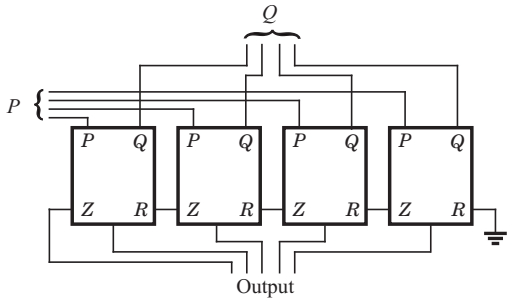


Fig. P4.2.43

The circuit act as a 4 bit

(A) adder giving $P + Q$

(B) subtractor giving $P - Q$

(C) subtractor giving $Q - P$

(D) adder giving $P + Q + R$

44. The circuit shown in fig. P4.2.44 converts

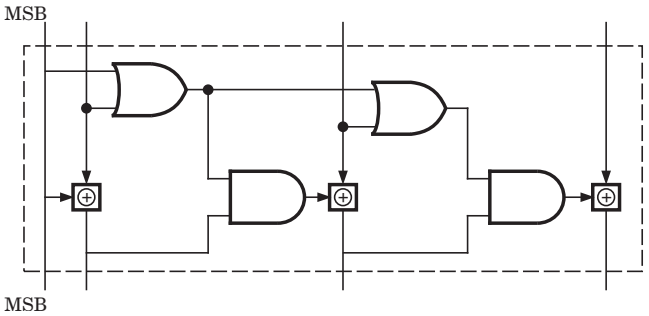


Fig. P4.2.44

(A) BCD to binary code

(B) Binary to excess

(C) Excess–3 to Gray Code

(D) Gray to Binary code

****

PQ \ RS	00	01	11	10
00			1	
01	1	1	1	1
11	1	1	1	
10			1	

Fig. S 4.2.13c

$Z = R + S + \overline{PQ + \overline{P}\,\overline{Q}\,\overline{R} + P\overline{Q}S} = R + S + \overline{PQ}\,\overline{\overline{P}\,\overline{Q}\,\overline{R}}\,\overline{P\overline{Q}\,\overline{S}}$

$= R + S + (\overline{P} + \overline{Q})(P + Q + R)(\overline{P} + Q + S)$

$= R + S + (\overline{P}Q + \overline{P}R + \overline{Q}P + \overline{Q}R)(\overline{P} + Q + S)$

$= R + S + \overline{P}Q + \overline{P}QS + \overline{P}R + \overline{P}RQ + \overline{P}RS + \overline{Q}PS + \overline{Q}\overline{P}R + \overline{Q}RS$

PQ \ RS	00	01	11	10
00		1	1	1
01	1	1	1	1
11		1	1	1
10		1	1	1

Fig. S 4.2.13d

$= R + S + \overline{P}Q$

We can see that $W = Z, \quad X = \overline{Z}$

14. (D) $\overline{A}\overline{B}\overline{D} + B\overline{C}D + BC\overline{D}$

AB \ CD	00	01	11	10
00	1			1
01		1		1
11		1		1
10	×	×		

Fig. S 4.2.14

15. (A) $f = \overline{x}_3x_2x_1 + x_3\overline{x}_2\overline{x}_1 + x_3\overline{x}_2x_1 = \overline{x}_3x_2x_1 + x_3\overline{x}_2$

$g = \overline{x}_4\overline{x}_3x_2 + x_4x_3\overline{x}_2 + x_4x_3x_2 = \overline{x}_4\overline{x}_3x_2 + x_4x_3$

$fg = \overline{x}_4\overline{x}_3x_2x_1 + x_4x_3\overline{x}_2$

$= \overline{x}_4\overline{x}_3x_2x_1 + x_4x_3\overline{x}_2\overline{x}_1 + x_4x_3\overline{x}_2x_1$

$h = \Sigma m(3, \ 12, \ 13)$

16. (A) $f = \Sigma m(4, \ 7, \ 15)$,

$f_1 = \Sigma m(0, \ 1, \ 2, \ 3, \ 4, \ 7, \ 8, \ 9, \ 10, \ 11, \ 15)$

$f_2 = \Sigma m(4, \ 7, \ 15) + \Sigma dc(5, \ 6, \ 12, \ 13, \ 14)$

There are 5 don't care condition. So $2^5 = 32$ different functions f_2 .

17. (A) $f_2 = \Sigma m(4, \ 7, 15) + \Sigma dc(5, \ 6, \ 12, \ 13, \ 14), \ f_2 = x$

wx \ yz	00	01	11	10
00	0	0	0	0
01	1	×	1	×
11	×	×	1	×
10	0	0	0	0

Fig. S 4.2.17

18. (B) $m_6 = \overline{A}BC\overline{D}$, $\quad m_9 = A\overline{B}\overline{C}D$

After complementing literal

$m_6' = A\overline{B}\overline{C}D = m_9$, $\quad m_9' = \overline{A}BC\overline{D} = m_6$

19. (B) 0, 3, 6 and 9 are divisible by 3

D_8D_4 \ D_2D_1	00	01	11	10
00	1		1	
01				1
11	×	×	×	×
10		1	×	×

Fig. S 4.2.19

$f = D_8D_1 + D_4D_2\overline{D}_1 + \overline{D}_4D_2D_1 + \overline{D}_8\,\overline{D}_4\,D_2\,D_1$

20. (B) $f = \overline{\Sigma m(0, \ 3, \ 6)} = \Sigma m(1, \ 2, \ 4, \ 5, \ 7)$

21. (C) $D = A\overline{B} + \overline{A}B, \quad X = \overline{A}B$

A	B	D	X
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Fig. S 4.2.20

22. (D) $f_1 = \Sigma m(0, 2, 4, 6)$,
$f_2 = \Sigma m(1, 3, 5, 7)$, $f_1 f_2 = 0$

23. (D) $Z = D(\overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}BC + A\overline{B}\overline{C} + ABC)$
$= D(\overline{A}\overline{B}(\overline{C} + C) + BC(\overline{A} + A) + A\overline{B}\overline{C})$
$= D(\overline{A}\overline{B} + BC + A\overline{B}\overline{C}) = D(\overline{B}(\overline{A} + A\overline{C}) + BC)$
$= D(\overline{B}\overline{A} + \overline{B}\overline{C} + BC) = D(B \cup C + \overline{A}\overline{B})$

24. (A) $X = \Sigma m(3, 5, 6, 7)$, $X = AB + BC + CA$

25. (D) $Y = \Sigma m(1, 3, 5, 7)$, $Y = C$

		BC			
		00	01	11	10
A	00			1	
	01		1	1	1

Fig. S4.2.24

26. (D) $D_0 = \overline{A}_1\overline{A}_0$, $D_1 = \overline{A}_1 A_0$, $D_2 = A_1\overline{A}_0$,

		BC			
		00	01	11	10
A	00		1	1	
	01		1	1	

Fig. S4.2.25

$D_3 = A_1 A_0$
For first decoder $A_0 = x$, $A_1 = y$, $D_2 = y\overline{x}$, $D_3 = xy$
For second decoder $A_1 = D_2 D_3 = y\overline{x}xy = 0$, $A_0 = z$
$f = D_0 + D_1 = \overline{A}_1\overline{A}_0 + \overline{A}_1 A_0 = \overline{A}_1 = 1$

27. (D) The output of first MUX is
$Z_o = ab + \overline{a}\overline{b} = \overline{(a \oplus b)}$
This is input to select S_0 of both second-level MUX
$Z_1 = CS_0 + \overline{C}\overline{S_0} = C \oplus \overline{S}_0 = a \oplus b \oplus c$

28. (A) $Z_2 = bS_0 + c\overline{S}_0$
$= b(ab + \overline{a}\overline{b}) + c(\overline{a}b + a\overline{b}) = ab + a\overline{b}c + \overline{a}bc$
$= a(b + \overline{b}c) + \overline{a}bc = ab + ac + \overline{a}bc$
$= ab + ac + bc$

29. (A) The equation of Z_1 is the equation of sum of A and B with carry and equation of 2 is the resultant carry. Thus, it is a full adder.

30. (B) $f_1 = \overline{C}D + CB = CB$, $S = F_1$
$f = \overline{f}_1 + f_1\overline{A} = \overline{CB} + CB\overline{A} = \overline{CB} + \overline{A}$
$= \overline{C} + \overline{B} + \overline{A} = \overline{ABC}$

31. (D) $Z = \overline{A}\overline{B}C + \overline{A}B + A\overline{B} + AB$
$= \overline{A}(\overline{B}C + B) + A(\overline{B} + B) = \overline{A}(B + C) + A = A + B + C$

32. (A) $Z = \overline{X}Y + X\overline{Y} + XY$, $Z = X + Y$

33. (A) $Z = \overline{A}\overline{B}C + \overline{A}BC + A\overline{B}\overline{C} + AB\overline{C}$
$= \overline{A}C + A\overline{C} = A \oplus C$

34. (A) The output from the upper first level multiplexer is f_a and from the lower first level multiplexer is f_b
$f_a = \overline{w}x + w\overline{x}$, $f_b = \overline{w}x + wx = x$
$f = f_a\overline{y}\overline{z} + f_b y\overline{z} + yz = (\overline{w}x + w\overline{x})\overline{y}\overline{z} + xy\overline{z} + yz$
$= \overline{w}x\overline{y}\overline{z} + w\overline{x}\overline{y}\overline{z} + xy + yz$

35. (D) Output is 1 when even parity

		BA			
		00	01	11	10
C	00	1		1	
	01		1		1

Fig. S4.2.35

Therefore $Y = \overline{A \oplus B \oplus C}$

36. (B) $I_1 = \overline{y} + z$, $I_3 = y \quad z$

		yz				
		00	01	11	10	
S_1S_0 ↕↕ wx	00	0	0	0	0	$I_0 = 0$
	01	1	1	1	0	$I_1 = \overline{y} + z$
	11	1	0	1	0	$I_3 = yz + \overline{y}\overline{z} = y \cup z$
	10	1	0	0	1	$I_2 = \overline{z}$

Fig. S 4.2.36

37. (C) Let $z = 0$, Then

$f = \overline{w}\,\overline{x}\,\overline{y} + \overline{w}\,\overline{x}y + w\overline{x}\,\overline{y} + wx\overline{y} = \overline{w}\;\overline{x} + w\;\overline{y}$

If we put $z = 0$ in given option then

(A) $= \overline{w}\,\overline{x} + x\overline{y}$ (B) $= wy + \overline{w}\;\overline{x}\;\overline{y}$ (C) $= \overline{w}\,\overline{x} + w\overline{y}$

Since MUX is enable so option (C) is correct.

38. (C) $f = x_0\overline{x}_2 + x_0\overline{x}_1\overline{x}_2 + \overline{x}_0x_2 = x_0\overline{x}_2(1 + \overline{x}_1) + \overline{x}_0x_2$

$= x_0\overline{x}_2 + \overline{x}_0x_2$

39. (B) $f_2 = \overline{x}_0x_1 + x_1x_2 + x_0\overline{x}_1\overline{x}_2$

$= \overline{x}_0x_1x_2 + \overline{x}_0x_1\overline{x}_2 + x_1x_2x_0 + x_1x_2\overline{x}_0 + x_0\overline{x}_1\overline{x}_2$

$= x_2x_1\overline{x}_0 + \overline{x}_2x_1\overline{x}_0 + \overline{x}_2\overline{x}_1x_0 + x_2x_1x_0$

$f_2(x_2,\ x_1,\ x_0) = \Sigma m(1,\ 2,\ 6,\ 7)$

40. (C) $f_3 = \overline{x}_0\overline{x}_1 + x_1x_2$

$= x_2\overline{x}_1\overline{x}_0 + \overline{x}_2\overline{x}_1\overline{x}_0 + x_2x_1x_0 + x_2x_1\overline{x}_0$

$f_3(x_2,\ x_1,\ x_0) = \Sigma m(0,\ 4,\ 6,\ 7)$

$f_3(x_2,\ x_1,\ x_0) = \Pi M(1,\ 2,\ 3,\ 5)$

41. (A)

Let $X_3X_2X_1X_0$ be 1001 then $Y_3Y_2Y_1Y_0$ will be 1111.
Let $X_3X_2X_1X_0$ be 1000 then $Y_3Y_2Y_1Y_0$ will be 1110
Let $X_3X_2X_1X_0$ be 0110 then $Y_3Y_2Y_1Y_0$ will be 1100

		bc			
		00	01	11	10
a	00			1	1
	01		1	1	

Fig. S4.2.42a

		bc			
		00	01	11	10
a	00				1
	01		1	1	1

Fig. S4.2.42b

		bc			
		00	01	11	10
a	00	1	1	1	
	01			1	

Fig. S4.2.42b

So this converts 2–4–2–1 BCD numbers.

42. (A) $f_1 = a\overline{b}c + \overline{a}b\overline{c} + bc = ac + \overline{a}b$

$f_2 = a\overline{b}c + ab + \overline{a}b\overline{c} = ac + b\,\overline{c}$

$f_3 = \overline{a}\,\overline{b}\,\overline{c} + abc + \overline{a}c = \overline{a}\overline{b} + bc$

Thus $P_1 = \overline{a}b,\ P_2 = ac,\ P_3 = b\overline{c},\ P_4 = bc,\ P_5 = \overline{a}\overline{b}$

43. (B) Let P = 1001 and Q = 1010 then

$Y_n = P_n \oplus Q_n \oplus R_n$, $Z_n = R_nQ_n + \overline{P}_nR_n + Q_n\overline{P}_n$

output is 1111 which is 2's complement of –1. So it gives $P - Q$. Let another example $P = 1101$ and $Q = 0110$ then output is 00111. It gives P–Q.

So (B) is correct.

	P_n	Q_n	R_n	Z_n	Y_n
$n = 1$	1	0	0	0	1
$n = 2$	0	1	0	1	1
$n = 3$	0	0	1	1	1
$n = 4$	1	1	1	1	1
					1

Fig. S4.2.43a

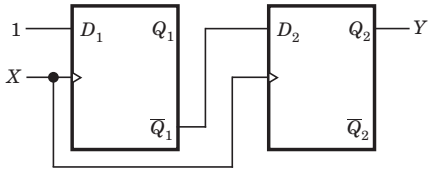
	P_n	Q_n	R_n	Z_n	Y_n
$n = 1$	1	0	0	0	1
$n = 2$	0	1	0	1	1
$n = 3$	1	1	1	1	1
$n = 4$	1	0	1	0	0
					0

Fig. S4.2.43b

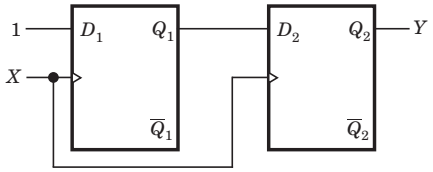
44. (D) Let input be 1010
output will be 1101
Let input be 0110
output will be 0100
This convert gray to Binary code.

****

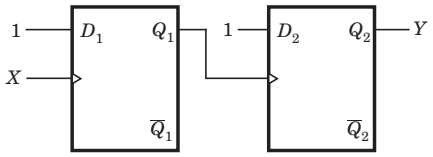
(B)



(C)



(D)



11. The circuit shown in fig. P4.3.11 is

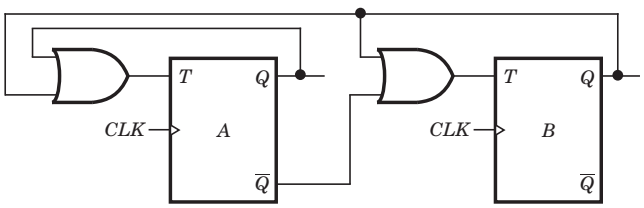


Fig.P4.3.11

(A) a MOD–2 counter

(B) a MOD–3 counter

(C) generate sequence 00, 10, 01, 00.....

(D) generate sequence 00, 10, 00, 10, 00 .....

12. The counter shown in fig. P4.3.12 is a

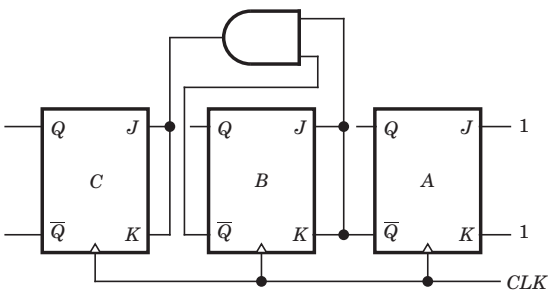


Fig.P4.3.12

(A) MOD–8 up counter

(B) MOD–8 down counter

(C) MOD–6 up counter

(D) MOD–6 down counter

13. The counter shown in fig. P4.3.13 counts from

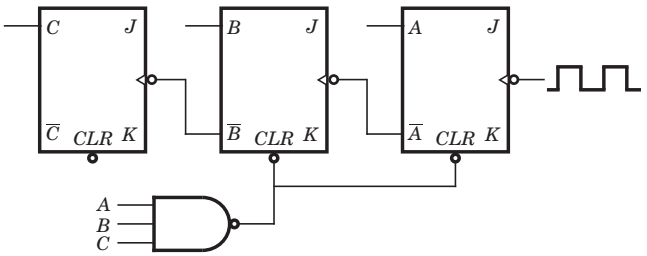


Fig.P4.3.13

(A) 0 0 0 to 1 1 1 (B) 1 1 1 to 0 0 0

(C) 1 0 0 to 0 0 0 (D) 0 0 0 to 1 0 0

14. The mod-number of the asynchronous counter shown in fig. P4.2.13 is

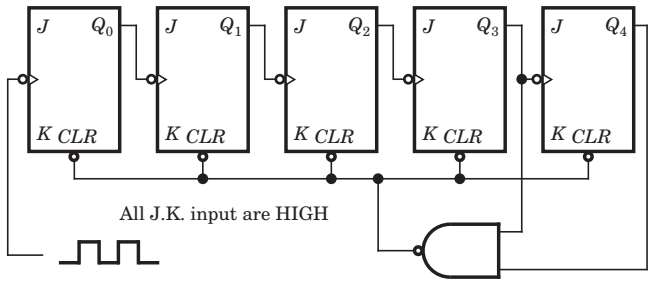


Fig.P4.3.14

(A) 24 (B) 48

(C) 25 (D) 36

15. The frequency of the pulse at z in the network shown in fig. P4.3.15. is

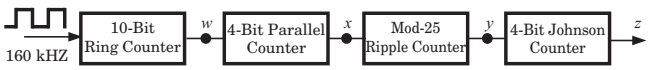


Fig.P4.3.15

(A) 10 Hz (B) 160 Hz

(C) 40 Hz (D) 5 Hz

16. The three-stage Johnson counter as shown in fig. P4.2.16 is clocked at a constant frequency of f_c from the starting state of $Q_2Q_1Q_0 = 101$. The frequency of output $Q_2Q_1Q_0$ will be

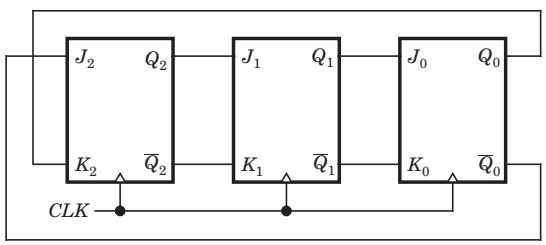


Fig.P4.3.16

(A) $\frac{f_c}{8}$ (B) $\frac{f_c}{6}$

(C) $\frac{f_c}{3}$ (D) $\frac{f_c}{2}$

17. The counter shown in the fig. P4.3.17 has initially $Q_2Q_1Q_0 = 000$. The status of $Q_2Q_1Q_0$ after the first pulse is

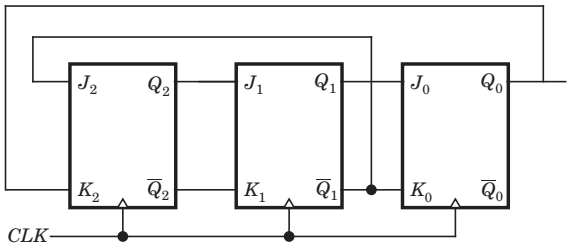


Fig.P4.3.17

(A) 0 0 1 (B) 0 1 0

(C) 1 0 0 (D) 1 0 1

18. A 4 bit ripple counter and a 4 bit synchronous counter are made by flips flops having a propagation delay of 10 ns each. If the worst case delay in the ripple counter and the synchronous counter be R and S respectively, then

(A) $R = 10$ ns, $S = 40$ ns (B) $R = 40$ ns, $S = 10$ ns

(C) $R = 10$ ns, $S = 30$ ns (D) $R = 30$ ns, $S = 10$ ns

19. A 4 bit modulo–6 ripple counter uses JK flip-flop. If the propagation delay of each FF is 50 ns, the maximum clock frequency that can be used is equal to

(A) 5 MHz (B) 10 MHz

(C) 4 MHz (D) 20 Mhz

20. The initial contents of the 4-bit serial-in-parallel-out right-shift, register shown in fig. P4.3.20 is 0 1 1 0. After three clock pulses are applied, the contents of the shift register will be

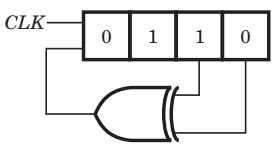


Fig.P4.3.20

(A) 0 0 0 0 (B) 0 1 0 1

(C) 1 1 1 1 (D) 1 0 1 0

21. In the circuit shown in fig. P4.3.21 is PIPO 4-bit register, which loads at the rising edge of the clock. The input lines are connected to a 4 bit bus. Its output acts as the input to a 16×4 ROM whose output is floating when the enable input E is 0. A partial table of the contents of the ROM is as follows

Address	0	2	4	6	8	10	12
Data	0011	1111	0100	1010	1011	1000	0010

The clock to the register is shown below, and the data on the bus at time t_1 is 0110.

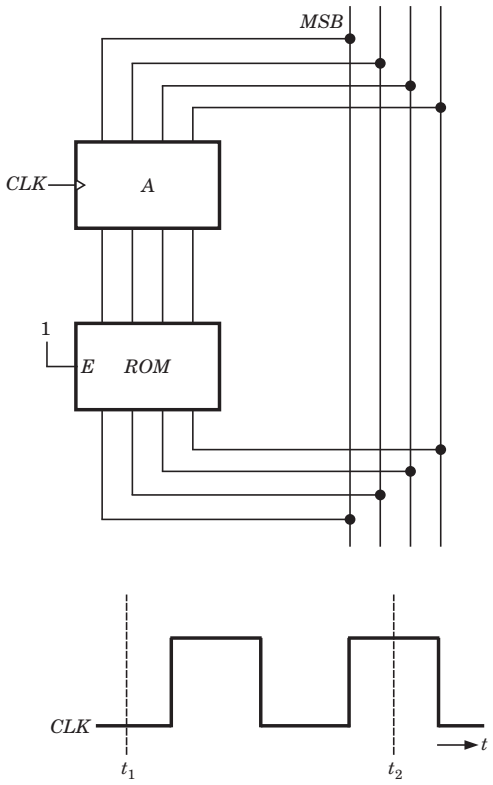


Fig. P4.3.21

The data on the bus at time t_2 is

(A) 1 1 1 1 (B) 1 0 1 1

(C) 1 0 0 0 (D) 0 0 1 0

22. A 4-bit right shift register is initialized to value 1000 for (Q_3, Q_2, Q_1, Q_0). The D input is derived from Q_0, Q_2 and Q_3 through two XOR gates as shown in fig. P4.2.22. The pattern 1000 will appear at

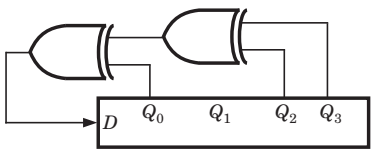


Fig.P4.3.22

(A) 3rd pulse (B) 7th pulse

(C) 6th pulse (D) 4th pulse

Statement for Q.23–24:

The 8-bit left shift register and *D*-flip-flop shown in fig. P4.3.22–23 is synchronized with same clock. The

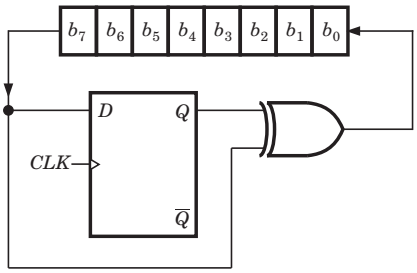


Fig.P4.3.23-24

D flip-flop is initially cleared.

23. The circuit act as

(A) Binary to 2's complement converter

(B) Binary to Gray code converter

(C) Binary to 1's complement converter

(D) Binary to Excess–3 code converter

24. If initially register contains byte B7, then after 4 clock pulse contents of register will be

(A) 73 (B) 72

(C) 7E (D) 74

Statement for Q.25–26:

A Mealy system produces a 1 output if the input has been 0 for at least two consecutive clocks followed immediately by two or more consecutive 1's.

25. The minimum state for this system is

(A) 4 (B) 5

(C) 8 (D) 9

26. The flip-flop required to implement this system are

(A) 2 (B) 3

(C) 4 (D) 5

27. The output of a Mealy system is 1 if there has been a pattern of 11000, otherwise 0. The minimum state for this system is

(A) 4 (B) 5

(C) 6 (D) 7

28. To count from 0 to 1024 the number of required flip-flop is

(A) 10 (B) 11

(C) 12 (D) 13

29. Four memory chips of 16×4 size have their address buses connected together. This system will be of size

(A) 64×4 (B) 32×8

(C) 16×16 (D) 256×1

30. The address bus width of a memory of size 1024×8 bits is

(A) 10 bits (B) 13 bits

(C) 8 bits (D) 18 bits

31. For the circuit of Fig. P4.3.31 consider the statement:

Assertion (A) : The circuit is sequential

Reason (R) : There is a loop in circuit

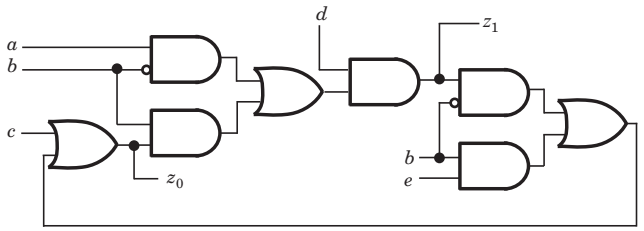


Fig.P4.3.131

Choose correct option

(A) Both A and R true and R is the correct explanation of A

(B) Both A and R true but R is not a correct explanation on of A

(C) A is true but R is false

(D) A is false

****

SOLUTIONS

1. (C) Given FF is a negative edge triggered T flip-flop. So at the negative edge of clock V_i FF will invert the output if there is 1 at input.

2. (A) At first rising edge of clock, D is HIGH. So Q will be high till 2nd rising edge of clock. At 2nd rising edge, D is low so Q will be LOW till 3rd rising edge of clock. At 3rd rising edge, D is HIGH, so Q will be HIGH till 4th rising edge. At 4th rising edge D is HIGH so Q will be HIGH till 5th rising. edge. At 5th rising edge, D is LOW, so Q will be LOW till 6th rising edge.

3. (C)

x	Q	S	R	Q^+
0	0	0	1	0
0	1	1	0	1
1	0	1	0	1
1	1	0	1	0

Fig. S4.3.3

4. (D) $Q^+ = x \oplus Q$

$Q_1^+ = x_1 \oplus Q_0 = x_1\overline{0} + \overline{x}_1 0 = x_1$

$Q_2^+ = x_2 \oplus x_1$, $Q_3^+ = x_3 \oplus x_2 \oplus x_1$

$Q_4^+ = x_4 \oplus x_3 \oplus x_2 \oplus x_1$

So this generate the even parity and check odd parity.

5. (C)

A	B	S	R	Q	Q^+
0	0	1	0	0	1
0	0	1	0	1	1
0	1	0	1	0	0
0	1	0	1	1	0
1	0	0	0	0	0
1	0	0	0	1	1
1	1	1	1	0	×
1	1	1	1	1	×

Fig. S4.3.5

$Q^+ = \overline{AB} + AQ = \overline{AB} + \overline{B}Q$

6. (D) $Q^+ = L\overline{M} + LM\overline{Q}$

$= L(\overline{M} + M\overline{Q})$

$= L\,\overline{M} + L\,\overline{Q}$

L	M	Q^+
0	0	0
0	1	0
1	0	1
1	1	$\overline{Q}_1$

Fig. S4.3.6

7. (D)

Initially	J	K	Q	$\overline{Q}$	Q_{n+1}	$\overline{Q}_{n+1}$
		1	0	1		
Clock 1st	1	1	0	1	1	0
2nd	0	1	1	0	0	1
3rd	1	1	0	1	1	0
4th	0	1	1	0	0	1
5th	1	1	0	1	1	0

Fig. S4.3.7

Therefore sequence is 010101.

8. (A)

A	B	X	Y
1	1	0	1
1	0	0	1

X and Y are fixed at 0 and 1.

9. (D) $Z = \overline{X}Q + Y\overline{Q}$

X	Y	Z
0	0	Q
0	1	0
1	0	1
1	1	$\overline{Q}_1$

Fig. S4.3.9

Comparing from the truth table of J–K FF

$Y = J$, $X = K$

10. (C)

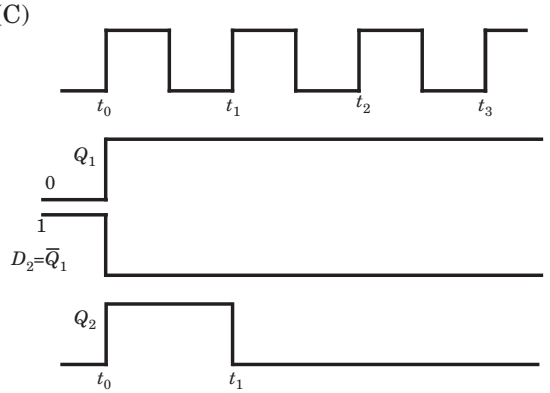


Fig.S4.3.10

11. (B)

Present State	FF Input	Next State
$Q_A\ Q_B$	$T_A\ T_B$	$Q_A^+\ Q_B^+$
0 0	0 1	0 1
0 1	1 1	1 0
1 0	1 0	0 0
1 1	1 1	0 0

Fig. S4.3.11

From table it is clear that it is a MOD–3 counter.

12. (B) It is a down counter because 0 state of previous FFs change the state of next FF. You may trace the following sequence, let initial state be 0 0 0

FF C	FF B	FF A	
$J\,K\,\overline{C}$	$J\,K\,\overline{B}$	$J\,K\,\overline{A}$	$C^+B^+A^+$
1 1 1	1 1 1	1 1 1	1 1 1
0 0 0	0 0 0	1 1 0	1 1 0
0 0 0	1 1 0	1 1 1	1 0 1
0 0 0	0 0 1	1 1 0	1 0 0
1 1 1	1 1 1	1 1 1	0 1 1
0 0 1	0 0 0	1 1 0	0 1 0
0 0 1	1 1 0	1 1 1	0 0 1
0 0 0	0 0 1	1 1 0	0 0 0

Fig. S4.3.12

13. (C) It is a down counter because the inverted FF output drive the clock inputs. The NAND gate will clear FFs A and B when the count tries to recycle to 111. This will produce as result of 100. Thus the counting sequence will be 100, 011, 010, 001, 000, 100 etc.

14. (A) It is a 5 bit ripple counter. At 11000 the output of NAND gate is LOW. This will clear all FF. So it is a Mod–24 counter. Note that when 11000 occur, the *CLR* input is activated and all FF are immediately cleared. So it is a MOD 24 counter not MOD 25.

15. (D) 10-bit ring counter is a MOD–10, so it divides the 160 kHz input by 10. therefore, $w = 16$ kHz. The four-bit parallel counter is a MOD–16. Thus, the frequency at $x = 1$ kHz. The MOD–25 ripple counter produces a frequency at $y = 40$ Hz. (1 kHz/25 = 40 Hz). The four-bit Johnson Counter is a MOD-8. This, the frequency at $z = 5$ Hz.

16. (D)

$\overline{Q}_0\,Q_0$	$Q_2\,\overline{Q}_2$	$Q_1\,\overline{Q}_1$	
$J_2\,K_2$	$J_1\,K_1$	$J_0\,K_0$	$Q_2^+\,Q_1^+\,Q_0^+$
			1 0 1
0 1	1 0	0 1	0 1 0
1 0	0 1	1 0	1 0 1
0 1	1 0	0 1	0 1 0
1 0	0 1	1 0	1 0 1

Fig. S4.3.16

We see that 1 0 1 repeat after every two cycles, hence frequency will be $f_c / 2$.

17. (C) At first cycle

$J_2K_2 = 1\,0 \quad \Rightarrow \quad Q_2 = 1,$

$J_1K_1 = 0\,0 \quad \Rightarrow \quad Q_1 = 1,$

$J_0K_0 = 0\,0 \quad \Rightarrow \quad Q_0 = 0$

18. (B) In ripple counter delay $4T_d = 40$ ns.

The synchronous counter are clocked simultaneously, then its worst delay will be equal to 10 ns.

19. (A) 4 bit uses 4 FF

Total delay $Nt_d = 4 \times 50 \text{ ns} = 200 \times 10^{-9}$

$$f = \frac{1}{200 \times 10^{-9}} = 5 \text{ Mhz}$$

20. (D) At pulse 1 input, $1 \oplus 0 = 1$

So contents are 1 0 1 1,

At pules 2 input $1 \oplus 1 = 0$'

So contents are 0 1 0 1,

At pules 3 input $0 \oplus 1 = 1$, contents are 1 0 1 0