Junction Field Effect Transistors

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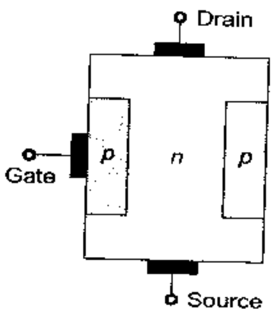
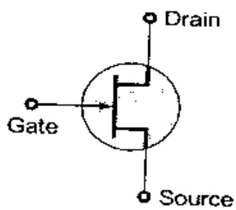
- FET is a unipolar and voltage controlled device.
- The terminals drain, gate and source of a FET are identical to collector base and emitter of a BJT.
- Since the input function is reverse biased in JFET, the current drawn is very small and so input impedance is very high.
- Less noisy device due to absence of minority carriers.
- Excellent thermal stability due to absence of leakage current.
- FET is considered as excellent signal chopper because of zero offset voltage.

Circuit Diagram and Symbol





Parameters

Drain current

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$$ In saturation region

where,
I_D = Drain current
I_{DSS} = Maximum value of current when $V_{GS} = 0$
V_p = Pinch off voltage
V_{GS} = Gate to source voltage

Drain resistance

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_{DS}}\right|_{V_{GS} = \text{constant}}$$

Note:

r_d ranges from 100 kΩ to 500 kΩ.

Transconductance

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}\text{-constant}}$$

Note:

g_m ranges from 0.1 mS to 10 mS.

In saturation region

$$g_m = -\frac{2I_{DSS}}{V_p}\left(1-\frac{V_{GS}}{V_p}\right) = -\frac{2}{V_p}\sqrt{I_D . I_{DSS}}$$

Also, $$g_m = g_{mo}\left(1-\frac{V_{GS}}{V_p}\right)$$

where, $$g_{mo} = -\frac{2I_{DSS}}{V_p}$$ = maximum value of transconductance

Amplification Factor

$$\mu = \left.\left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right)\right|_{I_D = \text{Constant}}$$

Note:

- μ ranges from 2.5 to 150.
- Relation between μ, r_d and g_m is $\mu = r_d \cdot g_m$.

Remember:

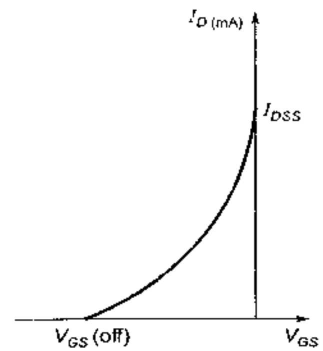
If two FETs are connected in parallel having transconductance g_{m_1} and g_{m_2}, drain resistance r_{d_1} and r_{d_2}, amplification factor μ_1 and μ_2 then

Effective transconductance $g_m = g_{m_1} + g_{m_2}$.

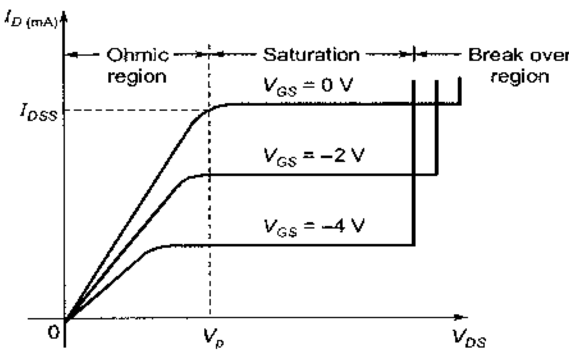
Effective drain resistance $r_d = r_{d_1} \| r_{d_2}$.

Effective amplification factor $\mu = \frac{\mu_1 r_{d_2} + \mu_2 r_{d_1}}{\mu_1 + \mu_2}$.

Characteristics of JFET



Transfer characteristic



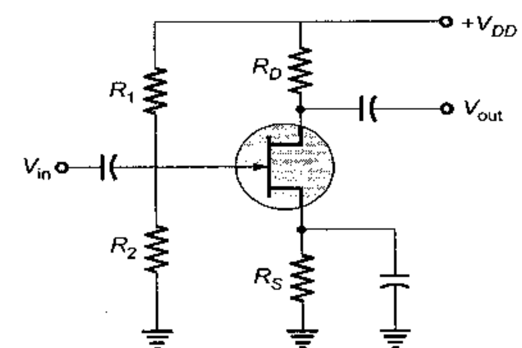
Drain characteristic

Remember:

When FET is operated below pinch-off voltage (V_p), it acts as a voltage variable resistor.

FET Amplifiers

Common Source Amplifier



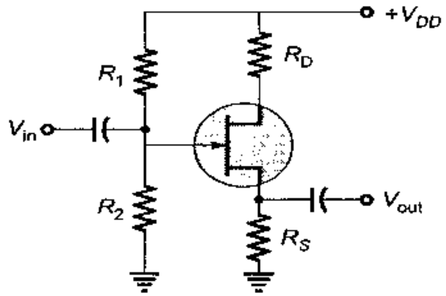
AC output voltage

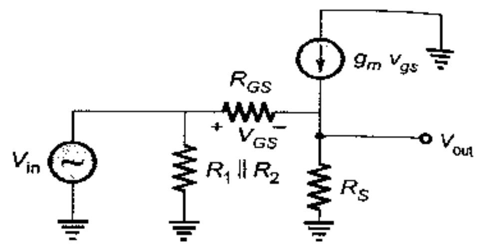
$$V_{out} = -g_m V_{GS} R_D$$

Unloaded voltage gain

$$A = -g_m R_D$$

Common Drain (CD) Amplifier





AC input voltage

$$V_{in} = (1 + g_m R_S) V_{GS}$$

AC output voltage

$$V_{out} = g_m V_{GS} R_s$$

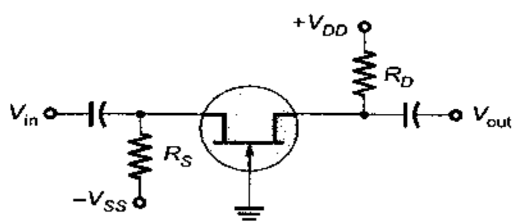
Unloaded voltage gain

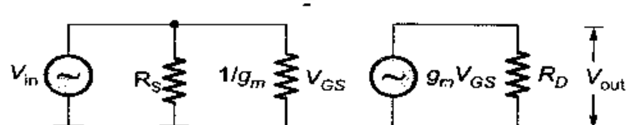
$$A = \frac{R_S}{R_S + 1/g_m} \cong 1 \quad \ldots(\text{as } R_S >> 1/g_m)$$

Output impedance

$$Z_{out(source)} = 1/g_m \quad ; \quad Z_{out} = R_S \parallel 1/g_m$$

Common Gate (CG) Amplifier





AC equivalent circuit

AC input voltage

$$V_{in} = V_{GS}$$

AC output voltage

$$V_{out} = g_m V_{GS} R_D$$

Unloaded voltage gain

$$A = g_m R_D$$

Input impedance

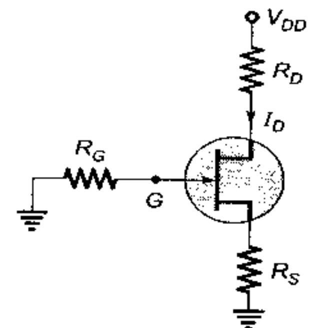
$$Z_{in} = \frac{1}{g_m}$$

DC on-state resistance

$$r_{DS(on)} = \frac{V_{DS}}{I_D}$$

where, $r_{DS(on)}$ = DC resistance in saturation region
V_{DS} = DC drain-source voltage
I_D = DC drain current

FET Biasing Circuit



Self bias circuit

Gate to source voltage

$$V_{GS} = -I_D R_s$$

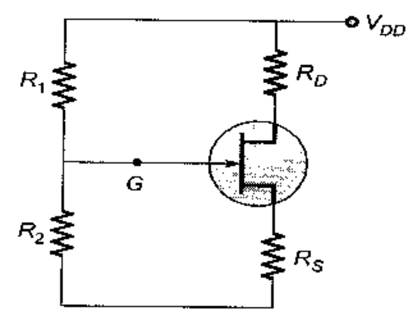
Source resistance

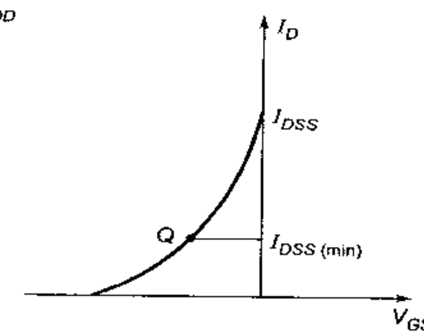
$$R_s = -V_p/I_{DSS}$$

Note: ....

Q-point is the interaction between the tranconductance and the self bias line.

Voltage divider/Source bias circuit

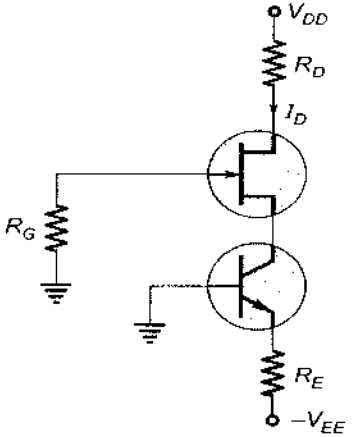


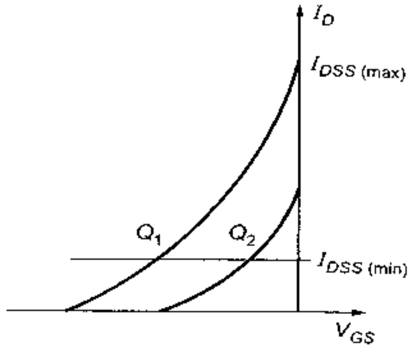


Drain current

$$I_D = \frac{V_{Th} - V_{GS}}{R_s} \qquad \text{where, } V_{Th} = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD}$$

Current source bias circuit





Collector current

$$I_C = I_D \approx \frac{V_{EE} - V_{BE}}{R_E}$$