Chapter 8

Boolean Algebra and Minimization of Functions

LEARNING OBJECTIVES

After reading this chapter, you will be able to understand:

- Logic gates
- Boolean algebra
- AXIOMS and Laws of boolean algebra
- Properties of boolean Algebra
- Boolean functions, min terms and max terms
- Minterm and maxterm

- Minimization of boolean functions
- Implementation of function by using NAND/NOR gates
- Digital IC families
- Bipolar logic families
- Unipolar logic families
- Classification of digital ICs

LOGIC GATES

Inverter or NOT Gate (7404 IC)

The inverter performs a basic logic operation called inversion or complementation. The purpose of the inverter is to change one logic level to the opposite level. In terms of digital circuits, it converts 1 to 0 and 0 to 1.
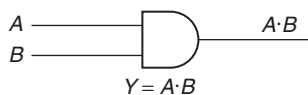

Symbol

$Y = \overline{A}$

Truth Table

Input	Output
A	Y
0	1
1	0

AND Gate (Logical Multiplier 7408 IC)

The AND gate performs logical multiplication more commonly know as AND function. The AND gate is composed of 2 or more inputs and a single output
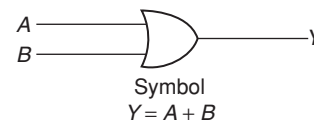

$Y = A \cdot B$

Figure 1 2 input AND gate

Truth Table

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate (Logical Adder 7432 IC)

The OR gate performs logical, addition commonly known as OR function.

Symbol

$Y = A + B$

Figure 2 2 input OR gate

Truth Table

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

NAND Gate (7400 IC)

The NAND gate's function is basically AND + NOT function.

$$Y = \overline{A \cdot B}$$
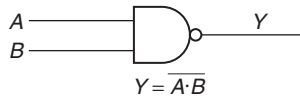
Figure 3 2 input NAND gate

Truth Table

Input		Output	
A	**B**	**A·B**	**$\overline{A+B}$ (Y)**
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

NOR Gate (7402 IC)

The NOR gate is basically OR + NOT function.

$$Y = \overline{A + B}$$
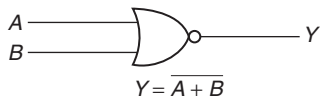
Figure 4 2 input NOR gate

Truth Table

Input		Output	
A	**B**	**A + B**	**$\overline{A+B}$ (Y)**
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Exclusive OR Gate X-OR (7486 IC)

X-OR is a gate in which unequal inputs create a high logic level output; and if both inputs are equal, the output, will be low. Other name for EX-OR gate is unequivalent gate.
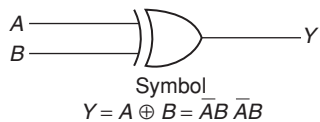

Symbol
$$Y = A \oplus B = \overline{A}B\ \overline{A}B$$

Figure 5 2 input X-OR gate

Truth Table

A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	0

7. Exclusive NOR gate (X-NOR): X-NOR is a gate in which equal inputs create a high logic level output; and

if both inputs are unequal, then the output will be low. Other name for EX-NOR gate is equivalent gate.
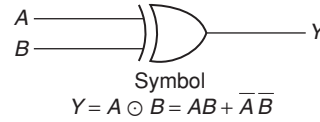

Symbol
$$Y = A \odot B = AB + \overline{A}\ \overline{B}$$

Figure 6 2 input X-NOR gate

Truth Table

A	**B**	**Y**
0	0	1
0	1	0
1	0	0
1	1	1

EX-NOR gate is complement of EX-OR gate.

BOOLEAN ALGEBRA

Boolean algebra is a system of mathematical logic. It is an algebraic system consisting of the set of elements (0, 1), two binary operators OR and AND and one unary operator NOT. The Boolean algebra is governed by certain well-developed rules and laws.

Axioms and Laws of Boolean Algebra

Axioms

1. **AND operation**
   (i) $0 \cdot 0 = 0$
   (ii) $0 \cdot 1 = 0$
   (iii) $1 \cdot 0 = 0$
   (iv) $1 \cdot 1 = 1$
2. **OR operation**
   (v) $0 + 0 = 0$
   (vi) $0 + 1 = 1$
   (vii) $1 + 0 = 1$
   (viii) $1 + 1 = 1$
3. **NOT operation**
   (ix) $\overline{1} = 0$
   (x) $\overline{0} = 1$

Laws

1. **Complementation law**
   (i) $\overline{0} = 1$
   (ii) $\overline{1} = 0$
   (iii) If $A = 0$, then $\overline{A} = 1$
   (iv) If $A = 1$, then $\overline{A} = 0$
   (v) $\overline{\overline{A}} = A$

2. **AND laws**
   (i) $A \cdot 0 = 0$ (NULL law)
   (ii) $A \cdot 1 = A$ (Identity law)
   (iii) $A \cdot A = A$
   (iv) $A \cdot \overline{A} = 0$

3. **OR laws**
   (i) $A + 0 = A$ (NULL law)
   (ii) $A + 1 = 1$ (Identity law)
   (iii) $A + A = A$
   (iv) $A + \bar{A} = 1$
4. **Commutative laws**
   (i) $A + B = B + A$
   (ii) $A \cdot B = B \cdot A$
5. **Associative laws**
   (i) $(A + B) + C = A + (B + C)$
   (ii) $(A \cdot B)C = A(B \cdot C)$
6. **Distributive laws**
   (i) $A(B + C) = AB + AC$
   (ii) $A + BC = (A + B)(A + C)$
7. **Redundant literal rule (RLR)**
   (i) $A + \bar{A}B = A + B$
   (ii) $A(\bar{A} + B) = AB$
8. **Idempotence laws**
   (i) $A \cdot A = A$
   (ii) $A + A = A$
9. **Absorption laws**
   (i) $A + A \cdot B = A$
   (ii) $A(A + B) = A$

Theorems

1. **Consensus theorem**
   Theorem 1: $AB + \bar{A}C + BC = AB + \bar{A}C$
   Proof:
   $$\begin{aligned}
   \text{LHS} &= AB + \bar{A}C + BC \\
   &= AB + \bar{A}C + BC(A + \bar{A}) \\
   &= AB + \bar{A}C + BCA + BC\bar{A} \\
   &= AB(1 + C) + \bar{A}C(1 + B) \\
   &= AB(1) + \bar{A}C(1) \\
   &= AB + \bar{A}C \\
   &= \text{RHS}
   \end{aligned}$$
   Theorem 2: $(A + B)(\bar{A} + C)(B + C) = (A + B)(\bar{A} + C)$
   Proof:
   $$\begin{aligned}
   \text{LHS} &= (A + B)(\bar{A} + C)(B + C) \\
   &= (A\bar{A} + AC + B\bar{A} + BC)(B + C) \\
   &= (AC + BC + \bar{A}B)(B + C) \\
   &= ABC + BC + \bar{A}B + AC + BC + \bar{A}BC \\
   &= AC + BC + \bar{A}B
   \end{aligned}$$
   $$\begin{aligned}
   \text{RHS} &= (A + B)(\bar{A} + C) \\
   &= A\bar{A} + AC + BC + \bar{A}B \\
   &= AC + BC + \bar{A}B \\
   &= \text{LHS}
   \end{aligned}$$

2. **Transposition theorem**
   $$AB + \bar{A}C = (A + C)(\bar{A} + B)$$
   Proof:
   $$\text{RHS} = (A + C)(\bar{A} + B)$$

$$\begin{aligned}
&= A\bar{A} + C\bar{A} + AB + CB \\
&= 0 + \bar{A}C + AB + BC \\
&= \bar{A}C + AB + BC(A + \bar{A}) \\
&= AB + ABC + \bar{A}C + \bar{A}BC \\
&= AB + \bar{A}C \\
&= \text{LHS}
\end{aligned}$$

3. **De Morgan's theorem**
   Law 1: $\overline{A + B} = \bar{A} \times \bar{B}$

   This law states that the complement of a sum of variable is equal to the product of their individual complements.
   Law 2: $\overline{AB} = \bar{A} + \bar{B}$

   This law states that the complement of the product of variables is equal to the sum of their individual complements.

Example 1: Simplify the Boolean function $Y = A(A + \bar{B})$
$$Y = A \cdot A + A \cdot \bar{B}$$
Solution: $\begin{aligned}Y &= A + A\bar{B} \\ &= A(1 + \bar{B}) \\ &= A\end{aligned}$

Example 2: Simplify the Boolean function $Y = A + \bar{A}B$
Solution: $\begin{aligned}Y &= A \cdot (B + 1) + \bar{A} \cdot B \\ &= A \cdot B + A + \bar{A}B \\ &= B(A + \bar{A}) + A \\ &= A + B\end{aligned}$

Example 3: Simplify the Boolean function
$$Y = A(A + B) + B(\bar{A} + B)$$
Solution: $\begin{aligned}Y &= A \cdot A + A \cdot B + B \cdot \bar{A} + B \cdot B \\ &= A + B(A + \bar{A}) + B \\ &= A + B \cdot 1 + B \\ &= A + B + B \\ &= A + B\end{aligned}$

Example 4: Simplify the Boolean function
$$Y = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + AB\bar{C} + A\bar{B}\bar{C}$$
Solution: $\begin{aligned}Y &= \bar{A}\bar{C}(\bar{B} + B) + A\bar{C}(B + \bar{B}) \\ &= \bar{A}\bar{C} + A\bar{C} \\ &= \bar{C}(\bar{A} + A) \\ &= \bar{C}\end{aligned}$

Example 5: Simplify the Boolean function
$$Y = \overline{\overline{\bar{A}BC + \bar{A}B\bar{C} + \bar{A}\bar{B}C}}$$
Solution: $\begin{aligned}&= \overline{\overline{\bar{A}C(B + \bar{B}) + \bar{A}B\bar{C}}} \\ &= \overline{\overline{\bar{A}C + \bar{A}B\bar{C}}} \\ &= \overline{\overline{\bar{A}(C + B\bar{C})}} \\ &= \overline{\overline{\bar{A}(C + B)}} \\ &= A + \bar{C}\bar{B}\end{aligned}$

Example 6: Simplify the Boolean function
$$Y = AB + C\bar{B} + CA + ABD$$

Solution: $Y = AB(1 + D) + C\bar{B} + CA$

$$= AB + C\bar{B} + CA$$
$$= AB + C\bar{B}$$

PROPERTIES OF BOOLEAN ALGEBRA

With n variables, maximum possible distinct functions $= 2^{2^n}$.

Duality

consider the distributive law

1. $x(y + z) = xy + xz$
2. $x + yz = (x + y)(x + z)$

The second one can be obtained from the law 1, if the binary operators and the identity elements are interchanged. This important property of Boolean algebra is called the *duality principle*.

The dual of an algebraic expression can be written by interchanging OR and AND operators, 1's by 0, and 0's by 1's.

Example 7: $x + x' = 1 \xleftarrow{\text{Dual}} x \cdot x' = 0$

Solution: $xy + xy' = x \xleftarrow{\text{Dual}} (x + y)(x + y') = x$

$x + x'y = x + y \xleftarrow{\text{Dual}} x(x' + y) = xy$

Example 8: The dual of $F = xy + xz + yz$ is?

Solution: Dual of $F = (x + y)(x + z)(y + z)$
$$= (x + xz + xy + yz)(y + z) = xy + yz + xz$$

So dual of $xy + xz + yz$ is same as the function itself, for N variables maximum possible self-dual functions $= 2^{2^{n-1}} = 2^{(2^{n/2})}$

Example 9: Which of the following statements is/are true
S_1: The dual of NAND function is NOR
S_2: The dual of X-OR function is X-NOR
(A) S_1 ND S_2 are true
(B) S_1 is true
(C) S_2 is true
(D) None of these

Solution: (A)
NAND $= (xy)' = x' + y'$
Dual of NAND $= (x + y)' = x'y'$
X-OR $= xy' + x'y$
Dual of X-OR $= (x + y')(x' + y) = xy + x'y' =$ X-NOR
Both S_1 and S_2 are true

Operator Precedence

The operator precedence for evaluating Boolean expression is

1. Parentheses
2. NOT
3. AND
4. OR

So the expression inside the parentheses must be evaluated before all the operations. The next operation to be performed is the complement and then follows AND and finally the OR.

Complement of Function

The complement of a function F is F' is obtained from an interchange of 0, s for 1, s and 1, s for 0, s in the value of F. The complements of a function may be derived algebraically through De Morgan's theorems.

$$(x_1 \cdot x_2 \cdot x_3 \ldots x_n)' = x_1' + x_2' + x_3' + \cdots + x_n'$$
$$(x_1 + x_2 + x_3 + \cdots + x_n)' = x_1' \cdot x_2' \cdot x_3' \cdot x_4' \ldots x_n'$$

Example 10: The complement of function $F = a(b'c + bc')$ is?

Solution: $(F)' = [a(b'c + bc')]'$
$$= a' + (b'c + bc')'$$
$$= a' + (b'c)' \cdot (bc')'$$
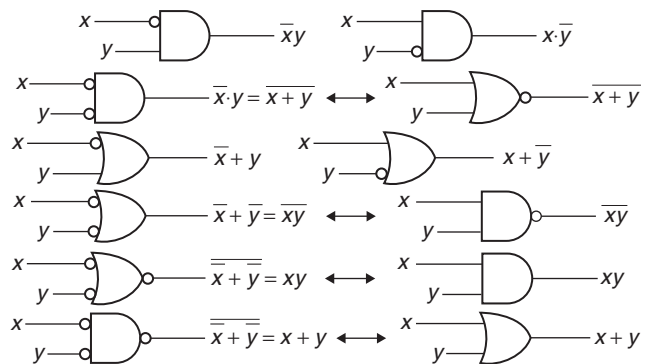$$= a' + (b + c)'(b' + c)$$
$$F' = a' + bc + b'c'$$

Figure 7 Gates with inverted inputs

BOOLEAN FUNCTIONS, MIN TERMS AND MAX TERMS

The starting point for designing most logic circuits is the truth table, which can be derived from the statement of problem. The truth table is then converted into a Boolean expression and finally the assembly of logic gates accordingly.

Let us consider the example of majority circuit. This circuit takes three inputs (A, B, C) and have one output (Y) which will give the majority of the inputs, i.e., if A, B, C are having more number of zeros. $Y = 0$ else if A, B, C are having more number of 1, s, $Y = 1$.

So from the statements we can derive the truth table as follows:
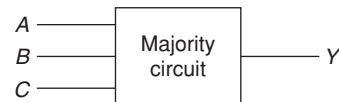
As we are using three Boolean variables A, B and C, total number of combinations in truth table are $2^3 = 8$.

Similarly for n variables, the truth table will have total of 2^n combinations, for a Boolean function.

Sl. No.	Input			Output	
	A	**B**	**C**	**Y**	
1	0	0	0	0	→ $Y = 0$, If inputs are having more zeros.
2	0	0	1	0	
3	0	1	0	0	
4	0	1	1	1	→ $Y = 1$, If inputs are having more 1's
5	1	0	0	0	
6	1	0	1	1	
7	1	1	0	1	
8	1	1	1	1	

For some combinations, output $Y = 1$, and for others $Y = 0$. The input combinations for which output $Y = 1$ are called as *min terms*.

Similarly the input combinations for which output $Y = 0$ are called as *max terms*.

Min terms are expressed as product terms. Similarly, max terms are expressed as sum terms.

The output $Y = 1$, only in rows 4, 6, 7, 8.

So the min terms combinations are 011, 101, 110, 111 in Boolean Algebra, 1 input will be written as A, B, C and 0 input will be written as $\bar{A}, \bar{B}, \bar{C}$ in complement form, we express these min terms as product terms, $\bar{A}BC, A\bar{B}C, AB\bar{C}, ABC$.

To express Y as Boolean expression, we can write it as sum of the min terms.

$$Y = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

We know that AND operation is a product while OR is sum. So the above equation is a sum of the products (SOP), (or) min terms expression.

The other way of expressing Y is $Y = \Sigma m (3, 5, 6, 7)$.

$$Y = m_3 + m_5 + m_6 + m_7.$$

The min term numbers are the decimal equivalent of input binary combinations.

Similar to SOP, we can have product of sums (POS) Boolean expression.

The output $Y = 0$ for the input combinations 000, 001, 010, 100. For max terms, one input will be indicated as $\bar{A}, \bar{B}, \bar{C}$ in complement form, 0 input will be indicated as A, B, C and max terms are expressed as sum terms.

$$A + B + C, \ A + B + \bar{C}, \ A + \bar{B} + C, \bar{A} + B + C$$

Any function can be expressed as product of max terms.

So $Y = (A + B + C)(A + B + \bar{C})(A + \bar{B} + C)(\bar{A} + B + C)$

The above equation is a product of sum expression (POS) or max terms expression.

In other way $Y = \pi M (0, 1, 2, 4)$

$$= M_0 \cdot M_1 \cdot M_2 \cdot M_4$$

The max term numbers are decimal equivalents of corresponding input binary combinations.

Min Term and Max Term

All the Boolean expressions can be expressed in a standard sum of product (SOP) form or in a standard product of sum (POS) form.

- A standard SOP form is one in which a number of product terms, each contains all the variables of the function either in complement or non-complement form are summed together.
- A standard POS form is one in which a number of sum terms, each one of which contain all the variable of the function either in complemented or non-complemented form are multiplied together.
- Each of the product term in standard SOP form is called a *min term*.
- Each of the sum term in the standard POS form is called a *max term*.

Conversion from min terms to max terms representation

$$Y = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$
$$Y' = (\bar{A}BC + A\bar{B}C + AB\bar{C} + ABC)'$$
$$= (\bar{A}BC)'(A\bar{B}C)'(AB\bar{C})'(ABC)'$$
$$(Y')' = [(A + \bar{B} + \bar{C})(\bar{A} + B + \bar{C})(\bar{A} + \bar{B} + C)(\bar{A} + \bar{B} + \bar{C})]'$$
$$= [\pi(3, 5, 6, 7)]' = \pi(0, 1, 2, 4)$$
$$Y = (A + B + C)(A + B + \bar{C})(A + \bar{B} + C)(\bar{A} + B + C)$$
or $Y = \Sigma(3, 5, 6, 7) = \pi(0, 1, 2, 4)$

Conversion from normal SOP/POS form to canonical SOP/POS

Let us consider $f(A, B, C) = A + BC + \bar{A}C$

The above function is in normal (minimized) SOP form, to convert this function to standard SOP or canonical SOP form, include missing variable in each and every term, to make it complete. First term A, missing literals are B, C. Consider $A \ X \ X$, so possible combinations are $\bar{A}BC, A\bar{B}C, AB\bar{C}, ABC$ or we can write

$$A = A(B + \bar{B})(C + \bar{C}) = ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C}$$

Second term BC = missing literal is A. Consider $XBC \Rightarrow$ so possible combinations are $ABC, \bar{A}BC$ or we can write

$$BC = (A + \bar{A})BC$$
$$= ABC + \bar{A}BC$$

Third term $\bar{A}C$ = missing literal is B. Consider $\bar{A}XC \rightarrow$ so possible combinations are $\bar{A}BC, \bar{A}, \bar{B}C$ or we can write

$$\bar{A}C = \bar{A}(B + \bar{B})C$$
$$= \bar{A}BC + \bar{A}\bar{B}C$$

Now, $f(A, B, C) = ABC + AB\overline{C} + A\overline{B}C + \overline{A}BC + \overline{A}\overline{B}C$, after removing the redundant terms.

Now consider

$$f(A, B, C) = (A + B)(\overline{A} + C)$$

To convert this expression to canonical form or standard POS form we can write

$$f(A, B, C) = (A + B + C \cdot \overline{C})(\overline{A} + B \cdot \overline{B} + C)$$

Here, the C variables is absent from first term and B from second term. So add $C \cdot \overline{C}$ (= 0) to first, and $B \cdot \overline{B}$ to second, and using distributive law arrive at the result.

$$f(A, B, C) = (A + B + C)(A + B + \overline{C})(\overline{A} + B + C)(\overline{A} + \overline{B} + C)$$

MINIMIZATION OF BOOLEAN FUNCTIONS

Simplification Procedure

- Obtain truth table, and write output in canonical form or standard form
- Generate K-map!
- Determine prime implicants
- Find minimal set of prime implicants.

Karnaugh Map (K-map) Method

Karnaugh map method is a systematic method of simplifying the Boolean expression. K-map is a chart or a graph composed of an arrangement of adjacent cell, each representing a particular combination of variable in sum or product form. (i.e., min term or max term).

Two-variable K-map

x	y	F
0	0	m_0
0	1	m_1
1	0	m_2
1	1	m_3

m_0	m_1
m_2	m_3

x \ y	0	1
0	$x'y'$	$x'y$
1	xy'	xy

Three-variable K-map

A three-variable map will have eight min terms (for three variables $2^3 = 8$) represented by 8 squares

x	y	z	F
0	0	0	m_0
0	0	1	m_1
0	1	0	m_2
0	1	1	m_3
1	0	0	m_4
1	0	1	m_5
1	1	0	m_6
1	1	1	m_7

m_0	m_1	m_3	m_2
m_4	m_5	m_7	m_6

x \ yz	00	01	11	10
0	$x'y'z$	$x'y'z$	$x'yz$	x''
1	$xy'z'$	$xy'z$	xyz	xyz'

3-variable K-map

Four-variable K-maps

The K-map for four variables is shown here, 16 min terms are assigned to 16 squares.

wx \ yz	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

The map is considered to lie on a surface with the top and bottom edges as well as the right and left edge touching each other to form adjacent squares.

- One square → a min term of four literals
- Two adjacent square → a term of three literals
- Four adjacent square → a term of two literals
- Eight adjacent square → a term of one literal
- Sixteen adjacent square → the constant one

Don't-care Combinations

It can often occurs that for certain input combinations, the value of the output is unspecified either because the input combination are invalid or because the precise value of the output is of no consequence. The combination for which the values of the expression are not specified are called don't-care combinations. During the process of design using an SOP, K-map, each don't-care is treated as a 1 if it is helpful in map reduction, otherwise it is treated as a 0 and left alone.

During the process of design using a POS K-map, each Don't-care is treated as a 0 if it is useful in map reduction, otherwise it is treated as a 1 and left alone.

Example 11: Find the minimal expression $\Sigma m (1, 5, 6, 12, 13, 14) + d(2, 4)$

Solution:

AB \ CD	00	01	11	10
00		1		×
01	×	1		1
11	1	1		1
10				

$$\therefore \quad F = B\overline{C} + B\overline{D} + \overline{A}\overline{C}D$$

Pairs, Quads and Octets

A \ BC	00	01	11	10
0		1	1	
1				

The map contains a pair of 1, s those are horizontally adjacent. Those cells represent $\overline{A}\overline{B}C$, $\overline{A}BC$.

For these two min terms, there is change in the form of variable B. By combining these two cells we can form a pair, which is equal to $\overline{A}\overline{B}C + \overline{A}BC = \overline{A}C(\overline{B} + B) = \overline{A}C$.

If more than one pair exists on K-map, OR the simplified products to get the Boolean function.

$$F = \overline{A}\overline{C} + AC$$

$$F = \overline{A}C\overline{D} + \overline{A}\overline{B}D + \overline{A}B\overline{C} + AC\overline{D}$$

So pair eliminates one variable by minimization.

Quad

Quad is a group of four 1, s those are horizontally or vertically adjacent.

$$F = C \qquad F = \overline{A}C + AC = (\overline{A} + A)C = C$$

By considering two pairs, also it will be simplified to C.
Quad eliminates two variables from the function

$$F = B\overline{D} + \overline{B}D$$

Corner min terms can from a quad:

$$F = \overline{Q}\overline{S}$$

Octet

The group of eight cells will form one octet.

$$F = Y$$

Other variable X, Z, W changes their form in octet. Octet can eliminate three variables and their complements.

$$F = \overline{D}$$

Other variable A, B, C are vanished.

Eliminating Redundant Groups

$$AB + \overline{A}C + BC$$

$$AB + \overline{A}C$$

Here BC is redundant pair, which covers already covered min terms of $AB, \overline{A}C$.

This K-map gives fourpairs and one quad.

But only four pairs are enough to cover all the min times, quad is not necessary.

$$\overline{P}\,\overline{R}S + \overline{P}QR + PQ\overline{R} + PRS \text{ is minimized function.}$$

Prime Implicant

The group of adjacent min terms is called a prime implicant, i.e., all possible pairs, quads, octets, etc.

Prime implicants are $\overline{B}\overline{C}$, $B\overline{C}$, $\overline{C}$, $\overline{A}\overline{B}$. Minimized function is $\overline{C} + \overline{A}\overline{B}$.

Essential Prime Implicant

The prime implicant which contains at least one min term which cannot be covered by any other prime implicant is called essential prime implicant.

Min term 0, 6 can be grouped with only one pair each. The total possible prime implicants are $\overline{A}\overline{B}$, $\overline{B}C$, AC, AB but min term 0, 6 can be covered with $\overline{A}\overline{B}$, AB. So we call them as essential prime implicants. Min term 5 can be paired with any of 1 or 7 min term.

The essential prime implicants are $XZ\overline{W}$, $\overline{X}\overline{Y}\overline{Z}$

Redundant Prime Implicant

The prime implicant whose min terms are already covered by at least one min term is called redundant prime implicants.

Here prime implicants are $\overline{A}\overline{B}$, AC, $\overline{B}C$. But $\overline{B}C$ is already covered by other min terms. So $\overline{B}C$ is redundant prime implicant.

Example 12: Find the minimal expression for $\Sigma m(1, 2, 4, 6, 7)$ and implement it using Basic gates.

Solution: K-map is

$$F = A\overline{C} + AB + B\overline{C} + \overline{B}C + \overline{A}\overline{B}C$$
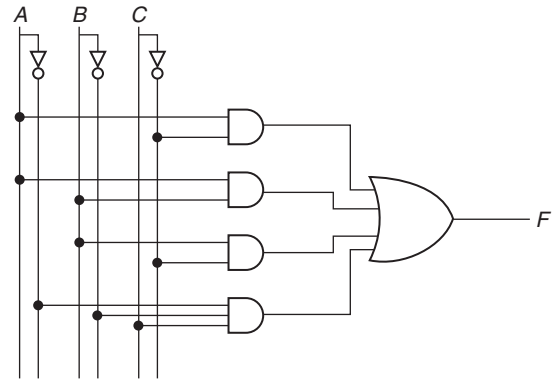
Figure 8 Logic diagram

Example 13: Find the minimal expression for Σm (2, 3, 6, 7, 8, 10, 11, 13, 14)

Solution: K-map is:

$\therefore \quad F(A, B, C, D) = AB\overline{C}D + A\overline{B}\overline{D} + \overline{A}C + \overline{B}C + C\overline{D}$

Example 14: Three Boolean functions are defined as below $f_1 = \Sigma m(0, 1, 3, 5, 6)$, $f_2 = \Sigma m(4, 6, 7)$ $f_3 = \Sigma m(1, 4, 5, 7)$, then find f.
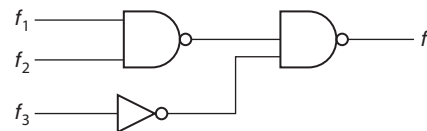
Solution: When two Boolean functions are ANDed, the resultant will contain the common min terms of both of the functions (e.g., intersection of min terms). If two Boolean functions are ORed, then resultant is the combination of all the min terms of the functions (like union of min terms)

Here $f = \overline{\overline{f_1 f_2} \cdot \overline{f_3}} = f_1 f_2 + f_3$

Here $f_1 \cdot f_2 =$ Common min terms in f_1 and $f_2 = \Sigma m(6)$
$f_1 \cdot f_2 + f_3 =$ Combination of min terms of $f_1 \cdot f_2$ and f_3
$= \Sigma(1, 4, 5, 6, 7)$

Example 15: What is the literal count for the minimized SOP, and minimized POS form for the following function? $f(A, B, C, D) = \Sigma m(0, 1, 2, 5, 12) + \phi d(7, 8, 10, 13, 15)$

Solution: $f(A, B, C, D) = \Sigma m(0, 1, 2, 5, 12) + \phi(7, 8, 10, 13, 15)$

f = 1 quad + 2 pairs
Literal count = $1 \times 2 + 2 \times 3 = 8$
$f(A, B, C, D) = \pi M(3, 4, 6, 9, 11, 14) + \phi(7, 8, 10, 13, 15)$

f will consists of three quads + one pair = $3 \times 2 + 1 \times 3 = 6$
$+ 3 = 9$

IMPLEMENTATION OF FUNCTION BY USING NAND–NOR GATES

NAND or NOR gates are called as universal gates, because any function can be implemented by using only NAND gates or only using NOR gates.
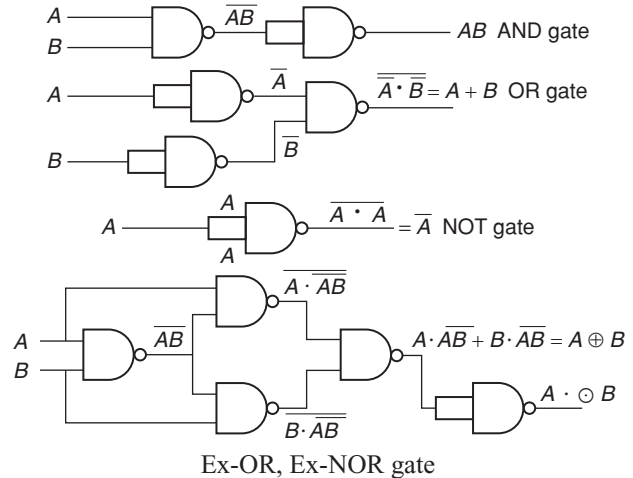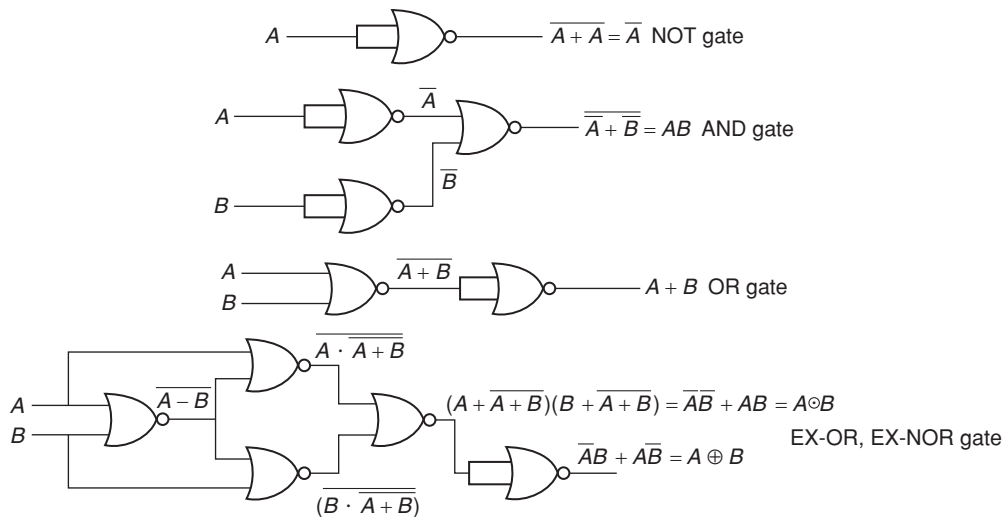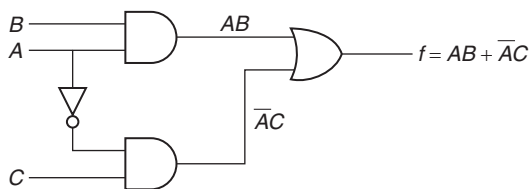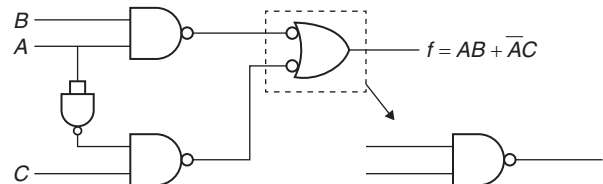

Figure 9 Implement of basics gates by using NAND gates

Figure 10 Implementation of basic gates by using NOR gates

Any function which is in the SOP form can be implemented by using AND-OR gates, which is also equivalent to NAND–NAND gates.

$$F = AB + \overline{A}C$$

By considering bubble at AND gate output and OR gate input, and by changing NOT gates to NAND gates, the circuit becomes as,

Now the circuit is in completely in NAND–NAND form

So the functions expressed in SOP form can be implemented by using AND–OR, (or) NAND–NAND gates.

Any function in POS from can be implemented by using OR–AND gates, which is similar to NOR–NOR gate.

Example 16: How many number of NAND gates are required to implement $f(A, B, C) = AB + BC + AC$
(A) 3   (B) 4   (C) 5   (D) 6

Solution:

By considering bubbles at output of AND gate and input of OR gate.

So four NAND gates are required.

Example 17: Number of NAND gates required for implementation of $f(A, B) = A + \overline{B}C$ is
(A) 3   (B) 4   (C) 5   (D) 6

Solution:

To convert the all gates into NAND gates, place bubble output of AND, and inputs of OR gates. Now, the circuit can be drawn as

Four NAND gates are required.

Example 18: $f = A + BC$, the number of NOR gates required to implement f, are?
(A) 3   (B) 4   (C) 5   (D) 2

Solution: $A + BC$ is in SOP form.
To implement this function by using NOR gates, we can write $f(A, B, C) = A + BC = (A + B)(A + C)$
Which is in the form of POS?

By including bubbles at output of OR gate, and input of AND gate, the circuit becomes

Now the circuit consists of all NOR gates. So three NOR Gates are required.

Example 19: How many number of two-input NAND–NOR gates are required to implement three-input NAND–NOR gates respectively?
(A) 2, 2   (B) 2, 3
(C) 3, 2   (D) 3, 3

Solution: $f(A, B, C) = \overline{ABC} = \overline{AB} + \overline{C}$

(1) Implement above function by using two-inputs gates:

Now convert each gate to NAND gate:

Three two-input NAND gates are required.

(2) $G(A, B, C) = \overline{A + B + C}$ – Implement it by using two-input gates

Now convert each gate to NOR gate:

Three two-input, NOR gates are required.

EX-OR, EX-NOR GATES

Inverted inputs for EX-OR, EX-NOR gates

$$\overline{A} \oplus B = \overline{\overline{A}B} + \overline{A}\,\overline{B} = AB + \overline{A}\,\overline{B} = A \odot B$$

$$A \oplus \overline{B} = \overline{A}\,\overline{B} + \overline{A}\,\overline{B} = AB + \overline{A}\,\overline{B} = A \odot B$$

$$\overline{A} \oplus \overline{B} = \overline{\overline{A}}\,\overline{B} + \overline{\overline{A}\,\overline{B}} = \overline{A}B + A\overline{B} = A \oplus B$$

$$\overline{A} \odot B = \overline{\overline{A}B} + \overline{\overline{A}}\,\overline{B} = \overline{A}B + A\overline{B} = A \oplus B$$

$$A \odot \overline{B} = A\overline{\overline{B}} + \overline{A}\overline{B} = AB + \overline{A}\overline{B} = A \oplus B$$

$$\overline{A} \odot \overline{B} = \overline{A}\overline{B} + \overline{\overline{A}}\overline{\overline{B}} = \overline{A}B + AB = A \odot B$$

From the above discussions, we can conclude that inverted input EX-OR gate is EX-NOR gate.

Similarly inverted input EX-NOR gate is EX-OR gate. If both inputs are inverted, the EX-OR/EX-NOR will remain as it is.

Consider a three-inputs X-OR gates by using two-input X-OR gates.
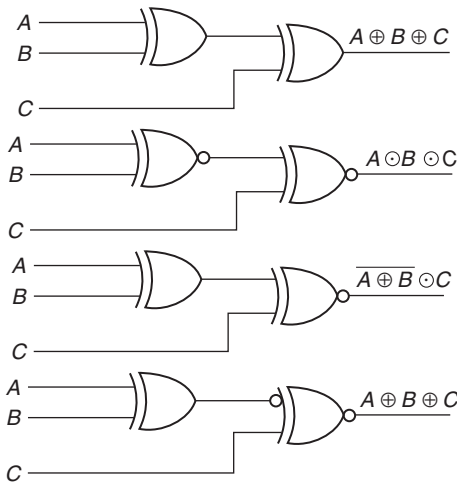
So we can conclude that $A \oplus B \oplus C = A \odot B \odot C$
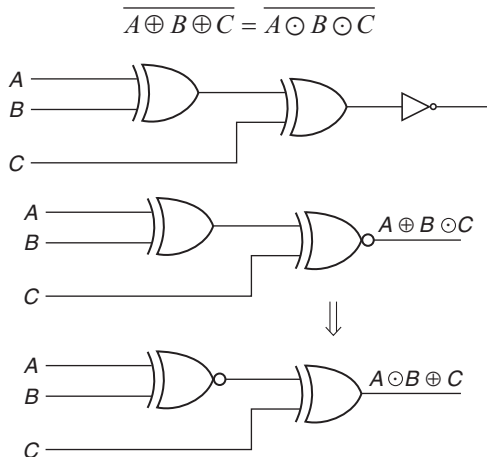
$$\overline{A \oplus B \oplus C} = \overline{A \odot B \odot C}$$

$$\overline{A \oplus B \oplus C} = \overline{A \odot B \odot C} = A \oplus B \odot C$$
$$= A \odot B \oplus C$$
$$A \oplus B \oplus C \oplus D = A \oplus B \odot C \odot D = A \odot B \odot C \oplus D = A \odot B \oplus C \odot D$$
$$A \odot B \odot C \odot D = \overline{A \oplus B \oplus C \oplus D}$$
$$A \odot B \odot C \odot D = A \oplus B \oplus C \odot D = A \oplus B \odot C \oplus D$$

Example 20: For the logic circuit shown in figure, the required input condition (A, B, C) to make the output $X = 0$ is?
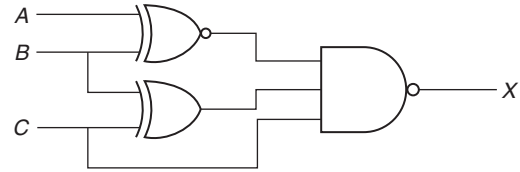
(A) 1, 1, 1   (B) 1, 0, 1
(C) 0, 1, 1   (D) 0, 0, 1

Solution: (D)
To get output $X = 0$, all inputs to the NAND gate should be 1, so $C = 1$. When $C = 1$, the output of X-OR gate $B \oplus C$ $= 1$ only when $B = 0$. If $B = 0$, the output of X-NOR gate $A \odot B = 1$.
Only when $A = 0$.
So $X = 1$, only when $(A, B, C) = (0, 0, 1)$.

Example 21: The minimized expression of

$$(A + \overline{B})(A\overline{B} + AC)(\overline{AC} + \overline{B}) \text{ is}$$

Solution: $(A + \overline{B})(A\overline{B} + AC)(\overline{AC} + \overline{B})$

$$= (A + \overline{B})(A\overline{B} \cdot \overline{AC} + A\overline{B} \cdot \overline{B} + AC \cdot \overline{AC} + AC \cdot \overline{B})$$
$$= (A + \overline{B})(A\overline{B} + A\overline{B}C) = (A + \overline{B})A\overline{B}(1 + C)$$
$$= A\overline{B} + A\overline{B} = A\overline{B}$$

Example 22: The Boolean function f is independent of
(A) a   (B) b
(C) c   (D) None of these

Solution: (A)
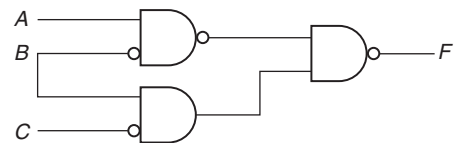
$F = \overline{\overline{ab} \cdot \overline{bc}}$

$= ab + \overline{\overline{bc}} = ab + b + \overline{c}$

$= b + \overline{c}$ is independent of 'a'.

Example 23:
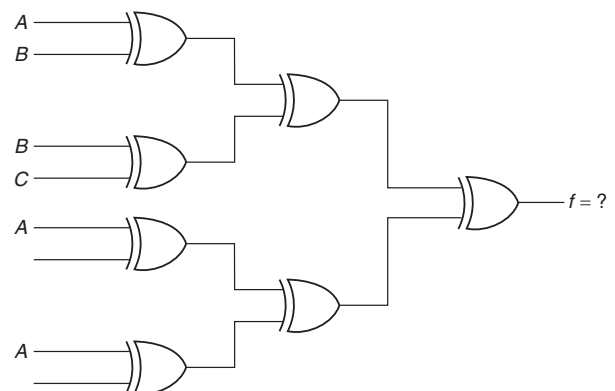
Solution: $f = \{A \oplus B \oplus B \oplus C\} \oplus \{A \oplus C \oplus B \oplus A\}$

$= \{A \oplus 0 \oplus C\} \oplus \{0 \oplus C \oplus B\}$

$= A \oplus C \oplus C \oplus B = A \oplus 0 \oplus B = A \oplus B$

DIGITAL IC FAMILIES

Digital logic gates will be implemented by using digital ICs. Logic family is the way to describe the internal circuitry of the IC. Each logic family is characterized by a circuit configuration, semiconductor technology and set of desirable properties.

Bipolar Logic Families

There are two types of operations in bipolar logic families:

1. Saturated
2. Non-saturated

In saturated logic, the transistors in the IC are driven to saturation whereas in the case of non-saturated logic, the transistors are not driven into saturation.

The saturated logic families are

- Diode transistor logic (DTL) transistor–transistor logic (TTL), etc.
- The non-saturated logic families are schottky TTL, emitter coupled logic (ECL), etc.

Unipolar Logic Families

MOS devices are unipolar devices and only MOSFETS are employed in MOS logic circuits,

MOS logic families are PMOS, NMOS, CMOS, etc.

Table 1 *Classification of digital ICs*

IC classification	Equivalent individual gates per chip	Number of components
Small-scale integration (SSI)	Less than 12	Up to 99
Medium-scale integration (MSI)	12–99	100–999
Large-scale integration (LSI)	100–99	1000–9,.999
Very large-scale integration VLSI)	Above 1000	Above 10,000
Ultra large-scale integration (ULSI)	—	10^6–10^7
Giant-scale integration (GSI)	—	Above 10^7

Characteristics of Digital ICs

Speed of Operations The speed of digital circuits is specified in terms of propagation delay time:
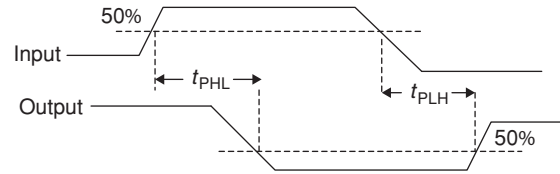
Input and output wave form to define propagation delay times

The propagation delay time of logic gates is taken as average of these two delay times.

Power Dissipation It is determined by the current I_{CC} that is drawn from V_{CC} supply and is given as $V_{CC} \times I_{CC}$. I_{CC} is the average of $I_{CC}(0)$ and $I_{CC}(1)$. It is known as static power dissipation as it is power consumed by current when input signals are not changing.

Figure of Merit It is a product of speed and power.

Figure of merit = propagation delay (ns) × power (mW)

Fan out It is the number of similar gates which can be driven by a gate, where high fan out is advantageous.

Current and Voltage Parameters

High-level input voltage V_{IH}: minimum input voltage which is recognized by the gate as logic 1.

Low-level input voltage V_{IL}: maximum input voltage which is recognized by gate as logic 0.

High-level output voltage V_{OH}: minimum voltage available at the output corresponding to logic 1.

Low-level output voltage V_{OL}: maximum voltage available at the output corresponding to logic 0.

High-level input current I_{IH}: Minimum current which must be supplied by a driving source corresponding to logic 1 level voltage.

Low-level input current I_{IL}: minimum current which must be supplied by a driving source corresponding to logic 0 level voltage.

High-level output current I_{OH}: maximum current which the gate can sink in 1 level.

Low-level output current I_{OL}: This is the maximum current which the gate can sink in 0 level.
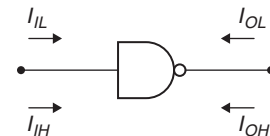
A gate with current directions marked:

$I_{CC}(1)$:   High-level supply current when output is at logic 1.

$I_{CC}(0)$:   Low-level supply current, when output of gate is at logic 0.

Noise immunity

Stray electric and magnetic fields may induce unwanted voltage, known as noise, on connecting wires between logic circuits.
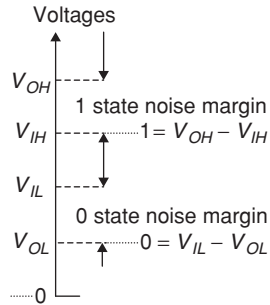
This may cause the voltage at the input to a logic circuit to drop below V_{IH} or rise above V_{IL} and may produce undesired operation.

The circuit's ability to tolerate noise signals is referred to as noise immunity, a quantitative measure of which is called noise margin.

Note:

Noise margin: High-state noise margin $V_{NH} = V_{OH(min)} - V_{IH(min)}$

Low-state noise margin $V_{NL} = V_{IL(max)} - V_{OL(max)}$
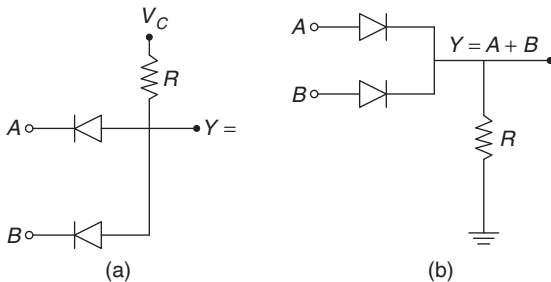
$\therefore$ Overall noise margin $NM = \min \{V_{NH} \cdot V_{NL}\}$

HTL logic family has highest noise margin among all logic families.

Fan out: Fan out (High) $= F_{OH} = \dfrac{I_{OH(max)}}{I_{IH(max)}}$

Fan out (Low) $= F_{OL} = \dfrac{I_{OL(max)}}{I_{IL(max)}}$

$\therefore$ Overall fan out $= \min \{F_{OH}, F_{OL}\}$

CMOS logic family has highest fan out among all families.

Figure 11 Basic gate and it diode circuit diagram (a) AND gate, (b) OR gate

Direct coupled transistor logic (DCTL)

In the RTL logic family, if the base resistor is disconnected, we obtain DCTL.
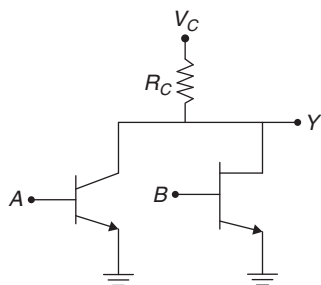
It is suffering from current hogging problem.

- The noise margin of the DCTL is very poor.
- The basic gate is a NOR gate.

Integrated ilogic Integrated Injection logic (I^2L) is the modified version of DCTL. In direct coupled transistor logic (DCTL) suffers from the current hogging problem. It is also called merged-transistor logic (MTL).

In I^2L logic family, PNP and NPN transistors are integrated; so, it uses very small silicon chip area.
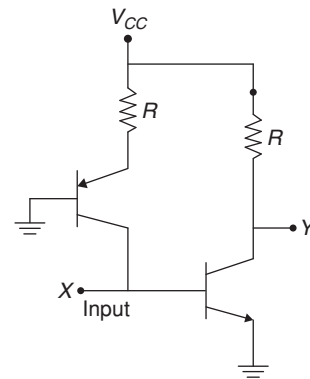
- I^2L available with multi-collector output. So its fan out is higher than RTL logic family.
- The speed of operation of I^2L depends upon the charging current and the propagation delay time is inversely proportional to the charging current.
- Figure of merit in the range of 0.1 to 0.7 pJ.
- I^2L has the highest figure of merit among all logic families.

Diode transistor logic (DTL)
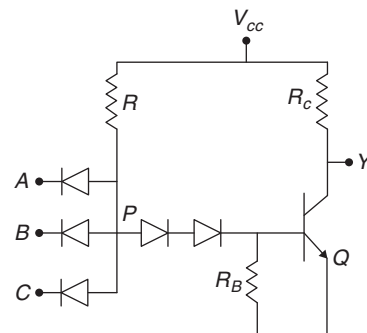
If any of the input is low, the input diode will be forward biased and the voltage at P drives transistor Q to cut off, so output Y is V_{CC}. If all the inputs are HIGH, then none of the input diode will be forward biased and voltage V_{CC} through 'R' and P will drive transistor Q into saturation and output Y will be V_{CE}, sat, which is (logic 0).

If we consider voltage corresponding to logic 1 and 0 as V_{CC} and V_{CE}, respectively, this circuit performs NAND operation.

The propagation delay time of commercially available DTL gates are of the order of 30 to 80 ns.

If outputs of gates are connected together, additional logic is preformed without additional hardware. This type of connection is referred to as wired logic (or) wired AND,

$$Y = Y_1 Y_2 = \overline{AB} \cdot \overline{CD} = \overline{AB + CD}$$
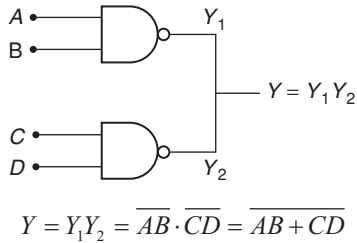
Transistor–transistor logic (TTL)

It is the most successful bipolar logic. TTL logic families use transistors, both to perform logic functions and to provide high-output drive capability.

The NAND gate is the basic TTL logic circuit. It uses multiple-emitter transistor Q_1.

The number of inputs (fan in) to the gate is same as the number of emitters fabricated during its manufacturing.
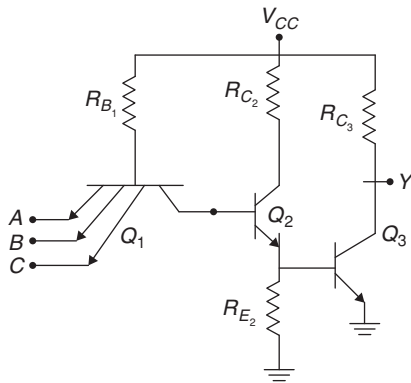
Figure 12 3-Input TTL NAND gate

If at least one input is low, the corresponding emitter base junction is forward biased, so the base voltage of Q_1 will not able to make base collector junction of Q_1 to forward bias, and for Q_2 and Q_3 to be conductions hence Q_2 and Q_3 are OFF and $Y = V_{CC} = V(1)$.

If all inputs are HIGH, the emitter base junctions of Q_1 are reverse biased. If we assume that Q_2 and Q_3 are ON, therefore $Y = V(0) = 0.2$ V.

The fan out (N) of a gate depends upon the maximum collector current rating of the transistor Q_3. The total collector current $I_{C_3} = I_{C_3, \text{sat}} = N \cdot I_L$, when the output is in the low state.

If the output of gates are connected together, wired AND logic is performed.

The output voltage is pulled up by the time constant $T = R_{C_3} \cdot C_0$ resistance R_{C_3} is known as pull-up resistor.

It is possible in TTL gates to hasten the charging of output capacitance without corresponding increase in power dissipation with the help of an output circuit arrangement referred to as on active pull up or totem pole output.

Wired–AND connection must not be used for totem–pole output circuits because of the current spike problem.

Open collector output: A circuit with open collector output is the same as the circuit except for the collector – resistor R_{C_3} of Q_3 which is missing. The collector terminal is available outside the IC, and the passive pull up is to be connected externally.

If any input of a TTL gate is left disconnected, (open or floating), the corresponding $E – B$ junction of Q_1 will not be forward biased. Hence it acts exactly in the same way as if a logic 1 is applied to that input. Therefore, in TTL ICs, all unconnected inputs are treated as logic 1's.

Schottky TTL

The speed limitation of TTL is mainly due to the turn-off time delays involved in transistors while making transistors from saturation to cut off. This can be eliminated by replacing the transistors of TTL gate by Schottky transistors.

Emitter-coupled logic (ECL)
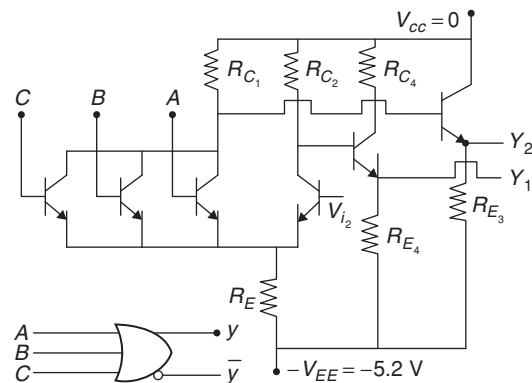
Figure 13 3-input ECL OR / NOR gate

ECL is the fastest of all logic families, and therefore is used in applications where very high speed is essential. High speeds have become possible in ECL because the transistors are used in different amplifier configurations, in which they are never driven into saturation and thereby the storage time is eliminated. Propagation delays of less than 1 ns per gate have become possible in ECL.

ECL is realized using difference amplifier in which the emitters if the two transistors are connected and hence it is referred to as emitter coupled logic. Two outputs, Y_1 and

Y_2 which are complementary are available at ECL output, Y_1 corresponds to OR output, and Y_2 corresponds to NOR output.

In ECL, the positive end of the supply is connected to ground in contrast to other logic families. Because of the low output impedance and high input impedance, the fan out of ECL is large.

Wired OR logic: The outputs of two or more ECL gates can be connected to obtain wired OR logic without using additional hardware.
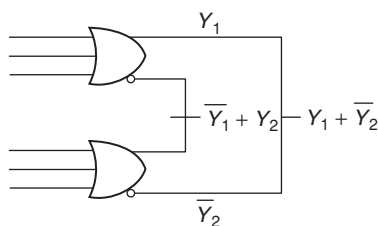

Figure 14 Wired–OR connection of ECL

If any input of an ECL gate is left unconnected, the corresponding E–B junction of input transistor will not be conducting, hence it acts as if a logic 0 level voltage is applied to that input.

MOS logic MOSFETS have become very popular for logic circuits due to high density of fabrication and low power dissipation. When MOS devices are used in logic circuits, there can be circuits in which either only p-channel (PMOS) or n-channel (NMOS) devices are used.

It is also possible to fabricate enhancement mode P-channel and n-channel MOS devices (CMOS) on the same chip.

The power dissipation is extremely small for CMOS and hence CMOS logic has became very popular.
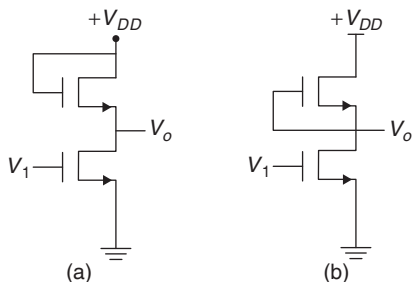
Figure 15 The basic MOS gate is an inverter

A MOS inverter with

(a) Enhancement load
(b) Depletion load

The logic levels of MOS Circuits are

$$V(0) = 0$$
$$V(1) = V_{DD}$$

MOSFET NAND and NOR gates
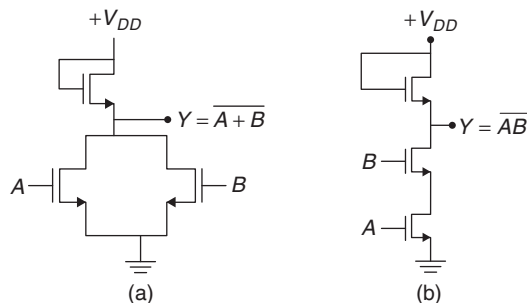
Figure 16 (a) 2-input NMOS NOR gate, (b) 2-Input NMOS NAND gate

NOR gates can be obtained by using multiple drives in parallel, whereas for NAND gates the drives are to be connected in series.

If the input is 0, the corresponding transistor is OFF, else it will be in ON state.

Since MOS devices have very high input impedance, therefore the fan out is large, but driving a large number of MOS gates increases the capacitance at the output of the driving gate, which in turn reduces the speed of MOS gates.

The propagation delay of MOS devices is large because of large capacitance present at the input and output of these devices.

MOS devices have very high input impedance and even a small static charge flowing into this high impedance can develop a dangerously high voltage. Therefore MOS ICs inputs must not be left unconnected.

CMOS logic A complementary MOSFET (CMOS) is obtained by connecting a p- and n-channel MOSFET in series, with drains tied together and the output is taken at the common drain.
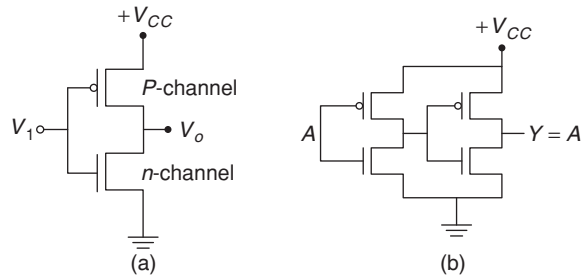
Figure 17 (a) A CMOS inverter, (b) CMOS non-inverting Buffer
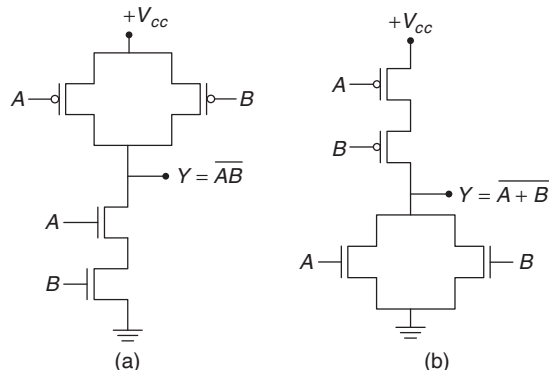
Figure 18 (a) 2-input CMOS NAND gate, (b) 2-input CMOS NOR gate

In CMOS logic, gates with larger number of inputs can be made by cascading gates with fewer inputs which are faster and smaller than the gates obtained by extending series parallel transistors.
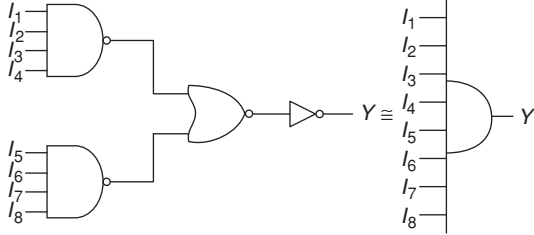
Internal structure and equivalent logic for eight input CMOS NAND.

In the given logical structure of eight input CMOS NAND gate, the total propagates delay of this circuit is less than the delay of one-level eight input NAND circuit.

CMOS logic levels are functions of supply voltage, and are approximately

$$V_{OH} = V_{CC} - 0.1 \text{ V}$$

$$V_{IH} = 0.7 V_{CC}, \ V_{IL} = 0.3 V_{CC}, \ V_{OL} = 0.1 \text{ V}$$

The DC margins are

$$\Delta 1 = V_{OH} - V_{IH} = V_{CC} - 0.1 \text{ V} - 0.7 V_{CC}$$

$$\Delta 0 = V_{IL} - V_{OL} = 0.3 V_{CC} - 0.1 \text{ V}$$

The CMOS noise margins are much higher than the TTL noise margins.

For HC series, CMOS current ratings are

$$I_{IH} = 1 \ \mu A, I_{IL} = -1 \ \mu A, I_{OH} = 0.02 \text{ mA}, I_{OL} = 0.2 \text{ mA}$$

$$\text{The low-sate fan out} = \frac{I_{OL}}{I_{IL}} = \frac{0.02}{0.001} = 20$$

$$\text{The HIGH-state fan out} = \frac{I_{OH}}{I_{IH}} = \frac{0.02}{0.001} = 20$$

An unused NAND or AND input should be tied to logic 1 level, voltage through a pull up resistor and an unused NOR/OR, input should be tied to logic 0 level voltage through a pull down resistor.

Due to the presence of parasitic transistors between V_{CC} and ground of any CMOS device for high input voltages, they cause a virtual short circuit, between V_{CC} and ground, resulting in a very high dissipation enough to destroy the device.

This condition is known as latch up, i.e., stay ON permanently to prevent latch up condition; modern CMOS logic circuits are fabrication with special structures like zener diodes at inputs, for protection.

CMOS transmission of a gate It is controlled by gate voltages C and $\overline{C}$, if $C = 1$ then signal transmitted from A to B, if $C = 0$ transmission is not possible.
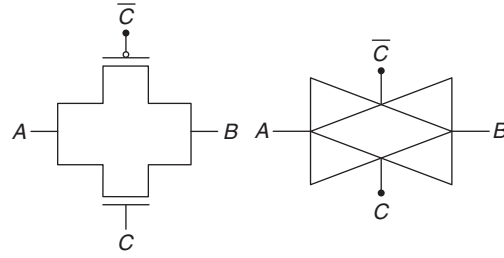
Solved Examples

Example 1: Simplify the Boolean function, $x \, y + x'z + y \, z$

Solution: $x \, y + x'z + y \, z$
By using consensus property
$xy + x'z + yz = xy + x'z$
$Y = xy + x'z$

Example 2: The output of the given circuit is equal to
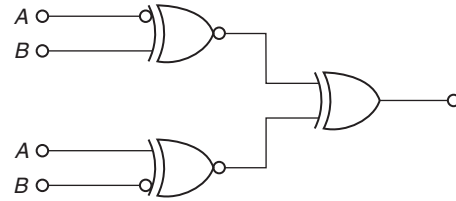
Solution: $\overline{A \odot B} = \overline{A}B + A\overline{B}$
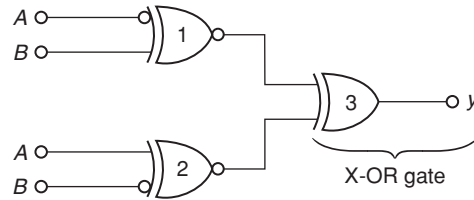
$$A \odot \overline{B} = \overline{A}B + A\overline{B}$$

So the output of above circuit is '0'. As two inputs are same at third gate. Output of X-OR gate with two equal inputs is zero.

$\therefore \ y = 0$

Example 3: The circuit shown in the figure is functionally equivalent to
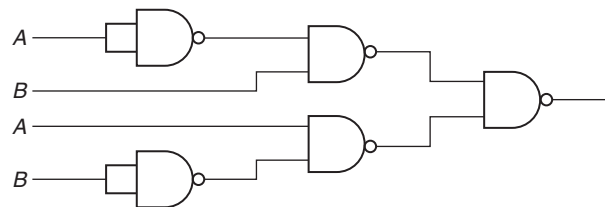
Solution:
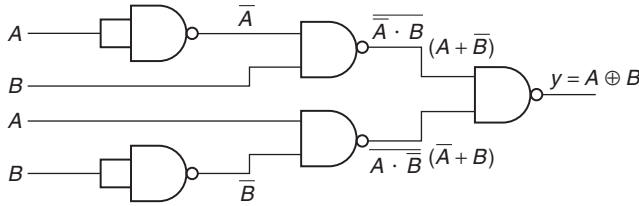
$$Y = \overline{(\overline{A \cdot B} \cdot \overline{A\overline{B}})} = \overline{(A+\overline{B})(\overline{A}+B)} \quad \because \quad (\overline{A \cdot B} = \overline{A} + \overline{B})$$

$$= \overline{(A+\overline{B})} + \overline{(\overline{A}+B)} = \overline{A} \cdot \overline{\overline{B}} + \overline{\overline{A}} \cdot \overline{B}$$

$$= \overline{A} \cdot B + A \cdot \overline{B} = A \oplus B$$

Example 4: Simplify the Boolean function $A \oplus \overline{A}B \oplus \overline{A}$

Solution: $A \oplus \overline{A}B \oplus \overline{A}$

Associativity

$$= 1 \oplus \overline{A}B = \overline{\overline{A}B}$$

$$= A + \overline{B} \quad (\because \quad \text{De morgan's})$$

Example 5:

CD\AB	00	01	11	10
00	0	0	1	1
01	0	×	×	1
11	×	×	1	×
10	1	0	1	1

The minimized expression for the given K-map is

Solution:

CD\AB	00	01	11	10
00	0	0	1	1
01	0	×	×	1
11	×	×	1	×
10	1	0	1	1

$$= A + \overline{B}C$$

Example 6: In the figure shown, y_2, y_1, y_0 will be 1's complement of $x_2 \, x_1 \, x_0$ if $z = $?
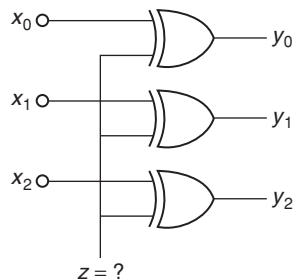
Solution: We are using X-OR gate
∴ X-OR output is complement of input only when other input is high.
∴ $Z = 1$

Example 7: The output y of the circuit shown is the figure is
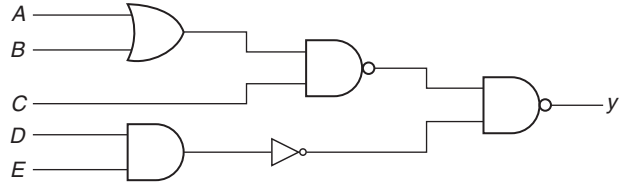
Solution:
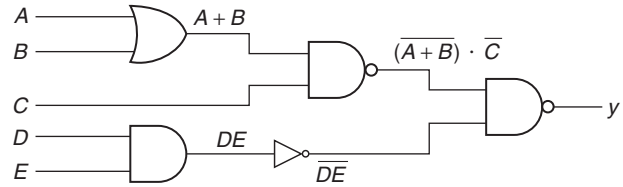
$$y = \overline{\overline{(A+B) \cdot C} \cdot \overline{DE}} = \overline{\overline{(A+B) \cdot C}} + \overline{\overline{DE}}$$

$$= (A+B)C + DE (\overline{x \cdot y} = \overline{x} + \overline{y})$$

Example 8: Simplify the following function

$$f = \overline{\overline{A(\overline{AB})} \cdot \overline{B(\overline{AB})}}$$

Solution: $\overline{\overline{A(\overline{AB})} \cdot \overline{B(\overline{A \cdot B})}}$

$$\overline{[A+(AB)] \cdot [B+(AB)]} = \overline{A+(AB)} + \overline{(B+AB)}$$

$$= \overline{A} \cdot \overline{(AB)} + \overline{B} \cdot \overline{(AB)} = \overline{A} \cdot (\overline{A}+\overline{B}) + \overline{B}(\overline{A}+\overline{B})$$

$$= \overline{A} \cdot \overline{A} + \overline{A}\overline{B} + \overline{B}\overline{A} + \overline{B} \cdot \overline{B} = \overline{A} + \overline{B} = \overline{AB}$$

Example 9: Which gate is represented by the circuit as shown in the figure?
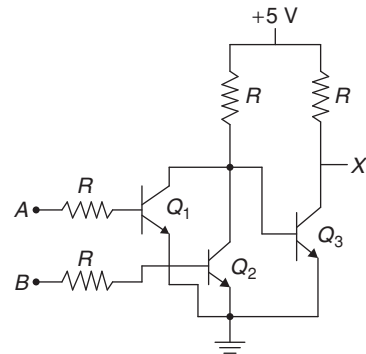
(A) NAND   (B) NOR
(C) OR   (D) AND

Solution: (C)
Transistors with A, B inputs form RTL–NOR gate, other transistor is inverter, so the circuit is OR gate. If any input is 1, either Q_1 or Q_2 will be in saturation, so Q_3 will be in cut off, $x \approx v_{cc}$ (logic 1), hence it is OR gate.

Example 10: In a 7400 TTL NAND gate, $V_{cc} = +5$ V and a 5 kΩ load is connected to its output. Find the output voltage

(i) when both the inputs are +5 V and
(ii) when both the inputs are 0 V

(A) .0.1 V, 4.09 V   (B) 4.8 V, 2.6 V
(C) 4.09 V, 2.26 V   (D) .1 V, 3 V

solution: (A)
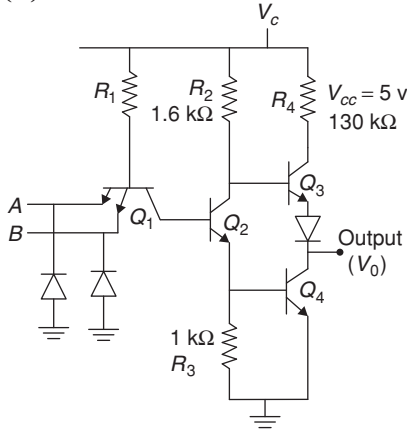
When both the inputs are high, i.e., +5 V, Q_2 and Q_4 are in saturation. When Q_4 is in saturation, its output is $V_{ce(sat)} = $ low = 0.1 V.

When both inputs are low 0 off the output is high.

(Q_3 is ON but Q_2 and Q_4 are off)

$$\therefore\ V_{OH} = V_{cc} - I_L R_4 - V_{ce(sat)} - V_D$$
$$= 5 - (I_{OH} \times 130) - .1 - .7$$
$$= (5 - 0.8 - 130 I_L)\ \text{V}$$

$$I_{OH} = \frac{V_{OH}}{5\ \text{k}\Omega}$$

$$V_{OH}\ 4.2 - 130 \times \frac{V_{OH}}{5000}\ \text{V}$$

$$V_{OH} = \frac{4.2}{1 + \dfrac{13}{500}}\ \text{V} = 4.09\ \text{V}.$$

EXERCISES

Practice Problems 1

Directions for questions 1 to 33: Select the correct alternative from the given choices.

1. The output of the following circuit is
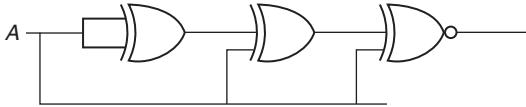
(A) 0   (B) 1
(C) A (D) A'

2. The circuit which will work as OR gate in positive level will work as ___ gate in negative-level logic
(A) NOR gate
(B) NAND gate
(C) Both NAND and NOR gate
(D) AND gate

3. Four logical expressions are given below:

(a) $\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D}\bar{E} \cdot \bar{F} \cdot \bar{G} \cdot \bar{H}$

(b) $\overline{AB} \cdot \overline{CD} \cdot \overline{EF} \cdot \overline{GH}$

(c) $\bar{A} + \bar{B} + \bar{C} + \bar{D} + \bar{E} + \bar{F} + \bar{G} + \bar{H}$

(d) $(\bar{A} + \bar{B})(\bar{C} + \bar{D})(\bar{E} + \bar{F})(\bar{G} + \bar{H})$

Two of these expression are equal. They are
(A) c and d   (B) b and d
(C) a and b   (D) a and c

4. For the logic circuit shown in figure, the simplified Boolean expression for the out put y is
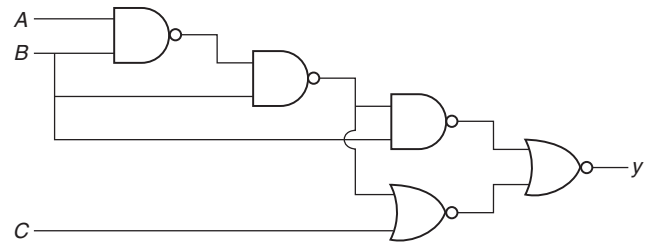
(A) $A + B + C$ (B) A
(C) $AB\bar{C}$ (D) $B\bar{C}$

5. In a digital system, there are three inputs A, B and C. The output should be high when at least two inputs are high. The minimized Boolean expression for the out put is
(A) $AB + BC + AC$

(B) $ABC + AB\bar{C} + \bar{A}BC + A\bar{B}C$

(C) $AB\bar{C} + A\bar{B}C + \bar{A}BC$

(D) $A\bar{B} + B\bar{C} + \bar{A}C$

6. Consider the following logic circuit whose inputs are functions f_1, f_2, f_3 and output is f.
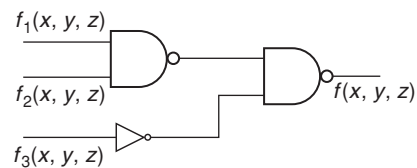
Given that $f_1(x, y, z) = \Sigma(0, 1, 3, 5)$ $f_2(x, y, z) = \Sigma(6, 7)$ and $f(x, y, z) = \Sigma(1, 4, 5)$, then f_3 is
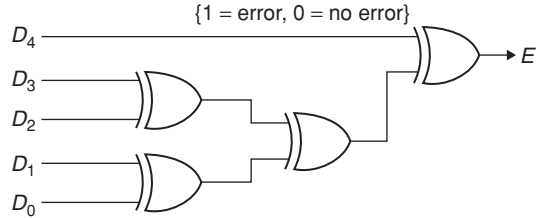
(A) $\Sigma(1, 4, 5)$
(B) $\Sigma(6, 7)$
(C) $\Sigma(0, 1, 3, 5)$
(D) None of these

7. The circuit shown above is to be used to implement the function $z = f(A, B) = \bar{A} + B$ what values are to be selected for I and J?
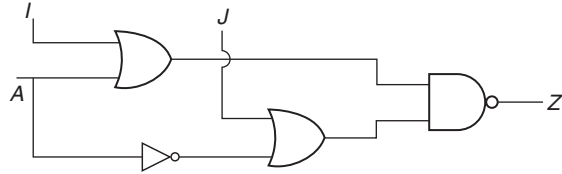

(A) $I = 0, J = B$
(B) $I = 1, J = B$
(C) $I = B, J = 1$
(D) $I = B, J = 0$

8. Parity checker output from the below figure, if input is 11111 $(D_4\, D_3\, D_2\, D_1\, D_0)$ and 10000 $(D_4\, D_3\, D_2\, D_1\, D_0)$.

(A) error, error
(B) error, no error
(C) no error, error
(D) no error, no error

9. For the given combinational network with three inputs A, B and C, three intermediate outputs P, Q and R, and two final outputs $X = P \cdot Q = \Sigma(0, 2, 4)$ and $Y = P \cdot R = \Sigma(1, 2, 4, 6)$ as shown below. Find the smallest function P(containing minimum number of min terms that can produce the output x and y).
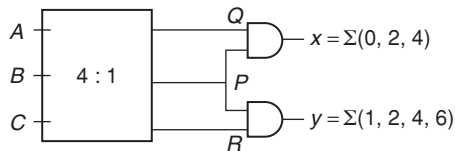
(A) $\Sigma(2, 4)$
(B) $\Sigma(0, 1, 2, 4, 6)$
(C) $\Sigma(3, 5, 7)$
(D) $\Sigma(1, 2, 6)$

10. The standard form of expression $AB + ACD + \bar{A}C$ is

(A) $AB\bar{C}\bar{D} + ABC\bar{D} + AB\bar{C}D + ABCD + A\bar{B}CD$
$+\bar{A}BCD + \bar{A}BC\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D}$

(B) $AB + ACD + \bar{A}C$

(C) $AB\bar{C} + ABC + ABCD + \bar{A}CB + \bar{A}CB\bar{D}$

(D) $\bar{A}\bar{B}\bar{C}\bar{D} + ABCD + \bar{A}BC + AB\bar{D} + ABC$

11. Factorize $\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}C\bar{D}$

(A) $B + C$
(B) $AB + CD$
(C) $\bar{B}\bar{C}$
(D) AC

12. The K-map of a function is as shown. Find the function.

(A) wx
(B) $\bar{z}$
(C) $\bar{w}(z + \bar{z}) + \bar{z}w$
(D) $\bar{w}x + \bar{z}$

13. The Boolean expression for P is
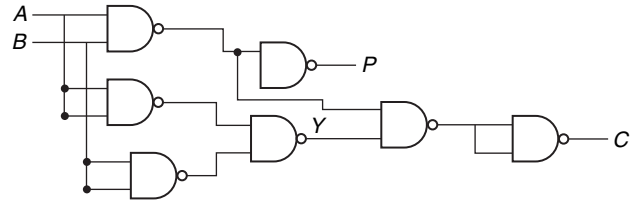
(A) AB
(B) $\overline{\overline{AB}}$
(C) $\bar{A} + \bar{B}$
(D) $A + B$

14. The Boolean expression for the truth table is

A	B	C	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

(A) $B(A+C)(\bar{A}+\bar{C})$
(B) $\bar{B}(A+\bar{C})(\bar{A}+\bar{C})$
(C) $B(A+\bar{C})(\bar{A}+C)$
(D) $\bar{B}(A+C)(\bar{A}+\bar{C})$

15. Simplify (d represents don't-care)

(A) $\bar{B}$
(B) $\bar{B}+C$
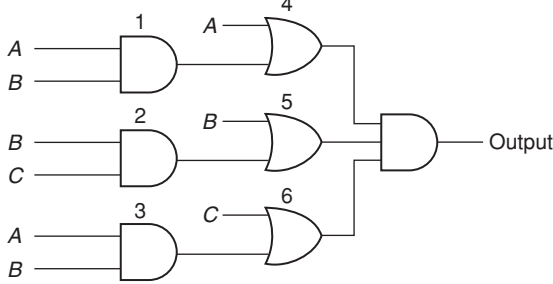(C) $\bar{B}+\bar{A}$
(D) $A+\bar{C}$

16. Simplify $\overline{(AB+\bar{C})(\bar{A}+B+C)}$

(A) $(\bar{A}+\bar{B}+\bar{C})\cdot(A+B+C)$

(B) $(\bar{A}+B+C)\cdot(A+\bar{B}+\bar{C})$

(C) $(\bar{A}+\bar{B})\cdot(A+B+C)$

(D) None of these

17. The point P in the figure is stuck at 1. The output f will be
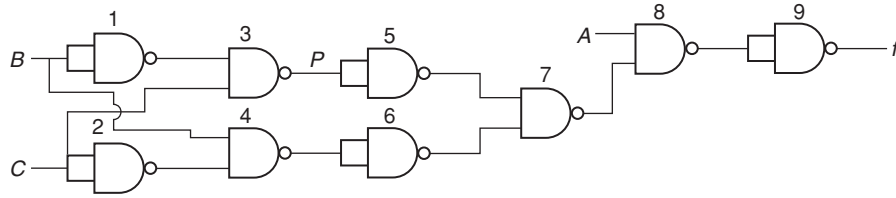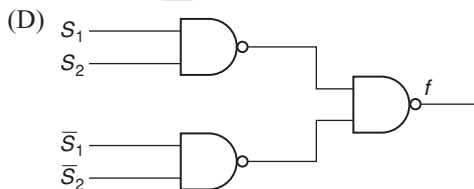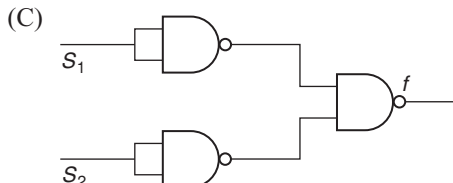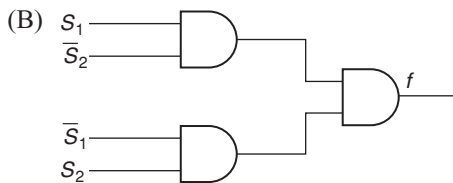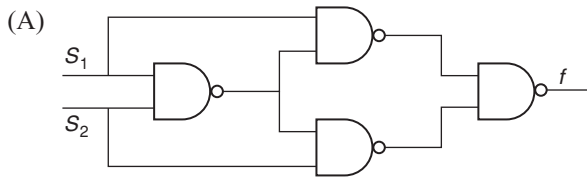

(A) $\overline{ABC}$ (B) $\overline{A}$ (C) $AB\overline{C}$ (D) A

18. Find the function represented by the figure
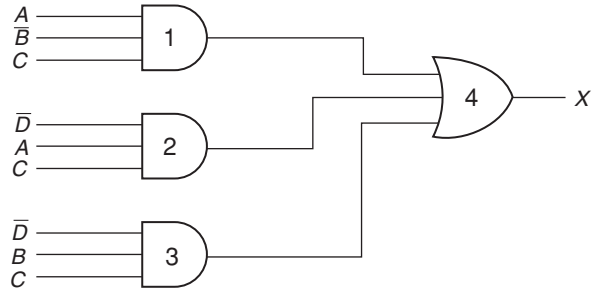

(A) $A + B + C$ (B) AB
(C) $AB + C$ (D) $B + C$

19. A staircase light is controlled by two switches, one is at the top of the stairs and other at the bottom of stairs. Realization of this function using NAND logic results in which of the following circuits? (Assume S_1 and S_2 are the switches)

(A)

(B)

(C)

(D)

20. For the given figure simplify the expression and find which is the redundant gate?

(A) $ABC + DBC, 4$ (B) $A\overline{B}C + \overline{D}AC, 3$
(C) $\overline{D}AC + \overline{D}BC, 1$ (D) $A\overline{B}C + \overline{D}BC, 2$

21. The function $f = A \oplus B \oplus C \oplus D$ is represented as
(A) $f(A, B, C, D) = \Sigma(2, 6, 10, 11, 12, 13, 14)$
(B) $f(A, B, C, D) = \Sigma(3, 5, 7, 10, 11, 12, 13, 14)$
(C) $f(A, B, C, D) = \Sigma(1, 2, 6, 8, 10, 12, 13, 14)$
(D) $f(A, B, C, D) = \Sigma(1, 2, 4, 7, 8, 11, 13, 14)$

22. Find the function represented
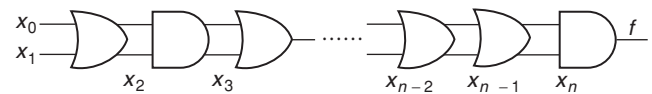
(A) $(x_0 + x_1)(x_2 + x_3)(x_4 + x_5) \ldots (x_{n-1} + x_n)$
(B) $x_0 + x_1 + x_2 + x_3 + \cdots + x_n$
(C) $x_0 x_2 x_4 \ldots x_n + x_1 x_2 \cdots x_n + x_{n-1} x_n$
(D) $x_0 x_1 + x_2 x_3 + \cdots + x_{n-1} x_n$

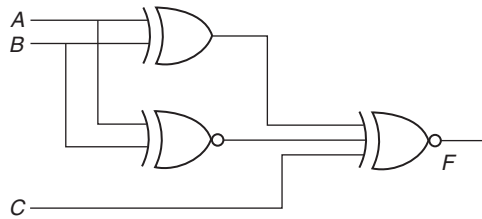**23.** The minimum number of NAND gates required to implement $A \oplus B \oplus C$ is
(A) 8   (B) 10
(C) 9   (D) 6

24. Which of the following circuit will generate an odd parity for a 4-bit input? (Assume ABCD as input)

(A)

(B)

(C)

(D)
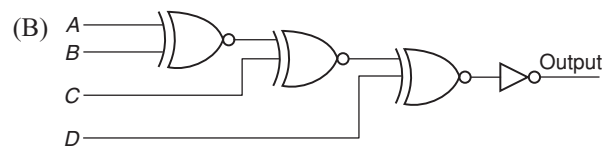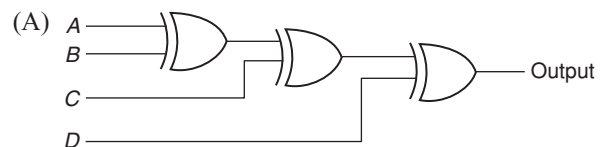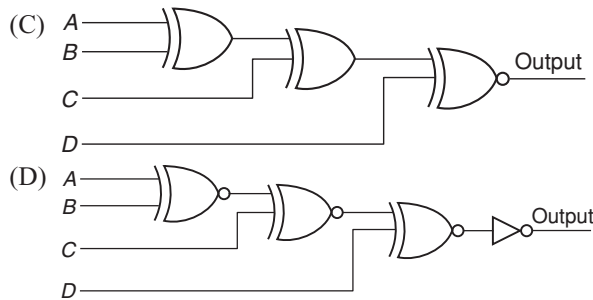
**25.** For the output F to be 1 in the circuit, the input combination should be

(A) $A = 1, B = 1, C = 0$
(B) $A = 1, B = 0, C = 0$
(C) $A = 0, B = 1, C = 0$
(D) $A = 0, B = 0, C = 1$

26. The highest noise margin is offered by
(A) TTL (B) ECL
(C) I²L (D) CMOS

27. A LSI IC Package contains _____ logic gates.
(A) 10 (B) 50
(C) less than 50 (D) more than 100

28. For interfacing two logic gates, the condition is
(A) $V_{OH} > V_{IH}, V_{IL} > V_{OL}$
(B) $V_{OH} < V_{IH}, V_{IL} < V_{OL}$
(C) $V_{OH} > V_{IH}, V_{IL} < V_{OL}$
(D) $V_{OH} = V_{IH}, V_{IL} = V_{OL}$

29. The I/O characteristics of which logic family is specified in the figure.
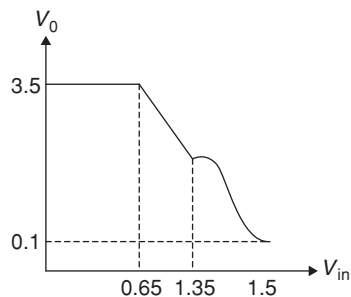
(A) TTL (B) CMOS
(C) I²L (D) DTL

30. The circuit diagram of a standard TTL NOT gate is shown. If input is 2.5 V, the modes of operation of transistor is
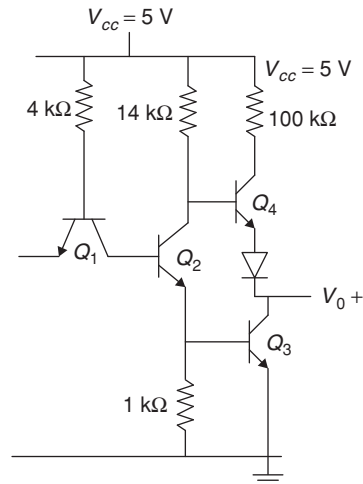
(A) Q_1: reverse active
Q_2: normal active
Q_3: saturation
Q_4: cut-off

(B) Q_1: reverse active
Q_2: saturation
Q_3: saturation
Q_4: cut-off

(C) Q_1: normal active
Q_2: cut-off
Q_3: cut-off
Q_4: saturation

(D) Q_1: saturation
Q_2: saturation
Q_3: saturation
Q_4: normal active

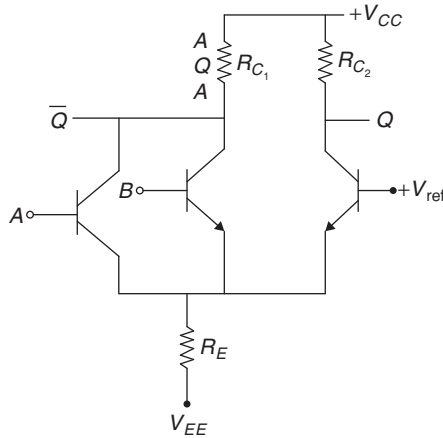**31.** The logic function implemented by the following circuit at output terminal is
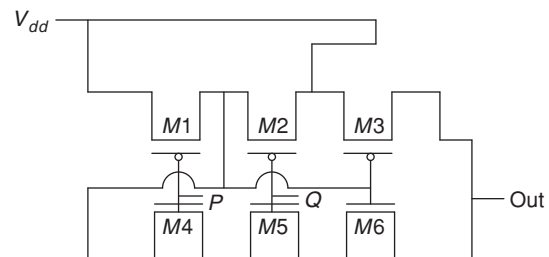
(A) P NOR Q (B) P NAND Q
(C) P OR Q (D) P AND Q

32. Match the options in column 1 with column 2

Column 1	Column 2
(a) TTL	1. Superfast computers
(b) NMOS	2. MSI
(c) CMOS	3. LSI
(d) ECL	4. VLSI

(A) a – 2, b – 3, c – 4, d – 1
(B) a – 3, b – 2, c – 4, d – 1

(C) a – 2, b – 3, c – 4, d – 1
(D) a – 1, b – 3, c – 1, d – 2

33. Which gate is represented by the circuit?


(A) NAND   (B) NOR
(C) OR   (D) AND

Practice Problems 2

Directions for questions 1 to 33: Select the correct alternative from the given choices.

1. An OR Gate has six inputs. How many input words are there in its truth table?
(A) 6   (B) 36
(C) 32   (D) 64

2. Sum of product form can be implemented by using
(A) AND–OR   (B) NAND–NAND
(C) NOR–NOR   (D) Both A and B

3. Which one of the following is equivalent to the Boolean expression?
$Y = AB + BC + CA$

(A) $\overline{AB + BC + CA}$

(B) $(\overline{A} + \overline{B})(\overline{B} + \overline{C})(\overline{A} + \overline{C})$

(C) $\overline{(A + B)(B + C)(A + C)}$

(D) $\overline{(\overline{A} + \overline{B})(\overline{B} + \overline{C})(\overline{C} + \overline{A})}$

4. What Boolean function does the following circuit represents?
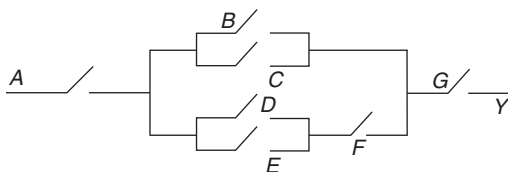
(A) $A\,[F + (B + C) \cdot (D + E)]\,G$
(B) $A + BC + DEF + G$
(C) $A\,[(B + C) + F\,(D + E)]\,G$
(D) $ABG + ABC + F(D + E)$

5. The minimum number of two input NOR gates are required to implement the simplified value of the following equation
$f(w, x, y, z) = \Sigma m(0, 1, 2, 3, 8, 9, 10, 11)$
(A) One   (B) Two
(C) Three   (D) Four

6. The output of a logic gate is '1' when all inputs are at logic '0'. Then the gate is either
(1) NAND or X-OR gate
(2) NOR or X-OR gate
(3) NOR or X-NOR gate
(4) NAND or X-NOR gate
(A) 1 and 2   (B) 2 and 3
(C) 3 and 4   (D) 4 and 1

7. If the functions w, x, y, and z are as follows.
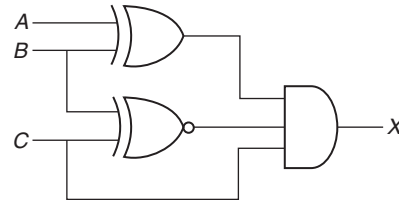
$w = R + \overline{P}Q + \overline{R}S$

$x = PQ\overline{R}\overline{S} + \overline{P}\overline{Q}\overline{R}S + P\overline{Q}\overline{R}\overline{S}$

$y = \overline{RS + PR + P\overline{Q} + \overline{\overline{P} \cdot \overline{Q}}}$

$z = R + S + \overline{PQ + \overline{P} \cdot \overline{Q} \cdot R + P \cdot \overline{Q} \cdot S}$

(A) $w = z$, $x = y$ (B) $w = z, x = \overline{z}$
(C) $w = y$ (D) $w = y = z$

8. For the logic circuit shown in the figure, the required input condition (A, B, C) to make the output $(x) = 1$ is

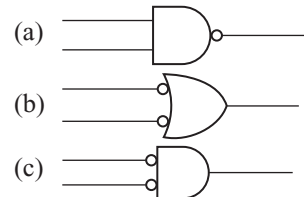(A) 0, 0, 1   (B) 1, 0, 1
(C) 1, 1, 1   (D) 0, 1, 1

9. Which of the following is a basic gate?
(A) AND   (B) X-OR
(C) X-NOR   (D) NAND

10. Which of the following represent the NAND gate?

(a)

(b)

(c)
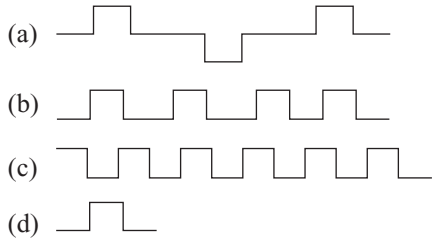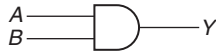
(A) a only   (B) a, b, c
(C) b, a   (D) a, c

11. The universal gates are
(A) NAND and NOR   (B) AND, OR, NOT
(C) X-OR and X-NOR   (D) All of these

12. In the circuit the value of input A goes from 0 to 1 and part of B goes from 1 to 0. Which of the following represent output under a static hazard condition?

(A) Output a   (B) Output b
(C) Output c   (D) Output d

13. The consensus theorem states that
   (A) $A + \bar{A}B = A + B$
   (B) $A + AB = A$
   (C) $AB + \bar{A}C + BC = AB + \bar{A}C$
   (D) $(A + B) \cdot (A + \bar{B}) = A$
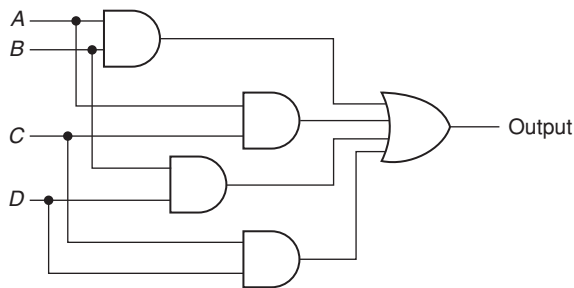
14. The dual form of expression

   $AB + \bar{A}C + BC = AB + \bar{A}C$ is

   (A) $(A + B)(\bar{A} + C)(B + C) = (A + B)(\bar{A} + C)$
   (B) $(A + B)(\bar{A} + C)(B + C) = (\bar{A} + \bar{B})(A + \bar{C})$
   (C) $(\bar{A} + \bar{B})(\bar{A} + \bar{C})(\bar{B} + \bar{C}) = (\bar{A} + \bar{B})(A + \bar{C})$
   (D) $\bar{A}\bar{B} + A\bar{C} + \bar{B}\bar{C} = \bar{A}\bar{B} + A\bar{C}$

15. The max term corresponding to decimal 12 is
   (A) $\bar{A} + \bar{B} + C + D$ (B) $A + B + \bar{C} + \bar{D}$
   (C) $\bar{A}\bar{B}CD$ (D) $AB\bar{C}\bar{D}$

16. The given circuit is equivalent to

   (A) $(A + C)(B + D)$ (B) $AC + BD$
   (C) $(A + D)(B + C)$ (D) $(\bar{A} + \bar{B})(\bar{C} + \bar{D})$

17. Minimized expression for Karnaugh map is

AB \\ C	00	01	11	10
0	1			1
1	1			1

   (A) $AB + C$ (B) $\bar{A}B + C$
   (C) $\bar{B}$ (D) $\bar{B} + C$

18. An X-OR gate will act as _____ when one of its input is one and as _____ when one of its input is zero.
   (A) buffer, buffer   (B) buffer, inverter
   (C) inverter, buffer   (D) inverter, inverter

19. The minimum number of two-input NAND gates required to implement $A \odot B$ if only A and B are available
   (A) 6   (B) 3
   (C) 5   (D) 4

20. Negative logic in a logic circuit is one in which
   (A) logic 0 and 1 are represented by GND and positive voltage respectively.
   (B) logic 0 and 1 are represented by negative and positive voltage.
   (C) logic 0 voltage level is lower than logic 1 voltage level.
   (D) logic 0 voltage level is higher than logic 1 voltage level.

21. If the input to a gate is eight in number, then its truth table contains _____ input words.
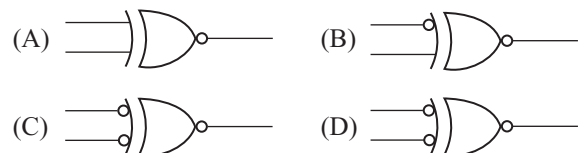   (A) 128   (B) 8
   (C) 64   (D) 256

22. The X-OR gate implementation using NAND gate is
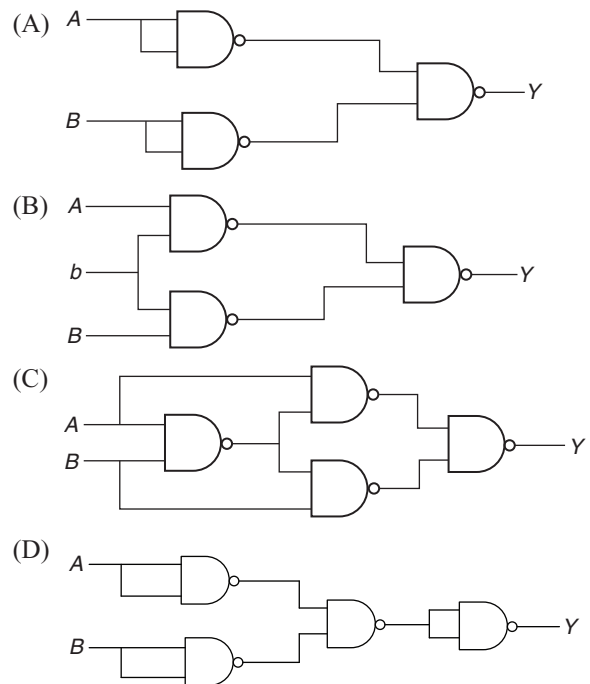
23. The equivalent of AND–OR logic circuit is
   (A) NAND–NOR   (B) NOR–AND
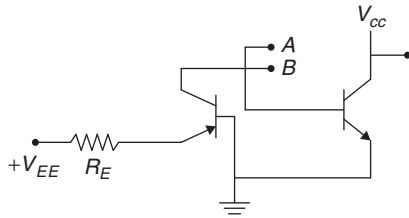   (C) NAND–NAND   (D) NAND–OR

24. The X-OR is equivalent to

25. Simplify $A\bar{B}C + B + B\bar{D} + AB\bar{D} + \bar{A}C$
   (A) B (B) $B + C$
   (C) $C + A$ (D) $\bar{A} + B$

26. The gate represented by the circuit is

    (A) NAND   (B)   NOR
    (C) OR   (D)   AND

27. The full form of I²L and ECL is
    (A) Inter-integrated logic and emitter-coupled logic
    (B) Inter-injection logic and emitter-combined logic
    (C) Integrated injection logic and emitter-coupled logic
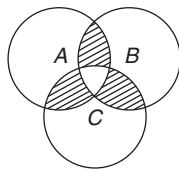   (D) Integrated Injection Logic and Emission-coupled logic

28. The most popular TTL family member among digital designers
    (A) High speed TTL
    (B) Standard TTL
    (C) Low power TTL
    (D) Low power schottky TTL

29. The totempole in standard TTL refers to
    (A) Output buffer
    (B) input emitter stage
    (C) open collector output state
    (D) phase splitter

30. Boolean expression for shaded portion is

    (A) $ABC + \overline{ABC}$

    (B) $AB + BC + CA$

    (C) $AB\overline{C} + A\overline{B}C + \overline{A}BC$

    (D) $AB\overline{C} + \overline{A}B\overline{C} + \overline{ABC}$

**31.** The output of the 74 series of TTL gates is taken from a BJT in
    (A) totempole and common collector configuration
    (B) Either totempole or open collector configuration
    (C) common base configuration
    (D) common collector configuration

**32.** The voltage transfer characteristics shown in that of
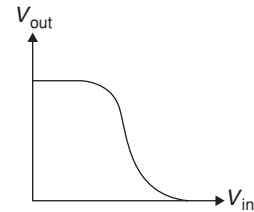
    (A) an NMOS inverter with enhancement mode transistor as load.
    (B) an NMOS inverter with depletion mode transistor as load
    (C) a CMOS inverter
    (D) a BJT inverter

**33.** Which of the following represent NMOS inverter?
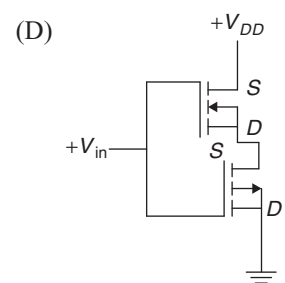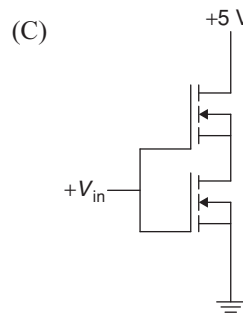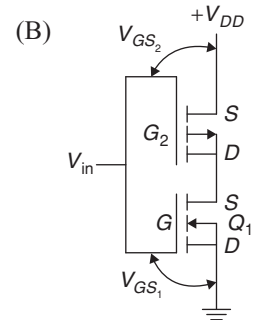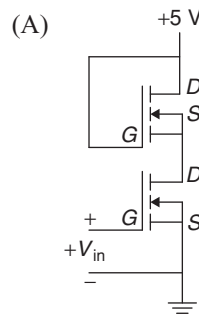
1. A, B, C and D are input bits, and Y is the output bit in the X-OR gate circuit of the figure below. Which of the following statements about the sum S of A, B, C, D and Y is correct? **[2007]**
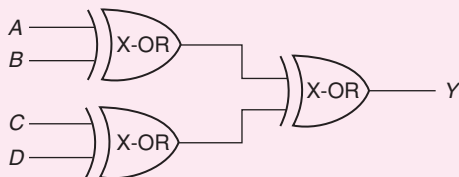
(A) S is always either zero or odd
(B) S is always either zero or even
(C) $S = 1$ only if the sum of A, B, C and D is even
(D) $S = 1$ only if the sum of A, B, C and D is odd

2. The octal equivalent of the HEX number $AB.CD$ is **[2007]**

(A) 253.314   (B) 253.632
(C) 526.314   (D) 526.632

3. The TTL circuit shown in the figure is fed with the waveform X (also shown). All gates have equal propagation delay of 10 ns. The output Y of the circuit is **[2010]**
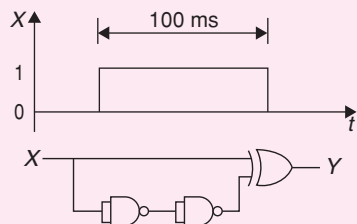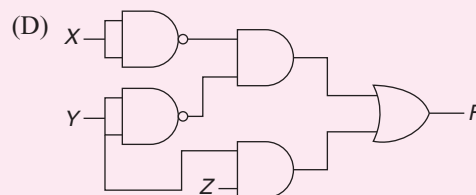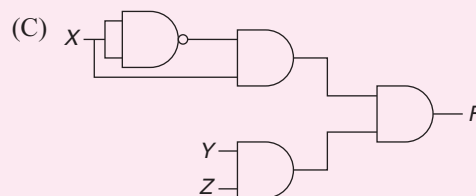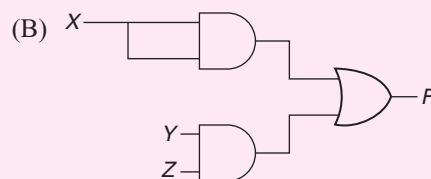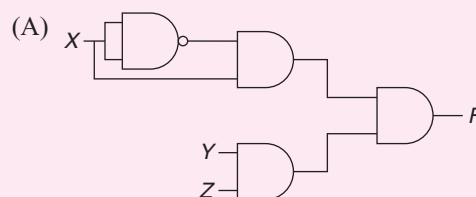

(A)

(B)

(C)

(D)

Common Data for Questions 4 and 5: The following karnaugh map represents a function F.

4. A minimized form of the function F is **[2010]**

(A) $F = \overline{X}Y + YZ$ (B) $F = \overline{X}\,\overline{Y} + YZ$
(C) $F = \overline{X}\,\overline{Y} + Y\overline{Z}$ (D) $F = \overline{X}Y + \overline{Y}Z$

5. Which of the following circuits is a realization of the above function F? **[2010]**

(A)

(B)

(C)

(D)

6. The output Y of the logic circuit given below is **[2011]**
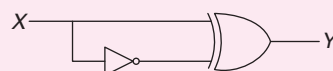

(A) 1   (B) 0
(C) X (D) $\overline{X}$

7. In the sum of products function $f(X, Y, Z) = \Sigma(2, 3, 4, 5)$, the prime implicants are **[2012]**

(A) $\overline{XY}, X\overline{Y}$

(B) $\overline{XY}, X\overline{Y}\,\overline{Z}, X\overline{Y}Z$

(C) $\overline{XY}\,\overline{Z}, \overline{X}YZ, X\overline{Y}$

(D) $\overline{XY}\,\overline{Z}, \overline{X}YZ, X\overline{Y}\,\overline{Z}, X\overline{Y}Z$

8. A bulb in a staircase has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches irrespective of the state of the other switch. The logic of switching of the bulb resembles **[2013]**
   (A) an AND gate
   (B) an OR gate
   (C) an X-OR gate
   (D) a NAND gate

9. In the circuit shown below, Q_1 has negligible collector-to-emitter saturation voltage and the diode drops negligible voltage across it under forward bias. If V_{cc} is +5 V, X and Y are digital signals with 0 V as logic 0 and V_{cc} as logic 1, then the Boolean expression for Z is **[2013]**
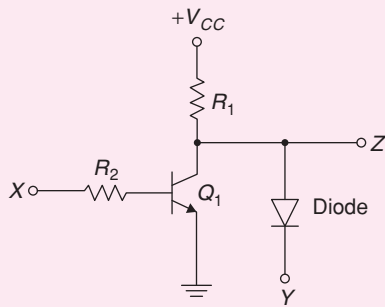
(A) XY

(B) $\overline{XY}$

(C) $X\overline{Y}$

(D) $\overline{X}Y$

10. Which of the following logic circuits is a realization of the function F whose karnaugh map is shown in figure **[2014]**

C\\AB	00	01	11	10
0	1	1		
1		1	1	

(A)

(B)

(C)

(D)
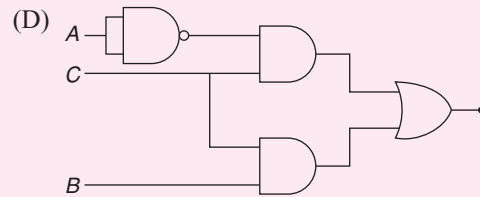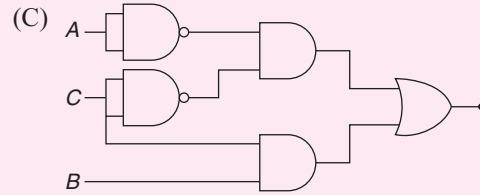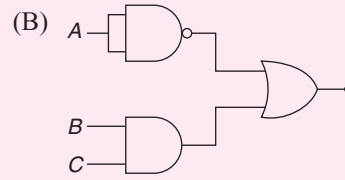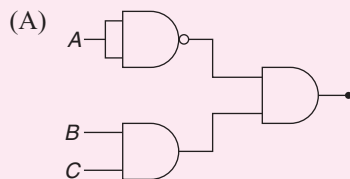
11. Which of the following is an invalid state in an 8-4-2-1 Binary-Coded Decimal counter **[2014]**
    (A) 1 0 0 0
    (B) 1 0 0 1
    (C) 0 0 1 1
    (D) 1 1 0 0

12. The SOP (sum of products) form of a Boolean function is $\Sigma(0, 1, 3, 7, 11)$, where inputs are A, B, C, D (A is MSB, and D is LSB). The equivalent minimized expression of the function is **[2014]**

13. $f(A, B, C, D) = \prod M(0, 1, 3, 4, 5, 7, 9, 11, 12, 13, 14, 15)$ is a maxterm representation of a Boolean function $f(A, B, C, D)$ where A is the MSB and D is the LSB. The equivalent minimized representation of this function is **[2015]**
    (A) $(A + \overline{C} + D)(\overline{A} + B + D)$
    (B) $A\overline{C}D + \overline{A}BD$
    (C) $\overline{A}C\overline{D} + A\overline{B}C\overline{D} + AB\overline{C}\,\overline{D}$
    (D) $(B + \overline{C} + D)(A + \overline{B} + \overline{C} + D)(\overline{A} + B + C + D)$

14. Consider the following Sum of Products expression, F. **[2015]**

$F = ABC + \overline{A}\,\overline{B}C + A\overline{B}C + \overline{A}BC + \overline{A}\,\overline{B}\,\overline{C}$

The equivalent Product of Sums expression is
(A) $F = (A + \overline{B} + C)(\overline{A} + B + C)(\overline{A} + \overline{B} + C)$
(B) $F = (A + \overline{B} + \overline{C})(A + B + C)(\overline{A} + \overline{B} + \overline{C})$
(C) $F = (\overline{A} + B + \overline{C})(A + B + \overline{C})(A + B + C)$
(D) $F = (\overline{A} + \overline{B} + C)(A + B + \overline{C})(A + B + C)$

(A) $(\bar{B}+C)(\bar{A}+C)(\bar{A}+\bar{B})(\bar{C}+D)$

(B) $(\bar{B}+C)(\bar{A}+C)(\bar{A}+\bar{C})(\bar{C}+B)$

(C) $(\bar{B}+C)(\bar{A}+C)(\bar{A}+\bar{C})(\bar{C}+\bar{D})$

(D) $(\bar{B}+C)(A+\bar{B})(\bar{A}+\bar{B})(\bar{C}+D)$

15. The output expression for the Karnaugh map shown below is **[2016]**

BC \ A	00	01	11	10
0	1	0	0	1
1	1	1	1	1

(A) $A+\bar{B}$ (B) $A+\bar{C}$
(C) $\bar{A}+\bar{C}$ (D) $\bar{A}+C$

16. The Boolean expression $\overline{\left(a+\bar{b}+c+\bar{d}\right)+\left(b+\bar{c}\right)}$ simplifies to **[2016]**
(A) 1 (B) $\overline{a.b}$
(C) $a.b$ (D) 0

ANSWER KEYS

EXERCISES

Practice Problems 1

1. B	**2.** D	**3.** B	**4.** C	**5.** A	**6.** A	**7.** B	**8.** A	**9.** B	**10.** A
11. C	**12.** D	**13.** A	**14.** A	**15.** A	**16.** A	**17.** D	**18.** B	**19.** A	**20.** D
21. D	**22.** C	**23.** A	**24.** C	**25.** D	**26.** D	**27.** D	**28.** A	**29.** A	**30.** B
31. D	**32.** C	**33.** B							

Practice Problems 2

1. D	**2.** D	**3.** D	**4.** C	**5.** A	**6.** C	**7.** B	**8.** D	**9.** A	**10.** C
11. A	**12.** D	**13.** A	**14.** A	**15.** A	**16.** C	**17.** C	**18.** C	**19.** C	**20.** D
21. D	**22.** C	**23.** C	**24.** B	**25.** B	**26.** A	**27.** C	**28.** D	**29.** A	**30.** C
31. B	**32.** C	**33.** A							

Previous Years' Questions

1. D	**2.** B	**3.** A	**4.** B	**5.** D	**6.** A	**7.** A	**8.** C	**9.** B	**10.** C
11. D	**12.** A	**13.** C	**14.** A	**15.** B	**16.** D				