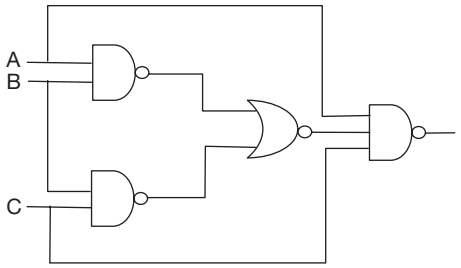
COMPUTER ORGANIZATION AND ARCHITECTURE TEST 5

Number of Questions: 35 **Section Marks: 30**

Directions for questions 1 to 35: Select the correct alternative from the given choices.

1. The output of the following circuit is:



(A) $\overline{A}\overline{B} + \overline{B}\overline{C}$ (B) $\overline{A}\overline{B} + \overline{B}\overline{C} + \overline{A}\overline{C}$
(C) $\overline{A} + \overline{B} + \overline{C}$ (D) $\overline{AB + BC}$

2. Match the following:
List I (Numbers in Decimal)
List II (equivalents in signed 2's complement representation)

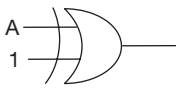
	List-I		List-II
P.	– 43	1.	01100000
Q.	– 78	2.	00110110
R.	+ 54	3.	111010101
S.	+ 96	4.	10110010

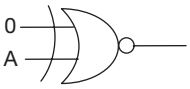
(A) P–3, Q–4, R–1, S–2
(B) P–4, Q–3, R–1, S–2
(C) P–3, Q–4, R–2, S–1
(D) P–4, Q–3, R–1, S–2

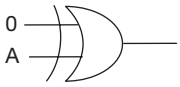
3. Which one of the following function will satisfy the property, "Dual of function = complement of the function"?
(A) $f(A, B, C) = \Sigma m\ (0, 1, 2, 3)$
(B) $f(A, B, C) = \Sigma m\ (4, 5, 6, 7)$
(C) $f(A, B, C) = \Sigma m\ (0, 2, 4, 6)$
(D) $f(A, B, C) = \Sigma m\ (0, 1, 6, 7)$

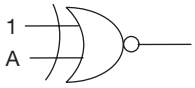
4. The number of min terms for the function $F(a, b, c, d, e) = b + cd$ is:
(A) 24 (B) 20
(C) 32 (D) 16

5. Which of the following will work like an inverter?

(P) 

(Q) 

(R) 

(S) 

(A) P, Q (B) Q, R
(C) R, S (D) P, S

6. Perform the following operation in 2's complement signed representation, and specify the result in 2's complement signed notation.

$(-13)_{10} + (-28)_{10} = ?$

(A) 10101001 (B) 11010111
(C) 11010110 (D) 00101001

7. Convert the following number to base 9.

$(1101222.201121)_3$

(A) 1358.647 (B) 4172.647
(C) 4178.153 (D) 1358.153

8. Which of the following is usually regarded as a bottleneck to von-Neumann computer Architecture?
(A) ALU
(B) Instruction set
(C) Processor/memory interface
(D) Control unit

9. Which of the following is the largest storage unit in a usual memory hierarchy?
(A) Cache memory (B) Main memory
(C) Register (D) Hard disk

10. Which type of cache miss does not occur in fully-Associative cache memory?
(A) Capacity miss (B) Conflict miss
(C) Compulsory miss (D) Cold start miss

11. Which of the following statement is FALSE?
(A) Pipelining does not improve the execution time of a single task.
(B) Pipelining improves the throughput of the total work load.
(C) Pipeline speed is limited by the slowest pipeline stage.
(D) In pipelining, only one task is processed at a time.

12. What is the execution time per stage of a pipeline that has 4 equal stages and a mean overhead of 12 cycles?
(A) 3 cycles (B) 4 cycles
(C) 6 cycles (D) 12 cycles

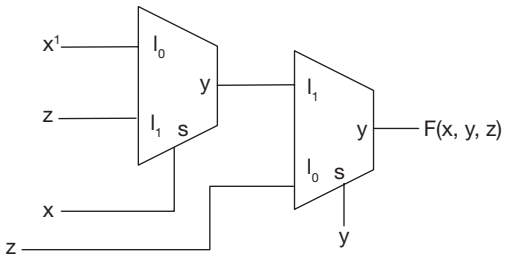
13. How many bits are needed to represent a direct address on a 64-bit machine?
(A) 6-bits (B) 64-bits
(C) 32-bits (D) 2^{64}-bits

14. A program has 5% divide instructions. Any non-divide instruction takes one cycle. All divide instructions take 25 cycles. What percent of CPU time is spent just doing divides?
(A) 100% (B) 95%
(C) 56.82% (D) 28.41%

15. Which of the following is not an advantage of memory mapped technique?
(i) Simple hardware
(ii) Simple instruction size
(iii) All address modes available
(iv) More memory address space
(A) (i), (iv) only (B) (iv) only
(C) (i), (ii), (iii) only (D) (iii), (iv) only

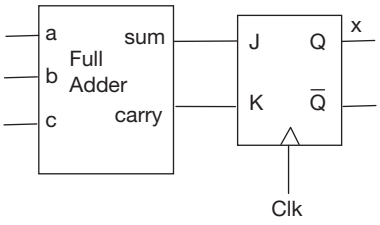
16. How many number of 2-input NAND gates are required to implement $f(A, B, C, D) = \Sigma m\ (1, 3, 4, 5, 6, 7, 9, 11, 12, 13, 14, 15)$?
(A) 4 (B) 3
(C) 2 (D) 1

17. The output of the following Multiplexer circuit is:



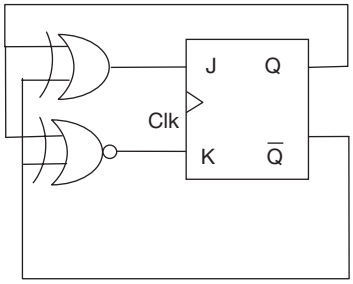
(A) $x^1 + yz$ (B) $x^1 y + z$
(C) $(x^1 + y)z$ (D) $x^1 y^1 + yz + xy^1 z$

18. Initially $Q_n = 0$, $\overline{Q}_n = 1,$, after clock pulse $Q_{n+1} = 1$, $\overline{Q}_{n+1} = 0$, which of the following correctly specifies about the inputs a, b, c?



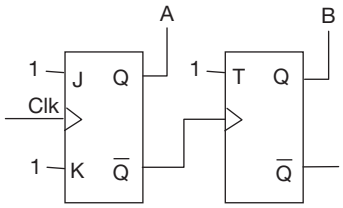
(A) two or more inputs should be 1.
(B) only one input has to be 1, or all inputs should be 1.
(C) c should be zero, a, b, can be either 11 or 00
(D) All inputs should be zero.

19. The states of Q, $\overline{Q}$ after a clock pulse are:



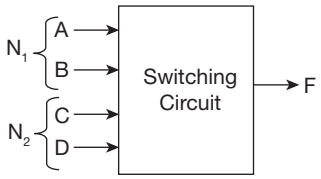
(A) 0, 1 (B) 1, 0
(C) 1, 1
(D) cannot be determined without initial states

20. The initial state of counter is $AB = 01$. What is the output (AB) after first clock pulse?



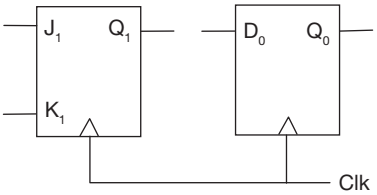
(A) 10 (B) 11
(C) 01 (D) 00

21. A switching circuit has four inputs as shown below. A and B represent the first and second bits of a binary number N_1, C and D represent the first and second bits of a binary number N_2.
The output is 1 only, if the product $N_1 \times N_2$ is less than or equal to 2.
The minimum POS form of $F(A, B, C, D)$ is



(A) $\overline{A}\overline{B} + \overline{C}\overline{D} + \overline{A}\overline{C} + \overline{A}\overline{D} + \overline{B}\overline{C}$
(B) $(A + C)\,(A + B + D)\,(B + C + D)$
(C) $(\overline{A} + \overline{D})(\overline{A} + \overline{B} + \overline{D})(\overline{B} + C + \overline{D})$
(D) $(\overline{A} + \overline{C})(\overline{A} + \overline{B} + \overline{D})(\overline{B} + \overline{C} + \overline{D})$

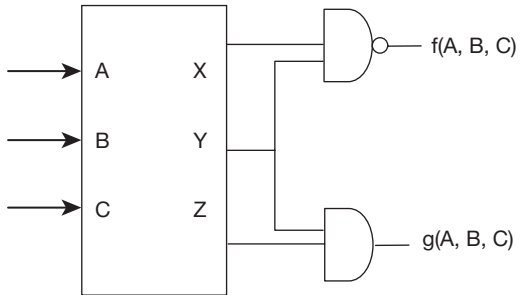
22. The synchronous counter which follows $(Q_1\ Q_0)$ $00 \rightarrow 10 \rightarrow 11 \rightarrow 01 \rightarrow 00$ by using JK-flip flop and D-flip flop, has inputs as



(A) $J_1 = \overline{Q}_1, K_1 = Q_0, D_0 = Q_0$
(B) $J_1 = Q_1, K_1 = \overline{Q}_1, D_0 = Q_0$
(C) $J_1 = \overline{Q}_0, K_1 = Q_0, D_0 = Q_1$
(D) $J_1 = Q_0, K_1 = \overline{Q}_0, D_0 = Q_1$

23. The minimum SOP form of:
(A) $\overline{P} + QR$ (B) $\overline{P} + Q$
(C) $\overline{P}\overline{Q} + R$ (D) P

24. A combinational circuit has 3 inputs A, B, C, and 3 outputs X, Y, Z. And the functions $f(A, B, C)$ and $g(A, B, C)$ are generated from the combinational logic circuit as shown here with NAND, AND gates. Find the least possible minterm expression for $Y(A, B, C)$.
$f(A, B, C) = \Sigma m(1, 3, 4, 5, 7)$
$g(A, B, C) = \Sigma m(4, 6)$
$Y(A, B, C) = \Sigma m(?)$



(A) $\Sigma m(0, 2, 3, 6, 7)$ (B) $\Sigma m(1, 3, 4, 5, 7)$
(C) $\Sigma m(0, 2, 4, 6)$ (D) $\Sigma m(0, 2, 4)$

25. From the above data, for which input A, B, C. The outputs all X, Y, Z will become 111 (i.e., $XYZ = 1$)
(A) 010 (B) 101
(C) 100 (D) 110

26. What is the speed up of the pipeline, which is executing 10 tasks. Consider the mean overhead of the pipeline as 5 and an execution time per stage as 1 cycle.
(A) 4.5 (B) 4
(C) 3 (D) 5

27. Consider a 32-bit computer that has an on-chip 16 Kbyte four-way set-associative cache. Assume that the cache has a line size of four 32-bit words. Then what will be Tag, Set and Word fields respectively:
(A) 18, 8, 6 (B) 18, 10, 4
(C) 20, 8, 4 (D) 20, 10, 2

28. Consider a memory of 64 blocks (labelled 0 through 63) and a cache of 8 lines (labelled 0 through 7). Using direct mapping, which of the following blocks of memory contend for line 2 of the cache?
(i) Block 10 (ii) Block 15
(iii) Block 20 (iv) Block 55
(v) Block 42 (vi) Block 63
(A) (i), (iii), (v) only (B) (i), (v) only
(C) (i), (ii), (iv) only (D) All the six

29. Convert the decimal number –30.375 to IEEE 754 Floating-point format. Which of the following correctly specifies the hexa-decimal equivalent of converted number?
(A) C1F30000 (B) 82830000
(C) 02830000 (D) 41F30000

30. Consider a main memory system that consists of Eight memory modules attached to the system bus, which is one word wide. When a write request is made the bus in occupied for 100 ns by the data, address and control signals. During the same 100 ns and for 500 ns thereafter, the addressed memory module executes one cycle accepting and storing the data. The internal operation of different memory modules may overlap in time, but only one request can be on the bus at any time. What is the maximum number of stores that can be initiated in one second?
(A) 10^9 (B) 10^7
(C) 10^5 (D) 10^2

31. Suppose a bus protocol requires 15 ns for devices to make requests, 15 ns for arbitration and 20 ns to complete each operation. How many operations can be completed per second?
(A) 10^7 (B) 2×10^7
(C) 5×10^7 (D) 50

32. A computer truncates the significant to four decimal places and gives the results in normalized form. What is the resultant of $(0.2233 \times 10^2) + (0.6688 \times 10^1)$?
(A) 0.2901×10^2 (B) 2.9018×10^1
(C) 0.2902×10^2 (D) 29.018

33. For each of the following cases, specify whether SRAM or DRAM would be more appropriate building block for the memory system?
(i) A memory system where performance is the most important goal.
(ii) A memory system where cost is the most important goal.
(A) SRAM, SRAM
(B) SRAM, DRAM
(C) DRAM, SRAM
(D) DRAM, DRAM

Linked answer questions 34 and 35:
Consider an unpipelined processor. Assume that it has 1 ns clock cycle and it uses 3 cycles for ALU operations, 5 cycles for branch instructions and 4 cycles for memory operations. Assume that the relative frequencies of these operations are 80%, 10% and 10% respectively. Suppose that due to clock skew and set up, pipelining the processor adds 0.1 ns of overhead to the clock.

34. What is the average instruction execution time on a pipelined processor?
(A) 4.3 ns (B) 4.4 ns
(C) 1.1 ns (D) 1 ns

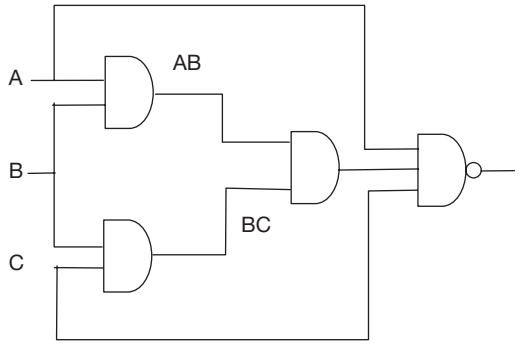
35. By ignoring latency impact, what is the speedup gain in the instruction execution rate using pipeline?
(A) 4.3 (B) 3.9
(C) 1.1 (D) 1

Answer Keys

1. C	**2.** C	**3.** D	**4.** B	**5.** A	**6.** B	**7.** A	**8.** C	**9.** D	**10.** B
11. D	**12.** B	**13.** B	**14.** C	**15.** B	**16.** B	**17.** B	**18.** B	**19.** B	**20.** B
21. D	**22.** C	**23.** A	**24.** C	**25.** D	**26.** B	**27.** C	**28.** B	**29.** A	**30.** B
31. B	**32.** A	**33.** B	**34.** C	**35.** B					

Hints and Explanations

1. In the circuit NAND – NOR structure can be redrawn as AND – AND Structure.



$\overline{A \cdot ABC \cdot C} = \overline{ABC} = \bar{A} + \bar{B} + \bar{C}$ Choice (C)

2. Positive numbers will be represented in their original binary magnitude but sign bit will be zero (0) to make it as positive number.
Negative Numbers are represented as 2's complement of their positive number representation in 2's complement signed number.
+ 43 = 00101011
– 43 = 11010101 (By taking 2's complement)
+ 78 = 01001110
– 78 = 10110010 (By taking 2's complement)
+ 54 = 00110110
+ 96 = 01100000 Choice (C)

3. Dual of function can be obtained by making min terms to max terms, i.e., 0 to 1, 1 to 0.
Dual of
000 ↔ 111
001 ↔ 110
010 ↔ 101
011 ↔ 100
$f = \Sigma m\ (0, 1, 6, 7)$
Dual is $f^D = \pi\ m\ (7, 6, 1, 0)$
$= \pi\ m\ (0, 1, 6, 7)$
$= \Sigma\ m\ (2, 3, 4, 5)$
Which is equal to $\bar{f}$ (complement of f). Choice (D)

4. $F = b + cd$
The term 'b' = - b - - - will have 16 min terms, the term cd = - - cd - will have 8 min terms out of those 4 min terms, have 'b'.
So remaining are 8 – 4 = 4
So total min terms = 16 + 4 = 20 Choice (B)

5. P is $1 \oplus A = \bar{A} \cdot 1 + A \cdot \bar{1} = \bar{A}$
Q is $A \odot 0 = \bar{A} \cdot 1 + A \cdot 0 = \bar{A}$
R is $0 \oplus A = \bar{A} \cdot 0 + A \cdot \bar{0} = A$
S is $1 \odot A = 1 \cdot A + 0 \cdot \bar{A} = A$
So P, Q work like inverter. Choice (A)

6. $(-13)_{10} + (-28)_{10} = (-41)_{10}$
The operation in 2's complement signed representation also given the same answer.
$(-41)_{10}$ is signed 2's complement representation is 11010111 ($\because$ +41 = 00101001) Choice (B)

7. Base 9 and base 3 are related ($3^2 = 9^1$). 2 digits of base 3 is equal to base 9.

Base-3	Base-9
01	1
02	2
10	3
11	4
12	5
20	6
21	7
22	8
100	10

Given number in base 3 is
01 10 12 22 · 20 11 21
1 3 5 8 · 6 4 7
$= (1358 \cdot 647)_9$ Choice (A)

8. In Von-Neumann computer architecture, most of the time is used for transferring data or instructions from memory to CPU. This is the bottleneck of Von-Neumann computer. Choice (C)

9. Choice (D)

10. In full-Associative cache, we can place any block of main memory at any line of cache. So there will be no conflict miss. Choice (B)

11. In pipelining, several tasks are processed simultaneously. Choice (D)

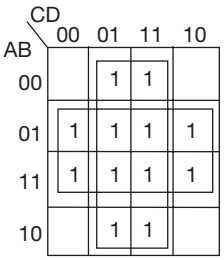
12. If there are k stages and each stage take T cycles then $(k-1)\ T$ = Pipeline mean overhead
$\Rightarrow \quad (4-1) \times T = 12$
$\Rightarrow \quad T = 4$ cycles. Choice (B)

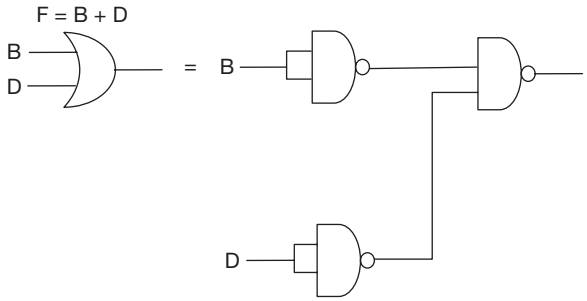
13. A 64-bit machine has 2^{64} locations. To address these locations, we require 64-bits. Choice (B)

14. Total time required to execute the given program
$= (0.95) * 1 + (0.05) * 25 = 0.95 + 1.25 = 2.2$
Time taken for Divide Operations $= 0.05 * 25 = 1.25$
$\therefore$ Percentage of CPU time spent on divides
$= \frac{1.25}{2.2} * 100 = 56.82\%$. Choice (C)

15. Using memory mapped technique, the memory address space will be reduced. Choice (B)

16. $f(A, B, C, D) = \Sigma m\,(1, 3, 4, 5, 6, 7, 9, 11, 12, 13, 14, 15)$





$F = B + D$. So 3, 2–input NAND gates are required to implement $F(A, B, C, D)$

Choice (B)

17. The first multiplexer output is
$y = I_0\bar{s} + I_1 s$
$= x^1 \cdot x^1 + zx = x^1 + zx = x^1 + z$
$F = (x^1 + z)y + z \cdot y^1 = x^1 y + yz + y^1 z$
$= x^1 y + (y + y^1)z = x^1 y + z$ Choice (B)

18. $Q_n = 0$, $Q_{n+1} = 1$
i.e., the state gets toggled i.e., when $J = 1$, $K = 1$
or the next state is set, $Q_{n+1} = 1$ i.e., when $J = 1$, $K = 0$
so $J = 1$, $k = x$ (either zero or 1)
so sum should be one, carry either zero or one.
So a, b, c should have only one 1 (sum = 1, carry = 0)
All inputs a, b, c can be 1 so that sum = 1, carry = 1.
Choice (B)

19. $J = Q_n \oplus \bar{Q}_n$(EXOR of $Q, \bar{Q}$) $= 1$

$K = Q_n \,\Theta\, \bar{Q}_n$(EXNOR of $Q, \bar{Q}$) $= 0$

When $J = 1$, $K = 0$, next clock pulse will give

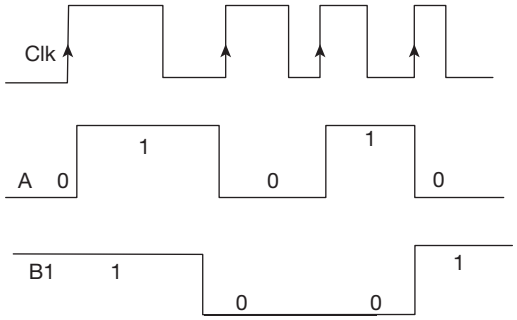
$Q = 1$, $\bar{Q} = 0$ Choice (B)

20. Given circuit is an Asynchronous counter, as clock is connected to rising edge.

$\bar{Q}$ connected to rising edge means this is an UP counter A is LSB, B is MSB.

$\bar{Q}_A$ connected to rising edge.

i.e., for every falling edge of Q_A, B will change so $AB = 11$

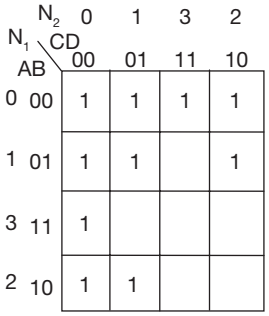


Clk	BA
0	10
1	11
2	00
3	01
4	10

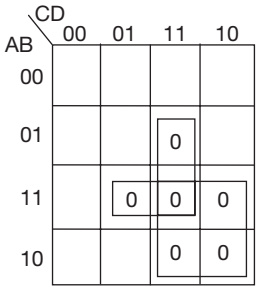
$\bar{Q}_A$ connected to rising edge.

i.e., for every falling edge of Q_A, B will change so $AB = 11$ Choice (B)

21.



The max terms will be (for POS form)



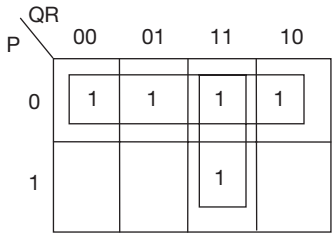
So $F = (\bar{A} + \bar{C})(\bar{B} + \bar{C} + \bar{D})(\bar{A} + \bar{B} + \bar{D})$ Choice (D)

22.

Present state		Next state		Inputs		
Q_1	Q_0	Q_1	Q_0	J_1	K_1	D_0
0	0	1	0	1	X	0
1	0	1	1	X	0	1
1	1	0	1	X	1	1
0	1	0	0	0	X	0

From the above table,
Writing the inputs interms of present state
$D_0 = Q_1, J_1 = \bar{Q}_0, K_1 = Q_0$ Choice (C)

23. Given function is in standard POS Form
$F(P, Q, R) = \pi M(5, 6, 4) = \Sigma m(0, 1, 2, 3, 7)$



$F(P, Q, R) = \bar{P} + QR$ Choice (A)

24. When we consider two min terms product,
$m_i, m_j = 0$ if $i \neq j$
e.x., $A\bar{B}C \cdot A\bar{B}\bar{C} = 0$ $m_i, m_j \neq 0$ if $i = j$
e.x., $A\bar{B}\bar{C}\ A\bar{B}\bar{C} = A\bar{B}\bar{C}$
If two functions ANDed with min terms, then resultant is common min terms of the two functions.
Example:
If $f_1(a, b, c) = m_1 + m_2 + m_3$
$f_2(a, b, c) = m_3 + m_4$
$f_1 \cdot f_2 = (m_1 + m_2 + m_3)(m_3 + m_4)$
$= m_1 \cdot m_3 + m_1 \cdot m_4 + m_2 \cdot m_3 + m_2 m_4 + m_3 \cdot m_3 + m_3 \cdot m_4$
$= m_3$ (all other terms will be zero)
In the given problem $f(A, B, C) = \overline{X \cdot Y}$
$= \Sigma m(1, 3, 4, 5, 7)$
So $X, Y = \Sigma m(0, 2, 6)$ (the remaining min terms)
$g(A, B, C) = Y \cdot Z = \Sigma m(4, 6)$
X and Y are having (0, 2, 6) min terms in common, i.e., Y will have all these 3 min terms.
Similarly Y and Z have (4, 6) min terms in common,
So Y will have these 2 min terms also.
So $Y = \Sigma m(0, 2, 4, 6)$ Choice (C)

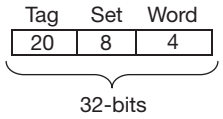
25. From the above solution
$f(A, B, C) = \bar{X}\bar{Y} = \Sigma m(1, 3, 4, 5, 7)$
$X \cdot Y = \Sigma m(0, 2, 6)$
$g(A, B, C) = YZ = \Sigma m(4, 6)$
The min terms common to XY and YZ are
$XY \cdot YZ = XYZ = \Sigma m(6)$
i.e., The output $X = 1$, $Y = 1$, $Z = 1$ only for the min term 6, i.e., $ABC = 110$. Choice (D)

26. Pipeline mean overhead = 5
Let there are k stages.
Given each stage take 1 cycle.
$(k-1)T$ = Pipeline overhead
$\Rightarrow$ $(k-1) \times 1 = 5$
$\Rightarrow$ $k = 6$

$$\text{Speed up} = \frac{\text{nonpipeline execution time}}{\text{pipeline execution time}}$$

$$= \frac{10 \times 6}{(10 + 6 - 1)} = \frac{60}{15} = 4$$ Choice (B)

27.



32-bits
Cache capacity = 16 KB = 2^{14} bytes
Line size = 4 × 32-bit words
= 4 × 4 Bytes = 16 Bytes = 2^4B

$$\text{Number of lines in cache} = \frac{2^{14}}{2^4} = 2^{10}$$

4 × Number of sets = 2^{10}
$\Rightarrow$ Number of sets = 2^8
$\therefore$ Set size = 8
Tag = 32 – (8 + 4) = 20. Choice (C)

28. Main memory has 64-blocks (0 – 63).
Cache has 8 lines (0 – 7).
To place a particular block of main memory in a line of cache, use the following formula:
Cache line number = Block number % number of cache lines.
In cache line number 2, at a time any one of the blocks 2, 10, 18, 26, 34, ..., 58 can be placed. Choice (B)

29. $-30.375 = -11110.011 = -1.1110011 \times 2^4$
Sign = 1
Mantissa = 11100110000000000000000
Exponent = 4
Biased exponent = 127 + 4 = 131 = 10000011
$\therefore$ –30.375 in IEEE standard is

1100	0001	1 111	0011	0000	0 000	0 000	0 000
C	1	F	3	0	0	0	0

$= (C1F30000)_{16}$. Choice (A)

30. First write operation requires 600 ns. (100 ns for bus, 500 ns for store)
During the store operation of first write another request may be given to bus.
So we can start a write operation after every 100 ns.
$\therefore$ Maximum number of stores that can be initiated in one second $= \frac{1}{100 \text{ ns}} = \frac{10^9}{10^2} = 10^7$ Choice (B)

31. Total time taken for one operation = 15 + 15 + 20 = 50 ns

One operation requires 50×10^{-9} sec
In one second, number of operations completed

$$= \frac{1}{50 \times 10^{-9}} = 2 \times 10^{7}.$$ Choice (B)

32. 0.2233×10^{2}
$\underline{+0.6688 \times 10^{1}}$
?

First equate the exponents
$0.6688 \times 10^{1} = 0.06688 \times 10^{2}$
0.22330×10^{2}
$\underline{0.06688 \times 10^{2}}$
$\underline{0.29018 \times 10^{2}}$

The resultant must have four decimal places (by truncation)
$\therefore$ Sum is 0.2901×10^{2}. Choice (A)

33. For high performance use SRAM and for low cost use DRAM. Choice (B)

34. Average instruction time on a pipelined processor
$= 1 \text{ ns} + 0.1 \text{ ns} = 1.1 \text{ ns}$. Choice (C)

35. Average instruction time on a non-pipelined processor
$= 1 + ((3 \times 0.8) + (5 \times 0.1) + (4 \times 0.1)) = 4.3$ ns

$$\text{Speed up} = \frac{4.3}{1.1} = 3.9$$ Choice (B)