Chapter 2

Boolean Algebra

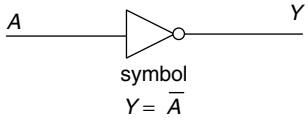
CHAPTER HIGHLIGHTS

- *Logic Gates*
- *Boolean Algebra*
- *AXIOMS and Laws of Boolean Algebra*
- *Properties of Boolean Algebra*
- *Operator Precedence*
- *Boolean Functions, Minterms and Maxterms*
- *Minterm and Maxterm*
- *Minimization of Boolean Functions*
- *Karnaugh Map (K-Map) Method*
- *Implementation of Function by using NAND/ NOR Gates*
- *EX-OR, EX-NOR Gates*
- *Digital IC Families*
- *Basic Gates and its Diode Circuit Diagram*
- *Integrated Injection Logic*
- *Diode Transistor Logic (DTL)*
- *Transistor – Transistor Logic (TTL)*
- *Schottky TTL*
- *MOSFET NAND and NOR Gates*

Logic Gates

Inverter or NOT Gate (7404 IC)

An Inverter performs a basic logic operation called inversion or complementation. The purpose of the inverter is to change one logic level to the opposite level. In terms of digital circuits, it converts 1 to 0 and 0 to 1.



symbol

$Y = \overline{A}$

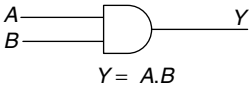
Truth Table

Input	Output
A	*Y*
0	1
1	0

AND Gate (Logical Multiplier) (7408 IC)

The AND gate performs logical multiplication more commonly known as AND function. The AND gate is composed of two or more inputs and a single output.

2 i/p AND Gate



$Y = A.B$

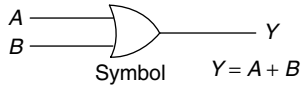
Truth Table

Input		Output
A	*B*	*Y*
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate (Logical Adder 7432 IC)

The OR gate performs logical addition commonly known as OR function.

2 input OR Gate



Symbol $Y = A + B$

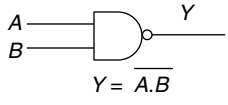
Truth Table

Input		Output
A	*B*	*Y*
0	0	0
0	1	1
1	0	1
1	1	1

NAND Gate (7400 IC)

The NAND gate function is basically AND + NOT function.

2 input NAND Gate



$Y = \overline{A.B}$

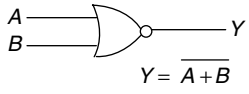
Truth Table

Input			Output
A	*B*	*A.B*	$\overline{A.B}$ (*Y*)
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

NOR Gate (7402 IC)

The NOR gate is basically OR + NOT function.

2 input NOR Gate



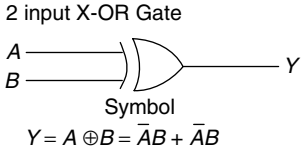
Truth Table

Input			Output
A	B	A + B	$\overline{A+B}$ (Y)
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Exclusive OR Gate X-OR (7486 IC)

X-OR is a gate in which unequal inputs create a high logic-level output and if both inputs are equal, the output will be low. Other name for EX-OR gate is nonequivalent gate.

2 input X-OR Gate



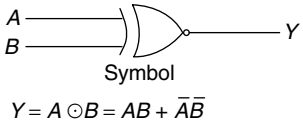
Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Exclusive NOR Gate (X-NOR)

X-NOR is a gate in which equal inputs create a high logic-level output and if both inputs are unequal, the output will be low. Other name for EX-NOR gate is equivalent gate.

2 input X-NOR Gate



Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

EXNOR gate is complement of EXOR gate.

EX-NOR gate is the complement of EX-OR gate.

Boolean Algebra

Boolean algebra is a system of mathematical logic. It is an algebraic system consisting of the set of elements (0,1), two binary operators OR and AND, and one unary operator NOT. The Boolean algebra is governed by certain well-developed rules and laws.

AXIOMS and Laws of Boolean Algebra

Axioms

1. **AND operation**
   (1) $0 \cdot 0 = 0$
   (2) $0 \cdot 1 = 0$
   (3) $1 \cdot 0 = 0$
   (4) $1 \cdot 1 = 1$
2. **OR operation**
   (5) $0 + 0 = 0$
   (6) $0 + 1 = 1$
   (7) $1 + 0 = 1$
   (8) $1 + 1 = 1$
3. **NOT operation**
   (9) $\overline{1} = 0$
   (10) $\overline{0} = 1$

Laws

1. **Complementation law:**
   (a) $\overline{0} = 1$
   (b) $\overline{1} = 0$
   (c) If $A = 0$, then $\overline{A} = 1$
   (d) If $A = 1$, then $\overline{A} = 0$
   (e) $\overline{\overline{A}} = A$
2. **AND laws**
   (a) $A \cdot 0 = 0$ (NULL law)
   (b) $A \cdot 1 = A$ (Identity law)
   (c) $A \cdot A = A$
   (d) $A \cdot \overline{A} = 0$
3. **OR laws**
   (a) $A + 0 = A$ (NULL law)
   (b) $A + 1 = 1$ (Identity law)
   (c) $A + A = A$
   (d) $A + \overline{A} = 1$
4. **Commutative laws**
   (a) $A + B = B + A$
   (b) $A.B = B.A$
5. **Associative laws**
   (a) $(A + B) + C = A + (B + C)$
   (b) $(A.B)\ C = A(B.C)$
6. **Distributive laws**
   (a) $A(B + C) = AB + AC$
   (b) $A + BC = (A + B)\ (A + C)$
7. **Redundant literal rule (RLR):-**
   (a) $A + \overline{A}B = A + B$
   (b) $A\ (\overline{A} + B) = AB$
8. **Idempotent laws**
   (a) $A \cdot A = A$
   (b) $A + A = A$
9. **Absorption laws**
   (a) $A + A \cdot B = A$
   (b) $A\ (A + B) = A$

Theorems

1. **Consensus theorem:**
   Theorem 1:
   $AB + \overline{A}C + BC = AB + \overline{A}C$
   Proof:
   $$\begin{aligned} \text{LHS} &= AB + \overline{A}C + BC \\ &= AB + \overline{A}C + BC\,(A + \overline{A})] \\ &= AB + \overline{A}C + BC\,A + BC\overline{A} \\ &= AB\,(1 + C) + \overline{A}C\,(1 + B) \\ &= AB\,(1) + \overline{A}C\ \ (1) \\ &= AB + \overline{A}C \\ &= \text{RHS}. \end{aligned}$$

Theorem 2:

$(A+B)\ (\bar{A}+C)\ (B+C)=(A+B)\ (\bar{A}+C)$

LHS $= (A+B)\ (\bar{A}+C)\ (B+C)$

$= (A\bar{A}+AC+B\bar{A}+BC)\ (B+C)$

$= (AC+BC+\bar{A}B)\ (B+C)$

$= ABC+BC+\bar{A}B+AC+BC+\bar{A}BC$

$= AC+BC+\bar{A}B$

RHS $= (A+B)\ (\bar{A}+C)$

$= A\bar{A}+AC+BC+\bar{A}B$

$= AC+BC+\bar{A}B$ = LHS.

2. **Transposition theorem:**

$AB+\bar{A}C = (A+C)\ (\bar{A}+B)$

RHS $= (A+C)\ (\bar{A}+B)$

$= A\bar{A}+C\bar{A}+AB+CB$

$= 0+\bar{A}C+AB+BC$

$= \bar{A}C+AB+BC\ (A+\bar{A})$

$= AB+ABC+\bar{A}C+\bar{A}BC$

$= AB+\bar{A}C$ = LHS

3. **DeMorgan's theorem:**

Law 1: $\overline{A+B} = \bar{A}.\bar{B}$

This law states that the complement of a sum of variable is equal to the product of their individual complements.

Law 2: $\overline{AB} = \bar{A}+\bar{B}$

This law states that the complement of the product of variables is equal to the sum of their individual complement.

Solved Examples

Example 1

Simplify the Boolean function $Y = A(A+\bar{B})$

Solution

$Y = A.A+A.\bar{B}$

$Y = A+A\bar{B}$

$= A(1+\bar{B})$ d

$= A$

Example 2

Simplify the Boolean function $Y = A+\bar{A}B$

Solution

$Y = A.(B+1)+\bar{A}.B$

$= A.B+A+\bar{A}B$

$= B\left(A+\bar{A}\right)+A = A+B$

Example 3

Simplify the Boolean function $Y = A(A+B)+B(\bar{A}+B)$

Solution

$Y = A.A+A.B+B.\bar{A}+B.B$

$= A+B(A+\bar{A})+B = A+B.1+B$

$= A+B+B = A+B$

Example 4

Simplify the Boolean function

$Y = \bar{A}\ \bar{B}\ \bar{C}+\bar{A}\ B\ \bar{C}+A\ B\ \bar{C}+A\ \bar{B}\ \bar{C}$

Solution

$Y = \bar{A}\bar{C}(\bar{B}+B)+A\bar{C}(B+\bar{B})$

$= \bar{A}\bar{C}+A\bar{C} = \bar{C}(\bar{A}+A) = \bar{C}$

Example 5

Simplify the Boolean function

$Y = \overline{\bar{A}BC+\bar{A}B\bar{C}+\bar{A}\bar{B}C}$

Solution

$Y = \overline{\bar{A}C(B+\bar{B})+\bar{A}B\bar{C}} = \overline{\bar{A}C+\bar{A}B\bar{C}}$

$= \overline{\bar{A}(C+B\bar{C})} = \overline{\bar{A}(C+B)} = A+\bar{C}\bar{B}$

Example 6

Simplify the Boolean function

Solution

$Y = AB+C\bar{B}+CA+ABD$

$Y = AB(1+D)+C\bar{B}+CA$

$= AB+C\bar{B}+CA = AB+C\bar{B}$

Properties of Boolean Algebra

With n-variables, maximum possible distinct functions $= 2^{2^n}$.

Duality

Consider the distributive law

1. $x\ (y+z) = xy+xz$
2. $x+yz = (x+y)\ (x+z)$

The second expression can be obtained from the Law 1, if the binary operators and the identity elements are interchanged. This important property of Boolean algebra is called the duality principle.

The dual of an algebraic expression can be written by interchanging OR and AND operators, that is, 1's by 0, and 0's by 1's.

Example 7

$$x + x^1 = 1 \xleftrightarrow{Dual} x \,.\, x^1 = 0$$

Solution

$$xy + xy^1 = x \xleftrightarrow{Dual} (x + y)\,(x + y^1) = x$$

$$x + x^1y = x + y \xleftrightarrow{Dual} x\,(x^1 + y) = xy$$

Example 8

Find the dual of $F = xy + xz + yz$ is?

Solution

Dual of $F = (x + y)\,(x + z)\,(y + z)$

$= (x + xz + xy + yz)\,(y + z) = xy + yz + xz$

Therefore, dual of $xy + xz + yz$ is same as the function itself. For N variables, maximum possible self-dual functions = $2^{2^{n-1}} = 2^{(2^n/2)}$

Example 9

Which of the following statement/s is/are true

S_1: The dual of NAND function is NOR

S_2: The dual of XOR function is XNOR

(A) S_1 and S_2 are true

(B) S_1 is true

(C) S_2 is true

(D) None of these

Solution

NAND = $(xy)^1 = x^1 + y^1$

Dual of NAND = $(x + y)^1 = x^1\,y^1$

XOR = $xy^1 + x^1y$

Dual of XOR = $(x + y^1)\,(x^1 + y) = xy + x^1y^1$ = XNOR

Both S_1 and S_2 are true.

Operator Precedence

The operator precedence for evaluating Boolean expression is

1. Parentheses
2. NOT
3. AND
4. OR

Therefore, the expression inside the parentheses must be evaluated before all the operations. The next operation to be performed is the complement, and then, follows AND; finally, the OR.

Complement of Function

The complement of a function F is F^1 is obtained from an interchange of 0's for 1's and 1's for 0's in the value of F. The complements of a functions may be derived algebraically through DeMorgan's theorems.

$$(x_1 \,.\, x_2 \,.\, x_3 \ldots\ldots x_n)^1 = x^1{}_1 + x^1{}_2 + x_3{}^1 \ldots\ldots + x_n{}^1$$

$$(x_1 + x_2 + x_3 + \ldots\ldots + x_n)^1 = x^1{}_1 \,.\, x_2{}^1 \,.\, x^1{}_3 \,.\, x^1{}_4 \ldots\ldots\ldots\ldots x_n{}^1$$

Example 10

Find the complement of function $F = a(b^1c + bc^1)$ is?

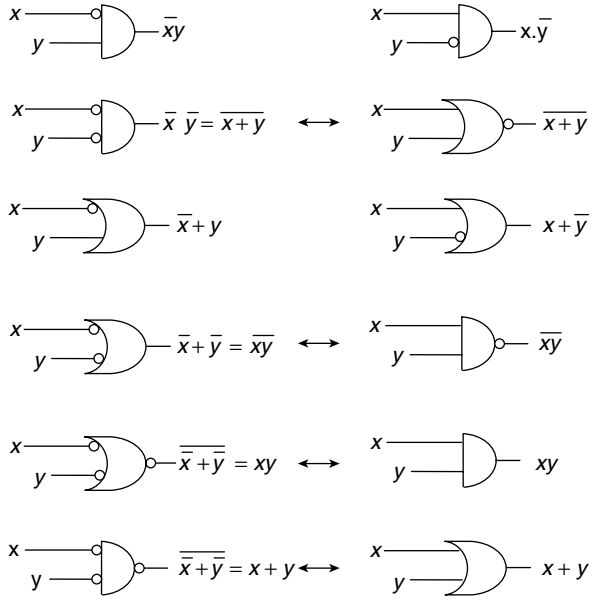
Solution

$$(F)^1 = [a(b^1c + bc^1)]^1 = a^1 + (b^1c + bc^1)^1$$

$$= a^1 + (b^1c)^1 \,.\, (bc^1)^1 = a^1 + (b + c)^1\,(b^1 + c)$$

$$F^1 = a^1 + bc + b^1c^1$$

Gates with Inverted Inputs

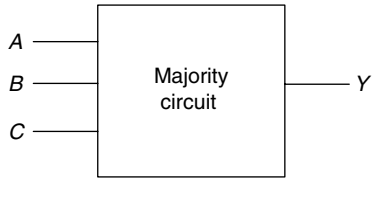


Boolean Functions, Minterms, and Maxterms

The starting point for designing most logic circuits is the truth table, which can be derived from the statement of problem. The truth table is then converted into a Boolean expression, and finally, the assembly of logic gates accordingly.

Let us consider the example of majority circuit. This circuit takes three inputs (A, B, C) and have one output (Y), which will give the majority of the inputs. If A, B, and C are having more number of zeros, $Y = 0$; else, if A, B, and C are having more number of 1's, $Y = 1$.

Therefore, from the statements, we can derive the truth table as follows:



As we are using three Boolean variables A, B, and C, total number of combinations in truth table are $2^3 = 8$.

Similarly, for n variables, the truth table will have total of 2^n combinations for a Boolean function.

S.no	Input			Output	
	A	B	C	Y	
1	0	0	0	0	→ $Y = 0$, if inputs are having more 0's
2	0	0	1	0	
3	0	1	0	0	
4	0	1	1	1	→ $Y = 1$, if inputs are having more 1's
5	1	0	0	0	
6	1	0	1	1	
7	1	1	0	1	
8	1	1	1	1	

For some combinations, output $Y = 1$, and for others, $Y = 0$. The input combinations for which output $Y = 1$ are called as minterms.

Similarly, the input combinations for which output $Y = 0$ are called as maxterms. Minterms are expressed as product terms. Similarly, maxterms are expressed as sum terms.

The output $Y = 1$, only in rows 4, 6, 7, 8. Therefore, the minterms combinations are 011, 101, 110, 111 in Boolean algebra. Input '1' will be written as A, B, and C and input '0' will be written as $\overline{A}\ \overline{B}, \overline{C}$ in complement form, we express these minterms as product terms $\overline{A}\,BC$, $A\,\overline{B}\,C$, $A\,B\,\overline{C}$, $ABCx$.

To express Y as Boolean expression, we can write it as sum of the minterms.

$$Y = \overline{A}\,BC + A\,\overline{B}\,C + A\,B\overline{C} + A\,B\,C$$

We know that AND operation is a product while OR is sum. Therefore, the abovementioned equation is a sum of the products (SOP) or minterms expression.

The other way of expressing Y is $Y = \Sigma m\ (3, 5, 6, 7)$.

$$Y = m_3 + m_5 + m_6 + m_7.$$

The minterm numbers are the decimal equivalent of input binary combinations.

Similar to SOP, we can have the product of sums (POS) Boolean expression.

The output $Y = 0$ for the input combinations 000, 001, 010, 100. For maxterms, input '1' will be indicated as $\overline{A}, \overline{B}, \overline{C}$ in complement form, input '0' will be indicated as A, B, C, and maxterms are expressed as sum terms.

$$A + B + C,\ A + B + \overline{C},\ A + \overline{B} + C,\ \overline{A} + B + C$$

Any function can be expressed as product of maxterms. Therefore,

$$Y = (A + B + C)(A + B + \overline{C})(A + \overline{B} + C)(\overline{A} + B + C)$$

The above mentioned equation is a product of sum expression (POS) or maxterms expression.

In other way, $Y = \pi M\ (0, 1, 2, 4) = M_0 \,.\, M_1 \,.\, M_2 \,.\, M_4$

The maxterm numbers are decimal equivalents of corresponding input binary combinations.

Minterm and Maxterm

All the Boolean expressions can be expressed in a standard sum of product (SOP) form or in a standard product of sum (POS) form.

1. A standard SOP form is one in which a number of product terms, each contains all the variables of the function either in complement or non-complement form are summed together.
2. A standard POS form is one in which a number of sum terms, each one of which contain all the variables of the function either in complemented or non-complemented form are multiplied together.
3. Each of the product term in standard SOP form is called a minterm.
4. Each of the sum term in the standard POS form is called a maxterm.

Conversion from Minterms To Maxterms Representation

$$Y = \overline{A}\,BC + A\,\overline{B}\,C + A\,B\overline{C} + A\,B\,C$$

$$Y^1 = (\overline{A}\,BC + A\,\overline{B}\,C + A\,B\overline{C} + A\,B\,C)^1$$

$$= (\overline{A}\,B\,C)^1\ (A\,\overline{B}\,C)^1\,(A\,B\,\overline{C})^1\,(A\,B\,C)^1$$

$$(Y^1)^1 = \left[\left(A + \overline{B} + \overline{C}\right)\left(\overline{A} + B + \overline{C}\right)\left(\overline{A} + \overline{B} + C\right)\left(\overline{A} + \overline{B} + \overline{C}\right)\right]^1$$

$$= [\pi(3, 5, 6, 7)]^1 = \pi(0, 1, 2, 4)$$

$$Y = \left(A + B + C\right)\left(A + B + \overline{C}\right)\left(A + \overline{B} + C\right)\left(\overline{A} + B + C\right)$$

(or)

$$Y = \Sigma(3, 5, 6, 7) = \pi(0, 1, 2, 4)$$

Conversion from Normal SOP/POS form to Canonical SOP/POS

Let us consider $f(A, B, C) = A + BC + \overline{A}C$.

The above mentioned function is in normal (minimized) SOP form to convert this function to standard SOP or canonical SOP form, which includes missing variable in each and every term, to make it complete.

From the expression, the first term is A and missing literals are B, C.

Consider AXX, and therefore, the possible combinations are $\overline{A}\,BC$, $A\,\overline{B}\,C$, $A\,B\,\overline{C}$, ABC

or we can write $A = A\left(B + \overline{B}\right)\left(C + \overline{C}\right) = ABC + AB\overline{C} + A\overline{B}C + A\overline{B}\,\overline{C}$

From the expression, the second term is BC and missing literal is A.

Consider $XBC \Rightarrow$ Therefore, the possible combinations are ABC, $\overline{A}\,B\,C$ or we can write $BC = (A + \overline{A})\,BC$

$$= ABC + \overline{A}\,B\,C$$

From the expression, the third term is $\overline{A}\,C$ = missing literal is B.

Consider $\overline{A}\,XC \rightarrow$ so possible combinations are $\overline{A}\,B\,C$, $\overline{A}$, $\overline{B}\,C$

or we can write $\overline{A}\,C = \overline{A}\left(B + \overline{B}\right)C$

$$= \overline{A}\,BC + \overline{A}\,\overline{B}\,C$$

Now,

$$f(A, B, C) = ABC + AB\overline{C} + A\overline{B}C + \overline{A}BC + \overline{A}\,\overline{B}\,C$$

After removing the redundant terms, let us consider $f(A, B, C) = (A+B)(\overline{A}+C)$

To convert this expression to canonical form or standard POS form, we can write

$$f(A, B, C) = (A+B+C.\,\overline{C})(\overline{A}+B.\,\overline{B}+C)$$

Here, C variables are absent from the first term and B from the second term. Therefore, add $C.\overline{C}$ $(=0)$ to first and $B.\overline{B}$ to second; further, by using distributive law, we arrive at the result.

$$f(A,B,C) = (A+B+C)(A+B+\overline{C})(\overline{A}+B+C)(\overline{A}+\overline{B}+C)$$

Minimization of Boolean Functions

Simplification Procedure

1. Obtain truth table and write output in canonical form or standard form.
2. Generate K-map.
3. Determine prime implicants.
4. Find minimal set of prime implicants.

Karnaugh Map (K-map) Method

1. Karnaugh map method is a systematic method of simplifying the Boolean expression.
2. K-map is a chart or a graph composed of an arrangement of adjacent cell, each representing a particular combination of variable in sum or product form (i.e., minterm or maxterm).

Two-variable K-map

x	y	F
0	0	m_0
0	1	m_1
1	0	m_2
1	1	m_3

m_0	m_1
m_2	m_3

x \ y	0	1
0	$x'y'$	$x'y'$
1	xy'	xy

Three-variable K-map

A three-variable map will have eight minterms (for three variables $2^3 = 8$) represented by eight squares.

x	y	z	F
0	0	0	m_0
0	0	1	m_1
0	1	0	m_2
0	1	1	m_3
1	0	0	m_4
1	0	1	m_5
1	1	0	m_6
1	1	1	m_7

m_0	m_1	m_3	m_2
m_4	m_5	m_7	m_6

x \ yz	00	01	11	10
0	x′y′z	x′y′z	x′yz	x′yz′
1	xy′z′	xy′z	xyz	xyz′

Four-variable K-maps

The K-map for four variables is shown here, and 16 minterms are assigned to 16 squares.

wx \ yz	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

1. The map is considered to lie on a surface with the top and bottom edges as well as the right and left edge touching each other to form adjacent squares.
2. One square → a minterm of 4 literals
3. Two adjacent square → a term of 3 literals
4. Four adjacent square → a term of 2 literals
5. Eight adjacent square → a term of 1 literal
6. 16 adjacent square → The constant 1

Don't Care Combinations

It can often occurs that for certain input combinations, the value of the output is unspecified either because the input combinations are invalid or because the precise value of the output is of no consequence. The combination for which the values of the expression are not specified are called Don't care combinations. During the process of design using an SOP K-map, each don't care is treated as 1 if it is helpful in map reduction, otherwise it is treated as 0 and left alone.

During the process of design using a POS K-map, each Don't care is treated as 0 if it is useful in map reduction, otherwise it is treated as 1 and left alone.

Example 11

Find the minimal expression

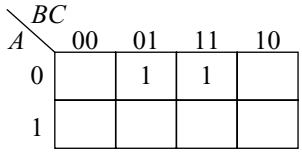
$$\Sigma m\,(1, 5, 6, 12, 13, 14) + d\,(2, 4)$$

Solution

AB \ CD	00	01	11	10
00		1		X
01	X	1		1
11	1	1		1
10				

Therefore, $F = B\overline{C} + B\overline{D} + \overline{A}\,\overline{C}\,D$

Pairs, Quads, and Octets

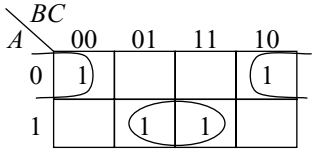


The map contains a pair of 1's those are horizontally adjacent. Those cells represent

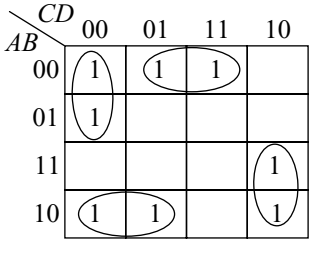
$$\overline{A}\ \overline{B}C\ ,\ \overline{A}BC.$$

For these two minterms, there is change in the form of variable B. By combining these two cells, we can form a pair, which is equal to $\overline{A}\ \overline{B}C\ +\ \overline{A}\ BC = \overline{A}C(\overline{B}+B) = \overline{A}C$

If more than one pair exists on K-map, OR the simplified products to get the Boolean function.



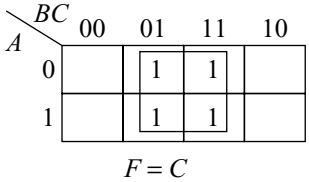
$$F = \overline{A}\ \overline{C} + AC$$



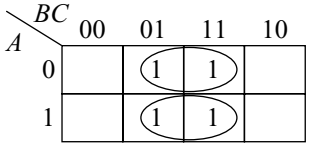
$$F = \overline{A}\,\overline{C}\ \overline{D} + \overline{A}\ \overline{B}\,D + A\overline{B}\ \overline{C} + AC\overline{D}$$

Therefore, pair eliminates one variable by minimization.

Quad: Quad is a group of four 1's those are horizontally or vertically adjacent.

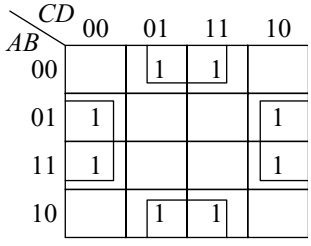


$$F = C$$



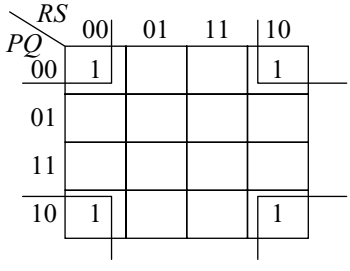
$$F = \overline{A}C + AC = \left(\overline{A} + A\right)C = C$$

Further, by considering two pairs, it will be simplified to C. Quad eliminates two variables from the function.



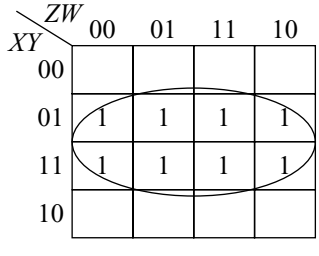
$$F = B\overline{D} + \overline{B}Dp$$

Corner minterms can form a quad



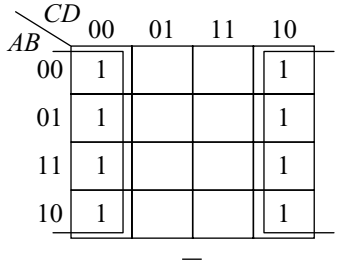
$$F = \overline{Q}\ \overline{S}$$

Octet: The group of eight cells will form one octet.



$$F = Y$$

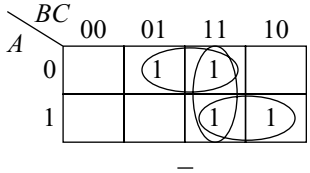
Other variables X, Z, and W change their form in octet. Octet can eliminate three variables and their complements.



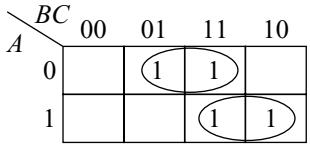
$$F = \overline{D}$$

Other variables A, B, and C are vanished.

Eliminating Redundant Groups

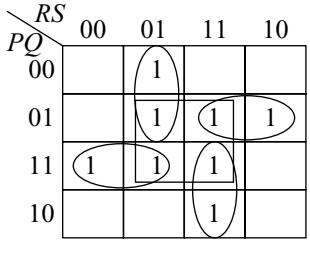


$$\rightarrow AB + \overline{A}C + BC$$

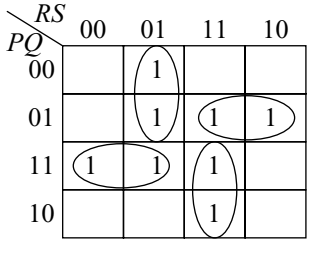


$\rightarrow AB + \overline{A}C$

Here, BC is redundant pair, which covers already covered minterms of AB, $\overline{A}C$



→ This K-map gives four pairs and one quad.

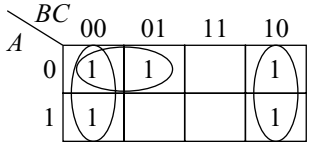


→ However, only four pairs are enough to cover all the minterms, and quad is not necessary.

→ $\overline{P}\ \overline{R}S + \overline{P}\ Q\ R + P\ Q\ \overline{R} + P\ RS$ is a minimized function.

Prime Implicant

The group of adjacent minterms is called a prime implicant, i.e., all possible pairs, quads, octets, etc.



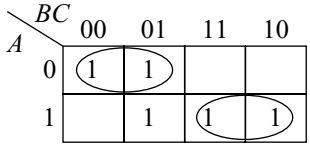
Prime implicants are

$\overline{B}\ \overline{C}$, $B\ \overline{C}$, $\overline{C}$, $\overline{A}\ \overline{B}$

Minimized function is $\overline{C} + \overline{A}\ \overline{B}$]

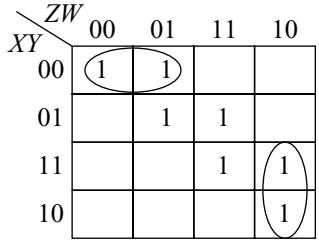
Essential Prime Implicant

The prime implicant that contains at least one minterm, which cannot be covered by any other prime implicant, is called essential prime implicant.



Minterms 0 and 6 can be grouped with only one pair each. The total possible prime implicants are $\overline{A}\ \overline{B}$, $\overline{B}C$, AC, AB; however, minterm 0 and 6 can be covered with $\overline{A}\ \overline{B}$, AB.

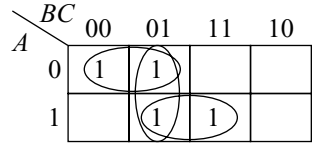
Therefore, we call them as essential prime implicants. Minterm 5 can be paired with any of minterm 1 or 7.



The essential prime Implicants are $XZ\overline{W}$, $\overline{X}\ \overline{Y}\ \overline{Z}$.

Redundant Prime Implicant

The prime implicant whose minterms are already covered by at least one minterm is called redundant prime implicants.



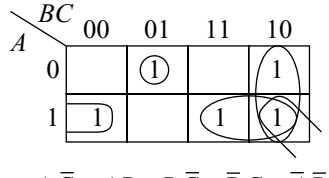
Here, prime Implicants are $\overline{A}\ \overline{B}$, AC, $\overline{B}\ C$. But, $\overline{B}\ Cp$ is already covered by other minterms. Therefore, $\overline{B}\ C$ is redundant prime implicant.

Example 12

Find the minimal expression for Σm (1, 2, 4, 6, 7) and implement it using basic gates.

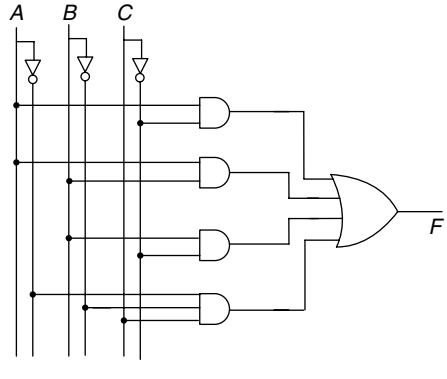
Solution

K-map is



$$F = A\overline{C} + AB + B\overline{C} + \overline{B}C + \overline{A}\,\overline{B}C$$

Logic diagram



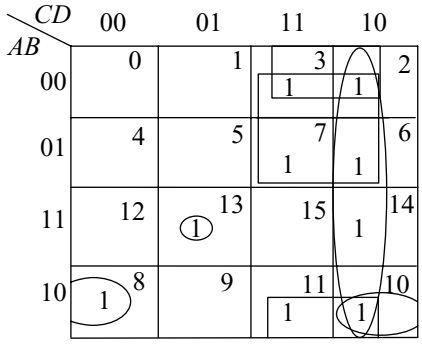
Example 13

Find the minimal expression for

$$\Sigma m\ (2,3,6,7,8,10,11,13,14)$$

Solution

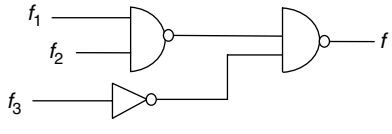
K-map is



Therefore, $F(A,B,C,D) = A\,B\,\bar{C}\,D + A\,\bar{B}\,\bar{D} + \bar{A}\,C + \bar{B}\,C + C\,\bar{D}$

Example 14

Three Boolean functions are defined as $f_1 = \Sigma m\ (0, 1, 3, 5, 6)$, $f_2 = \Sigma m\ (4, 6, 7)$, and $f_3 = \Sigma m(1, 4, 5, 7)$. Find f.



Solution

When two Boolean functions are ANDed, the resultant will contain the common minterms of both of the functions (like intersection of minterms). If two Boolean functions are ORed, then resultant is the combination of all the minterms of the functions (like union of minterms).

Here, $$f = \overline{\overline{f_1\ f_2}\ .\ \overline{f_3}} = f_1 f_2 + f_3$$

Here, $f_1 f_2$ = common minterms in f_1 and $f_2 = \Sigma m(6)$.

$f_1 f_2 + f_3$ = combination of minterms of $f_1 f_2$ and f_3.

$= \Sigma(1, 4, 5, 6, 7)$

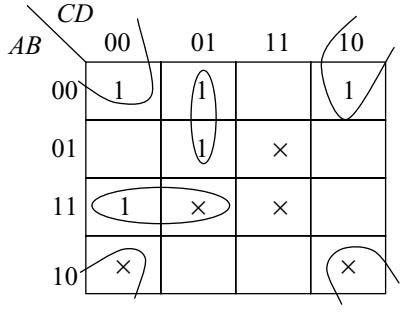
Example 15

What is the literal count for the minimized SOP and minimized POS form for the function?

$f(A, B, C, D) = \Sigma m(0, 1, 2, 5, 12) + \phi d(7, 8, 10, 13, 15)$

Solution

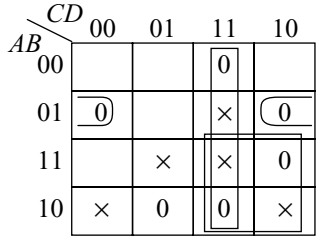
$f(A, B, C, D) = \Sigma m(0, 1, 2, 5, 12) + \phi(7, 8, 10, 13, 15)$



f = 1 quad + 2 pairs

Literal count = $1 \times 2 + 2 \times 3 = 8$

$f(A, B, C, D) = \pi M(3, 4, 6, 9, 11, 14) + \phi(7, 8, 10, 13, 15)$

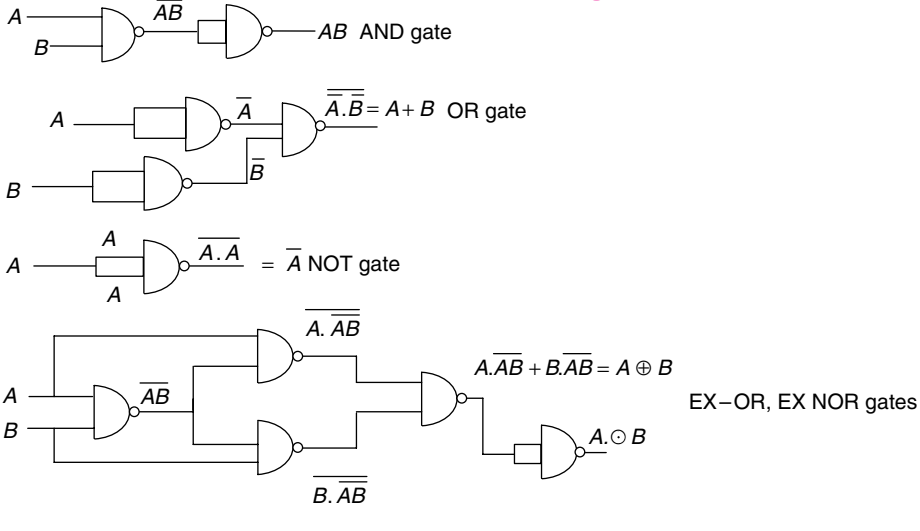


f will consist of 3 quads + 1 pair = $3 \times 2 + 1 \times 3 = 6 + 3 = 9$

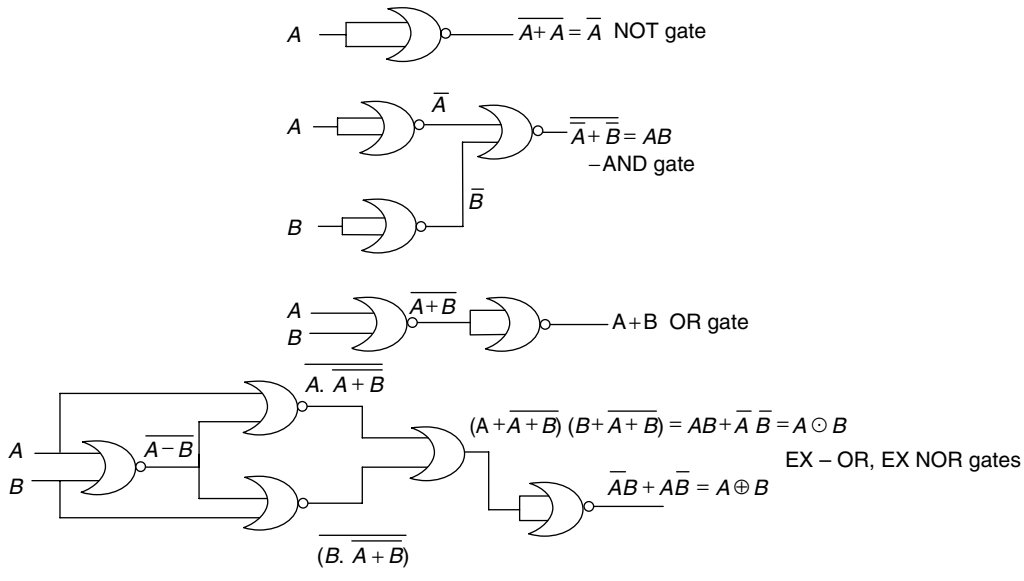
Implementation of Function by Using NAND/NOR Gates

NAND or NOR gates are called as universal gates because any function can be implemented by using only NAND gates or only using NOR gates.

Implementation of Basic Gates by Using NAND gates

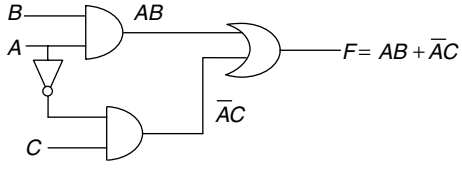


Implementation of Basic Gates by Using NOR Gates

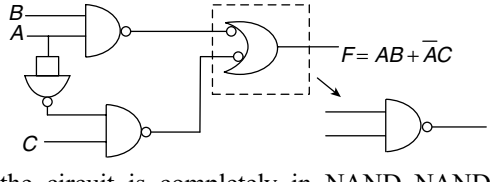


Any functions, which is in the SOP form, can be implemented by using AND–OR gates, which is also equivalent to NAND–NAND gates.

$$F = AB + \overline{A}C$$



By considering bubble at AND gate output and OR gate input and by changing NOT gates to NAND gates, the circuit becomes



Now, the circuit is completely in NAND–NAND form. Therefore, the functions expressed in SOP form can be implemented by using AND–OR or NAND–NAND gates.

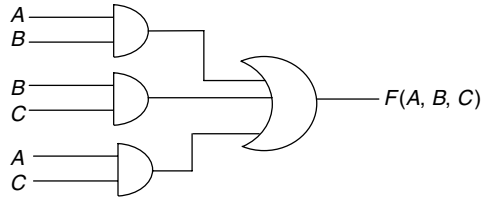
Any function in POS form can be implemented by using OR–AND gates, which is similar to NOR–NOR gate.

Example 16

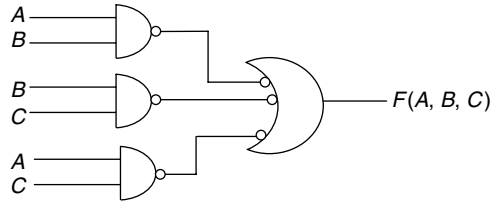
How many number of NAND gates are required to implement $F(A, B, C) = AB + BC + AC$?

(A) 3 (B) 4 (C) 5 (D) 6

Solution



By considering bubbles at output of AND gate and input of OR gate, we get



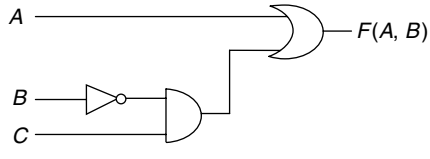
Therefore, four NAND gates are required.

Example 17

Find the number of NAND gates required for the implementation of $f(A, B) = A + \overline{B}C$ is

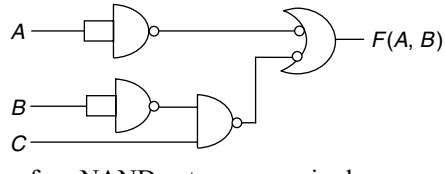
(A) 3 (B) 4 (C) 5 (D) 6

Solution



To convert all gates into NAND gates, place bubble output of AND and inputs of OR gates.

Now, the circuit can be drawn as



Therefore, four NAND gates are required.

Example 18

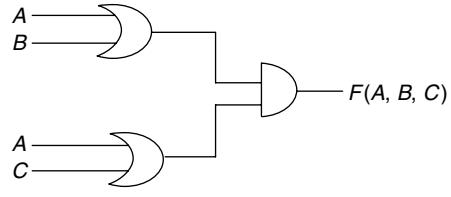
How many number of NOR gates are required to implement $f = A + BC$?

(A) 3 (B) 4 (C) 5 (D) 2

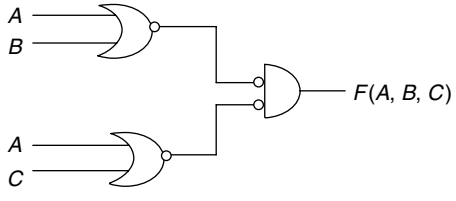
Solution

$A + BC$ is in SOP form.

To implement this function by using NOR gates, we can write $f(A, B, C) = A + BC = (A + B)(A + C)$, which is in the form of POS



By including bubbles at the output of OR gate and input of AND gate. The circuit becomes



Now, the circuit consists of all 3 NOR gates.

Example 19

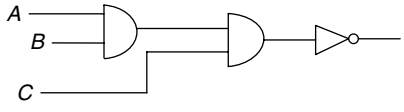
How many number of 2 input NAND/NOR gates are required to implement 3 input NAND/NOR gates, respectively?

(A) 2, 2 (B) 2, 3 (C) 3, 2 (D) 3, 3

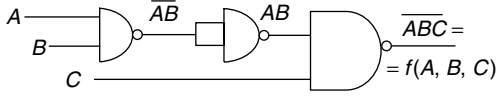
Solution

$$F(A, B, C) = \overline{A\,B\,C} = \overline{A\,B} + \overline{C}$$

1. Implement abovementioned function by using two input gates.

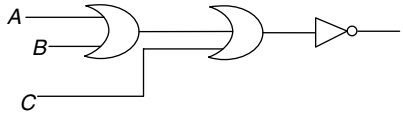


Now, convert each gate to NAND gate.

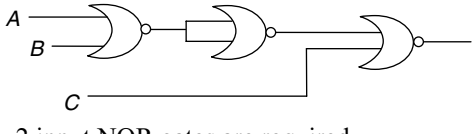


3, 2 input NAND gates are required

2. Implement $G(A, B, C) = \overline{A + B + C}$ by using two input gates.



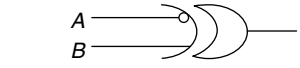
Now, convert each gate to NOR gate.



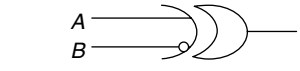
3, 2 input NOR gates are required.

Ex-or and Ex-nor Gates

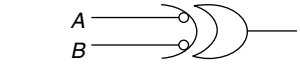
Inverted inputs for EX-OR and EX-NOR gates.



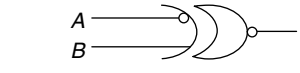
$$\overline{A} \oplus B = \overline{\overline{A}}B + \overline{A}\,\overline{B} = AB + \overline{A}\,\overline{B} = A \odot B$$



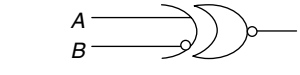
$$A \oplus \overline{B} = A\,\overline{\overline{B}} + \overline{A}\,\overline{B} = AB + \overline{A}\,\overline{B} = A \odot B$$



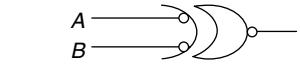
$$\overline{A} \oplus \overline{B} = \overline{A\overline{B}} + \overline{\overline{A}B} = \overline{A}B + A\overline{B} = A \oplus B$$



$$\overline{A} \odot B = \overline{A}B + \overline{\overline{A}\,\overline{B}} = \overline{A}B + A\overline{B} = A \oplus B$$



$$A \odot \overline{B} = A\overline{B} + \overline{A}\,\overline{\overline{B}} = A\overline{B} + \overline{A}B = A \oplus B$$

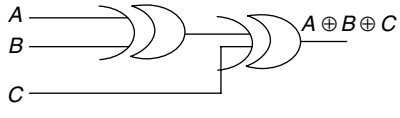


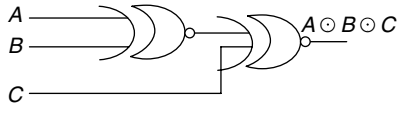
$$\overline{A} \odot \overline{B} = \overline{A}\,\overline{B} + \overline{\overline{A}}\,\overline{\overline{B}} = \overline{A}\,\overline{B} + AB = A \odot B$$

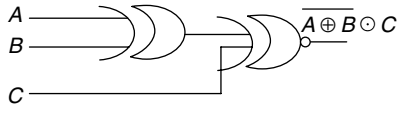
From the above mentioned discussions, we can conclude that inverted input EX-OR gate is EX-NOR gate.

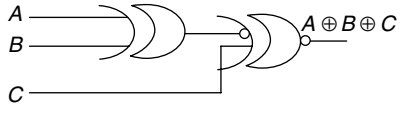
Similarly, inverted input EX-NOR gate is EX-OR gate. If both inputs are inverted, the EX-OR/EX-NOR will remain same.

Consider a 3-input XOR gate by using 2-input XOR gate.



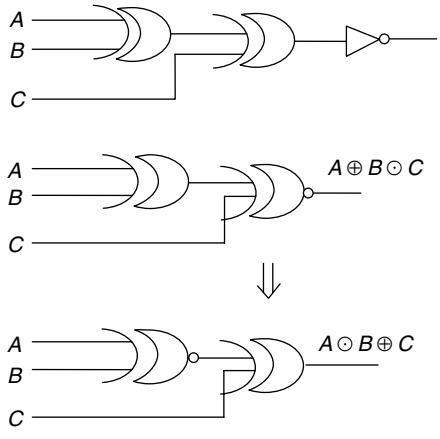






Therefore, we can conclude that $A \oplus B \oplus C = A \odot B \odot C$

$$\overline{A \oplus B \oplus C} = \overline{A \odot B \odot C}$$



$$\overline{A \oplus B \oplus C} = \overline{A \odot B \odot C} = A \oplus B \odot C = A \odot B \oplus C$$

$$A \oplus B \oplus C \oplus D = A \oplus B \odot C \odot D = A \odot B \odot C \oplus D$$

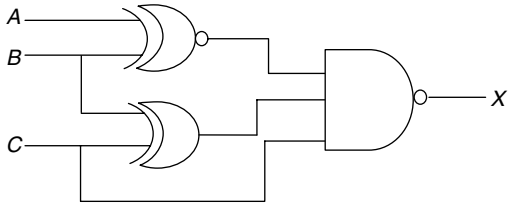
$$= A \odot B \oplus C \odot D$$

$$A \odot B \odot C \odot D = \overline{A \oplus B \oplus C \oplus D}$$

$$A \odot B \odot C \odot D = A \oplus B \oplus C \odot D = A \oplus B \odot C \oplus D$$

Example 20

For the logic circuit shown in the figure, find the required input condition (A, B, C) to make the output $X = 0$ is?



(A) 1, 1, 1 (B) 1, 0, 1 (C) 0, 1, 1 (D) 0, 0, 1

Solution

To get output $X = 0$, all inputs to the NAND gate should be 1, and therefore, $C = 1$.

When $C = 1$, the output of XOR gate $B \oplus C = 1$ only when $B = 0$

If $B = 0$, the output of XNOR gate $A \odot B = 1$

only when $A = 0$

Therefore, $X = 1$, only when $(A, B, C) = (0, 0, 1)$.

Example 21

Find the minimized expression of

$$\left(A + \overline{B}\right)\left(A\,\overline{B} + AC\right)\left(\overline{A}\,\overline{C} + \overline{B}\right) \text{ is}$$

Solution

$$\left(A + \overline{B}\right)\left(A\,\overline{B} + AC\right)\left(\overline{A}\,\overline{C} + \overline{B}\right)$$

$$= \left(A + \overline{B}\right)\left(A\,\overline{B}.\overline{A}\,\overline{C} + A\overline{B}.\overline{B} + AC.\overline{A}\,\overline{C} + AC.\overline{B}\right)$$

$$= \left(A + \overline{B}\right)\left(A\overline{B} + A\overline{B}\,C\right) = \left(A + \overline{B}\right) A\,\overline{B}\,(1 + C)$$

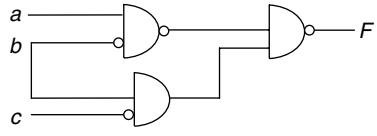
$$= A\overline{B} + A\overline{B} = A\overline{B}$$

Example 22

The Boolean function F is independent of

(A) a (B) b

(C) c (D) none of these

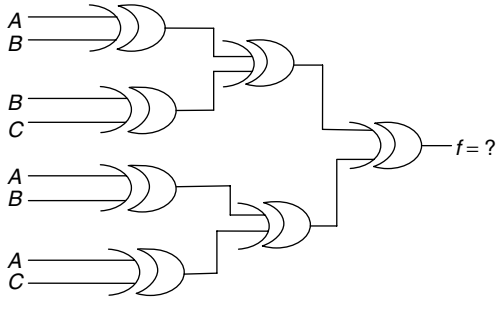


Solution

$$F = \overline{\overline{a\ b}.\overline{b}\ c} = ab + \overline{\overline{b}\ c} = ab + b + \overline{c}$$

$= b + \overline{c}$ is independent of 'a'

Example 23



Solution

$$f = \{A \oplus B \oplus B \oplus C\} \oplus \{A \oplus C \oplus B \oplus A\}$$

$$= \{A \oplus 0 \oplus C\} \oplus \{0 \oplus C \oplus B\}$$

$$= A \oplus C \oplus C \oplus B = A \oplus O \oplus B = A \oplus B$$

Digital IC Families

Digital logic gates will be implemented by using digital ICs. Logic family is the way to describe the internal circuitry of the IC. Each logic family is characterized by a circuit configuration, semiconductor technology, and set of desirable properties.

Bipolar Logic Families

There are two types of operations in bipolar logic families: 1. Saturated and 2. Non-saturated.

In saturated logic, the transistors in the IC are driven to saturation, whereas in the case of non-saturated logic, the transistors are not driven into saturation.

The saturated logic families are diode transistor logic (DTL) transistor–transistor logic (TTL), etc.

However, the non-saturated logic families are Schottky TTL, emitter-coupled logic (ECL), etc.

Unipolar Logic Families

MOS devices are unipolar devices and only MOSFETS are employed in MOS logic circuits;

MOS logic families are PMOS, NMOS, and CMOS.

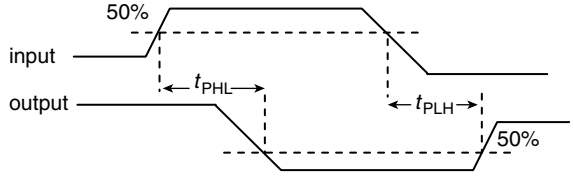
Classification of Digital ICs

IC classification	Equivalent individual gates per chip	Number of components
Small scale integration (SSI)	Less than 12	Up to 99
Medium scale integration (MSI)	12–99	100–999
Large scale integration (LSI)	100–99	1000–9,999
Very large scale integration (VLSI)	Above 1,000	Above 10,000
Ultra large scale integration (ULSI)	—	10^6–10^7
Giant scale integration (GSI)	—	Above 10^7

Characteristics of Digital ICs

Speed of Operations

The speed of digital circuits is specified in terms of propagation delay time.



Input and output waveform to define propagation delay times. The propagation delay time of logic gates is taken as average of these two delay times.

Power Dissipation

It is determined by the current I_{CC} that is drawn from V_{CC} supply and is given as $V_{CC} \times I_{CC}$. I_{CC} is average of I_{CC} (0) and I_{CC} (1), and it is known as static power dissipation, as it is power consumed by current when input signals are not changing.

Figure of Merit

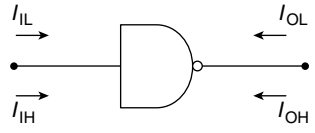
It is product of speed and power.

Figure of merit = propagation delay (ns) × power (mW).

Fan-out: It is the number of similar gates that can be driven by a gate; high fan-out is advantageous.

Current and Voltage Parameters

1. High-level input voltage V_{IH}: minimum input voltage that is recognized by the gate as logic 1.
2. Low-level input voltage V_{IL}: maximum input voltage that is recognized by gate as logic 0.
3. High-level output voltage V_{OH}: minimum voltage available at the output corresponding to logic 1.
4. Low level output voltage V_{OL}: maximum voltage available at the output corresponding to logic 0.
5. High-level input current I_{IH}: minimum current that must be supplied by a driving source corresponding to logic '1' level voltage.
6. Low-level input current I_{IL}: minimum current that must be supplied by a driving source corresponding to logic '0' level voltage.
7. High-level output current I_{OH}: maximum current that the gate can sink in logic '1' level.
8. Low-level output current I_{OL}: this is the maximum current that the gate can sink in logic '0' level.



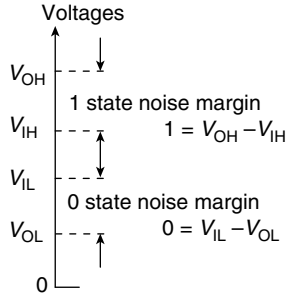
A gate with current directions marked:

I_{CC} (1): High-level supply current when output is at logic 1.

I_{CC}(0): Low-level supply current when output of gate is at logic 0.

Noise Immunity

Stray electric and magnetic fields may induce unwanted voltage known as noise on connecting wires between logic circuits.



This may cause the voltage at the input to a logic circuit to drop below V_{IH} or rise above V_{IL} and may produce undesired operation.

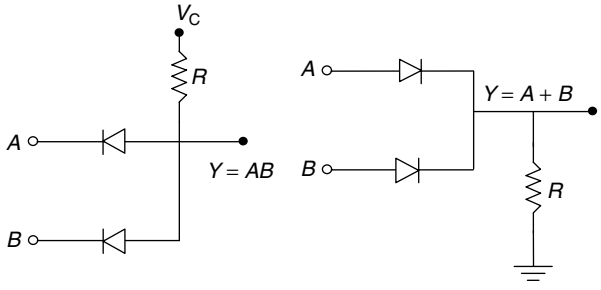
The circuit's ability to tolerate noise signals is referred to as noise immunity, a quantitative measure of which is called noise margin.

1. **Noise Margin:**
   High-state noise margin $V_{NH} = V_{OH(min)} - V_{IH(min)}$
   Low-state noise margin $V_{NL} = V_{IL(max)} - V_{OL(max)}$
   Therefore, overall noise margin $NM = \min \{V_{NH}, V_{NL}\}$
   HTL logic family has the highest noise margin among all logic families.

2. **Fan-out:**
   $$\text{Fan-out (high)} = F_{OH} = \frac{I_{OH(max)}}{I_{IH(max)}}$$
   $$\text{Fan-out (low)} = F_{OL} = \frac{I_{OL(max)}}{I_{IL(max)}}$$
   Therefore, overall Fan-out = min $\{F_{OH}, F_{OL}\}$.
   CMOS logic family has the highest fan-out among all families.

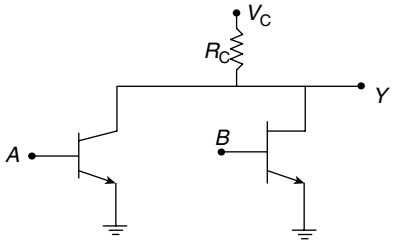
Basic Gates and its Diode Circuit Diagram

AND gate:- **OR gate:-**



Direct Coupled Transistor Logic (DCTL)

In the RTL logic family, if the base resistor is disconnected, we obtain DCTL.



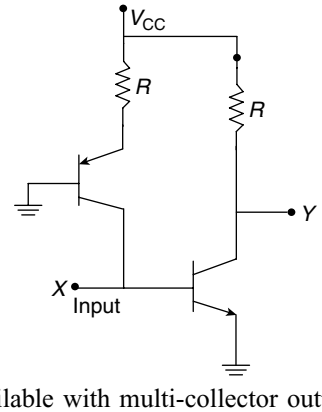
It is suffering from current hogging problem.

1. The noise margin of the DCTL is very poor.
2. The basic gate is an NOR gate.

Integrated Injection Logic

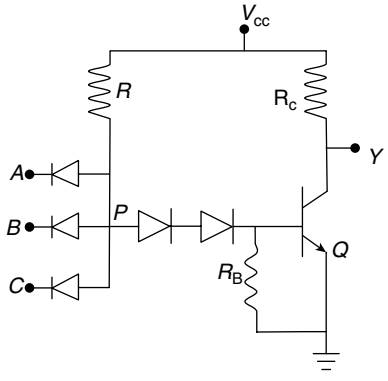
Integrated injection logic (I^2L) is the modified version of direct coupled transistor logic (DCTL). The DCTL suffers from the current hogging problem. It is also called merged-transistor logic (MTL).

In I^2L logic family, PNP and NPN transistors are integrated so it uses very small silicon chip area.



1. I^2L available with multi-collector output. Therefore, its fan-out is higher than RTL logic family.
2. The speed of operation of I^2L depends upon the charging current and the propagation delay time is inversely proportional to the charging current.
3. Figure of merit is in the range of 0.1–0.7 pJ.
4. I^2L has the highest figure of merits among all logic families.

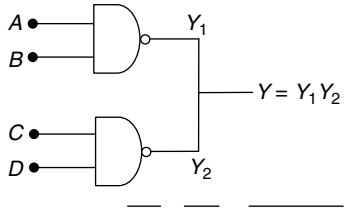
Diode-transistor logic (DTL)



If any of the input is low, the input diode will be forward biased and the voltage at P drives transistor Q to cut off; therefore, output Y is V_{CC}. If all the inputs are HIGH, then none of the input diode will be forward biased and voltage V_{CC} through 'R' and P will drive transistor Q into saturation and output Y will be $V_{CE,\ sat}$, which is logic 0.

If we consider voltage corresponding to logic 1 and 0 as V_{CC} and V_{CE}, respectively, this circuit performs NAND operation.

The propagation delay time of commercially available DTL gates are of the order of 30 to 80 ns. If outputs of gates are connected together, additional logic is performed without additional hardware. This type of connection is referred to as wired logic or wired AND.

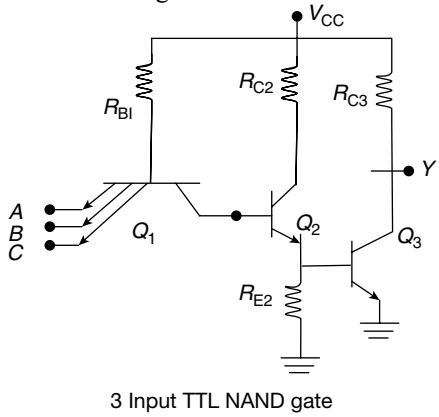


$$Y = Y_1\ Y_2 = \overline{AB}\ .\ \overline{CD} = \overline{AB + CD}$$

Transistor–Transistor Logic (TTL)

It is the most successful bipolar logic; TTL logic families use transistors both to perform logic functions and to provide high output drive capability.

The NAND gate is the basic TTL logic circuit. It uses multiple-emitter transistor Q_1. The number of inputs (fan-in) to the gate is same as the number of emitters fabricated during its manufacturing.



3 Input TTL NAND gate

If at least one input is low, the corresponding emitter base junction is forward biased; therefore, the base voltage of Q_1 will not able to make base collector junction of Q_1 to forward bias and for Q_2 and Q_3 to be conductions. Hence, Q_2 and Q_3 are OFF and $Y = V_{CC} = V(1)$.

If all inputs are HIGH, the emitter-base junctions of Q_1 are reverse biased. If we assume that Q_2 and Q_3 are ON, then $Y = V(0) = 0.2$ V.

The fan-out (N) of a gate depends upon the maximum collector current rating of the transistor Q_3. The total collector current $I_{C3} = I_{C3,\,sat} = N.\ I_L$, when the output is in the low state.

If the output of the gates are connected together, wired AND logic is performed. The output voltage is pulled up by the time constant $T = R_{C3}$. C_0 resistance R_{C3} is known as pull-up resistor.

It is possible in TTL gates to hasten the charging of output capacitance without corresponding increase in power dissipation with the help of an output circuit arrangement referred to as on active pull-up or totem pole output.

Wired-AND connection must not be used for totem-pole output circuits because of the current spike problem.

Open-collector Output

A circuit with open-collector output is same as the circuit except for the collector-resistor R_{C3} of Q_3, which is missing. The collector terminal is available outside the IC and the passive pull up is to be connected externally.

If any input of a TTL gate is left disconnected, (open or floating) the corresponding E–B junction of Q_1 will not be forward biased. Hence, it acts exactly in the same way as if logic 1 is applied to that input. Therefore, in TTL, ICs and all unconnected inputs are treated as logic 1's.

Schottky TTL

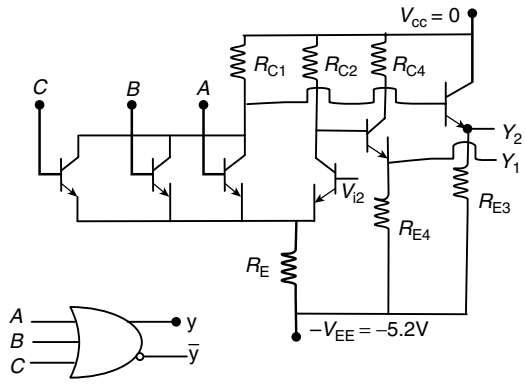
The speed limitation of TTL is mainly due to the turn-off time delays involved in transistors while making transistors from saturation to cut off. This can be eliminated by replacing the transistors of TTL gate by Schottky transistors.

Emitter-coupled Logic (ECL)

ECL is the fastest of all logic families, and therefore, it is used in applications where very high speed is essential. "High speeds have become possible in ECL because the transistor are used in differential amplifier configuration, in which they are never driven into saturation". Thereby, the storage time is eliminated. Propagation delays of less than 1 ns per gate have become possible in ECL.

ECL is realized using difference amplifier in which the emitters of the two transistors are connected, and hence, it is referred to as emitter-coupled logic. Two outputs, Y_1 and Y_2, which are complementary, are available at ECL output; Y_1 corresponds to OR output and Y_2 corresponds to NOR output.

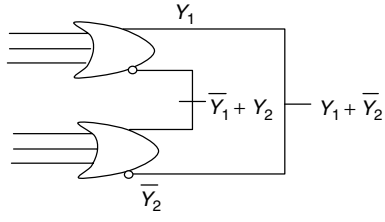
In ECL, the positive end of the supply is connected to ground in contrast to other logic families. Because of the low output impedance and high input impedance, the fan-out of ECL is large.



3 input ECL OR / NOR gate

Wired OR Logic

The outputs of two or more ECL gates can be connected to obtain wired OR logic without using additional hardware.



Wired-OR connection of ECL

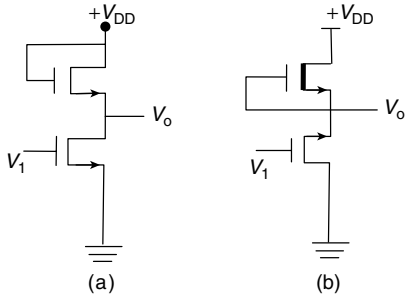
If any input of an ECL gate is left unconnected, the corresponding E–B junction of input transistor will not be conducting. Hence, it acts as if logic 0 level voltage is applied to that input.

MOS Logic

MOSFETS have become very popular for logic circuits due to high density of fabrication and low power dissipation. When MOS devices are used in logic circuits, there can be circuits in which either only p-channel (PMOS) or n-channel (NMOS) devices are used.

It is also possible to fabricate enhancement mode P-channel and n-channel MOS devices (CMOS) on the same chip. The power dissipation is extremely small for CMOS, and hence, CMOS logic has become very popular.

The basic MOS gate is an inverter.



An MOS inverter with
(a) enhancement load and
(b) depletion load is shown in the figure.

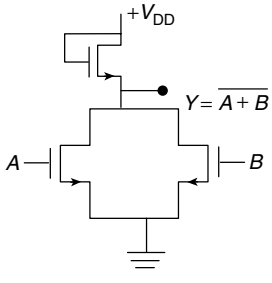
The logic levels of MOS circuits are

$$V(0) = 0$$
$$V(1) = V_{DD}$$

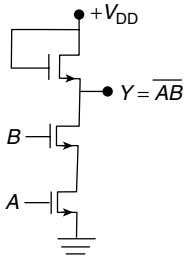
MOSFET NAND and NOR Gates

NOR gates can be obtained by using multiple drives in parallel, whereas for NAND gates, the drives are to be connected in series.

If the input is 0, the corresponding transistor is OFF, else it will be in ON state. Since MOS devices have very high input impedance, the fan-out is large, but driving a large number of MOS gates increases the capacitance at the output of the driving gate, which in turn reduces the speed of MOS gates.



2 Input NMOS NOR gate



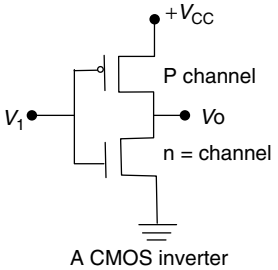
2 Input NMOS, NAND gate

The propagation delay of MOS devices is large because of large capacitance present at the input and output of these devices.

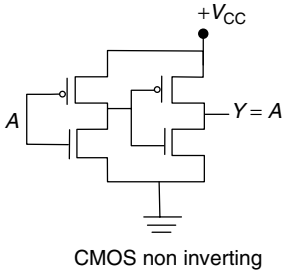
MOS devices have very high input impedance and even a small static charge flowing into this high impedance can develop a dangerously high voltage. Therefore, MOS ICs inputs must not be left unconnected.

CMOS Logic

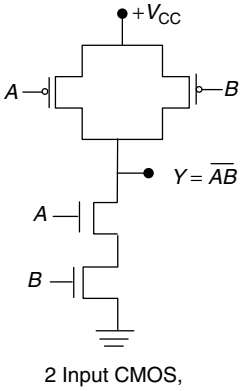
A complementary MOSFET (CMOS) is obtained by connecting a *p*-channel and *n*-channel MOSFET in series with drains tied together and the output is taken at the common drain.



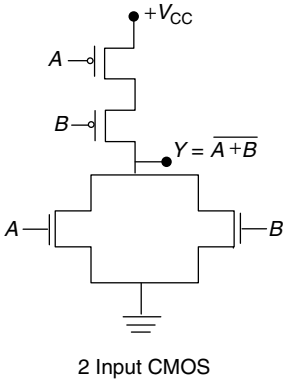
A CMOS inverter



CMOS non inverting Buffer

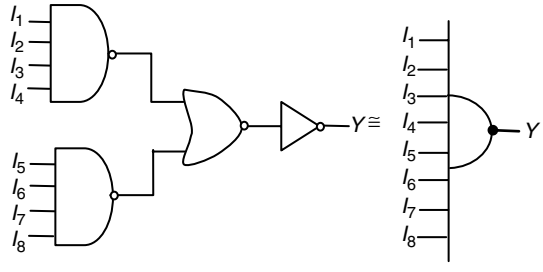


2 Input CMOS, NAND gate



2 Input CMOS NOR gate

In CMOS logic, gates with larger number of inputs can be made by cascading gates with fewer inputs, which are faster and smaller than the gates obtained by extending series–parallel transistors.



Internal structure and equivalent logic for 8-input CMOS NAND

In the given logical structure of 8-input CMOS NAND gate, the total propagation delay of this circuit is less than the delay of one-level 8-input NAND circuit.

CMOS logic levels are functions of supply voltage and are approximately

$$V_{OH} = V_{CC} - 0.1V$$

$$V_{IH} = 0.7V_{CC}\,,\ V_{IL} = 0.3V_{CC},\ V_{OL} = 0.1V$$

The DC margins are

$$\Delta 1 = V_{OH} - V_{IH} = V_{CC} - 0.1V - 0.7V_{CC}$$

$$\Delta 0 = V_{IL} - V_{OL} = 0.3V_{CC} - 0.1V$$

The CMOS noise margins are much higher than the TTL noise margins.

For HC series, CMOS current ratings are

$I_{IH} = 1\ \mu A,\ I_{IL} = -1\ \mu A,\ I_{OH} = 0.02\ mA,\ I_{OL} = 0.2\ mA$

$$\text{The low-state fan-out} = \frac{I_{OL}}{I_{IL}} = \frac{0.02}{0.001} = 20$$

$$\text{The high-state fan-out} = \frac{I_{OH}}{I_{IH}} = \frac{0.02}{0.001} = 20$$

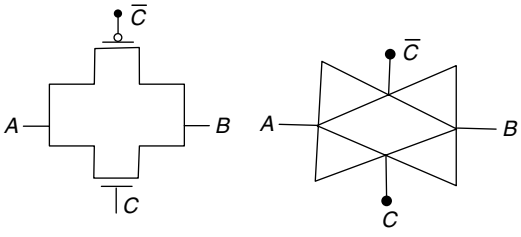
An unused NAND or AND input should be tied to logic 1 level, voltage through a pull up resistor and an unused NOR/OR input should be tied to logic 0 level voltage through a pull down resistor.

The presence of parasitic transistors between V_{CC} and ground of any CMOS device; for high input voltages, they cause a virtual short circuit between V_{CC} and ground, resulting in a very high dissipation enough to destroy the device.

This condition is known as latch up (i.e., stay ON permanently). To prevent latch-up condition, modern CMOS logic circuits are fabricated with special structures like Zener diodes at inputs for protection.

CMOS Transmission Gate

It is controlled by gate voltages C and $\overline{C}$. If $C = 1$, then signal transmitted from A to B; if $C = 0$, transmission is not possible.



Example 24

Simplify the Boolean function, $x\,y + x'z + y\,z$

Solution

$$x\,y + x^1\,z + y\,z$$

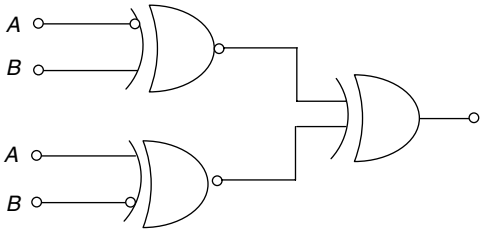
By using consensus property

$$xy + x^1z + yz = xy + x^1z$$

$$Y = xy + x^1z$$

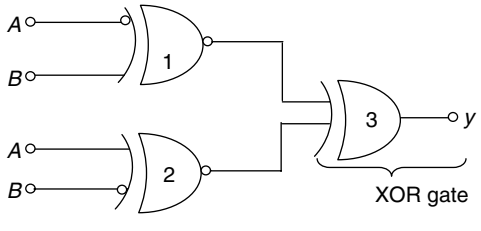
Example 25

The output of the given circuit is equal to



Solution

$$\overline{A} \odot B = \overline{A}B + A\overline{B}$$



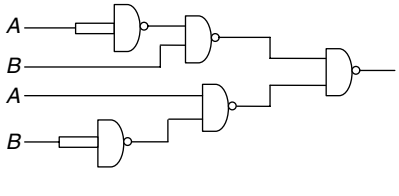
$$A \odot \overline{B} = \overline{A}B + A\overline{B}$$

Therefore, the output of the above mentioned circuit is '0'. As two inputs are same at third gate, the output of XOR gate with two equal inputs is zero.

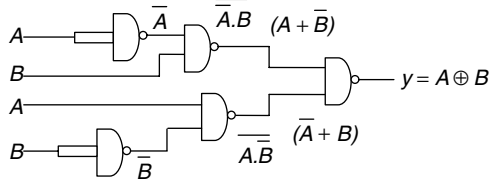
Therefore, $y = 0$.

Example 26

The circuit shown in the figure is functionally equivalent to



Solution



$$y = \overline{\left(\overline{\overline{A}.B}.\overline{A\overline{B}}\right)} = \overline{\left(A+\overline{B}\right)\left(\overline{A}+B\right)} \because \left(\overline{A.B} = \overline{A}+\overline{B}\right)$$

$$= \overline{\left(A+\overline{B}\right)}+\overline{\left(\overline{A}+B\right)} = \overline{A}.\overline{\overline{B}}+\overline{\overline{A}}.\overline{B} = \overline{A}.B + A.\overline{B}c = A \oplus B$$

Example 27

Simplify the Boolean function $A \oplus \overline{A}\,B \oplus \overline{A}p$

Solution

$$A \oplus \overline{A}\,B \oplus \overline{A}$$

Associativity

$$= 1 \oplus \overline{A}B = \overline{\overline{A}\,B} = A + \overline{B} \qquad (\because \textit{Demorgans})$$

Example 28

CD \ AB	00	01	11	10
00	0	0	1	1
01	0	x	x	1
11	x	x	1	x
10	1	0	1	1

Find the minimized expression for the given K-map is

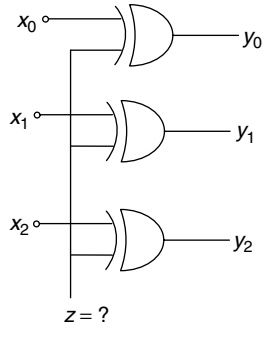
Solution

AB \ CD	00	01	11	10
00	0	0	1	1
01	0	x	x	1
11	x	x	1	x
10	1	0	1	x

$$= A + \overline{B}C$$

Example 29

In the figure shown, y_2, y_1, and y_0 will be 1's complement of x_2, x_1, and x_0 if $z = ?$



Solution

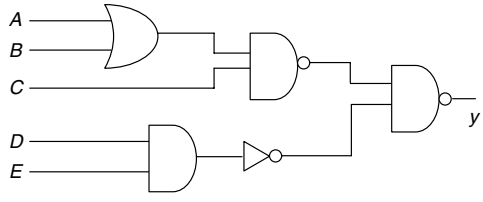
We are using XOR gate

Therefore, XOR output is the complement of input only when other input is high.

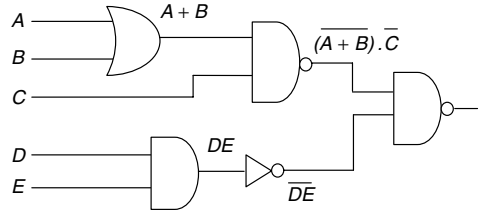
Therefore, $Z = 1$

Example 30

The output y of the circuit shown in the figure is



Solution



$$y = \overline{\overline{(A+B).C}.\overline{DE}} = \overline{\overline{(A+B).C}} + \overline{\overline{DE}}$$

$$= (A+B)C + DE\left(\overline{x.y} = \overline{x} + \overline{y}\right)$$

Example 31

Simplify the following function

$$f = \overline{\overline{A(\overline{AB})}.\overline{B(\overline{AB})}}$$

Solution

$$\overline{\overline{A\left(\overline{AB}\right)}.\overline{B\left(\overline{A.B}\right)}}$$

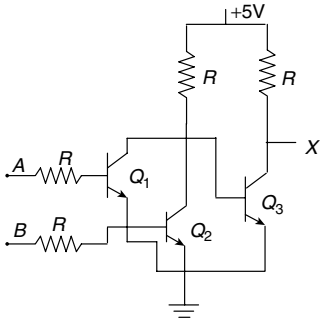
$$\overline{\left[A+\left(\overline{AB}\right)\right].\left[B+\left(\overline{AB}\right)\right]} = \overline{A+\left(\overline{AB}\right)} + \overline{\left(B+\overline{AB}\right)}$$

$$= \overline{A}.\left(\overline{AB}\right) + \overline{B}.\left(\overline{AB}\right) = \overline{A}.\left(\overline{A}+\overline{B}\right) + \overline{B}\left(\overline{A}+\overline{B}\right)$$

$$= \overline{A}.\overline{A} + \overline{A}\,\overline{B} + \overline{B}\,\overline{A} + \overline{B}.\overline{B} = \overline{A} + \overline{B} = \overline{AB}$$

Example 32

Which gate is represented by the circuit shown in figure?



(A) NAND (B) NOR

(C) OR (D) AND

Solution

Transistors with A, B inputs form RTL NOR gate; other transistor is inverter, so the circuit is OR gate. If any input is 1, either Q_1 or Q_2 will be in saturation; therefore, Q_3 will be in cut off, $x \approx V_{CC}$ (logic 1), and hence, it is OR gate.

Example 33

In a 7400 TTL NAND gate, Vcc = +5 V and a 5 kΩ load is connected to its output. Find the output voltage

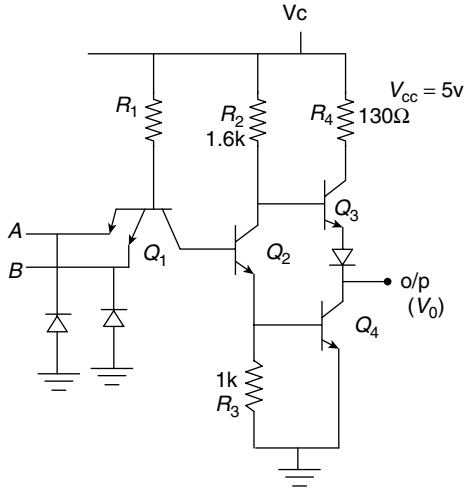
(i) when both the inputs are +5 V and

(ii) when both the inputs are 0 V

(A) 0.1 V, 4.09 V (B) 4.8 V, 2.6 V

(C) 4.09 V, 2.26 V (D) 0.1 V, 3 V

Solution



When both the inputs are high (i.e., +5 V), Q_2 and Q_4 are in saturation. When Q_4 is in saturation, its output is Vce(sat) = low = 0.1 V.

When both inputs are low 0 V, the output is high (Q_3 is ON but Q_2 and Q_4 are OFF)

Therefore, $V_{OH} = V\text{cc} - I_L R_4 - V\text{ce(sat)} - V_D$

$$= 5 - (I_{OH} \times 130) - 0.1 - 0.7$$

$$= (5 - 0.8 - 130 I_L)\ \text{V}$$

$$I_{OH} = \frac{V_{OH}}{5\text{k}\Omega}$$

$$V_{OH} = 4.2 - 130 \times \frac{V_{OH}}{5000}\ \text{V}$$

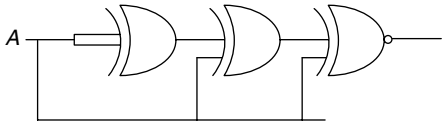
$$V_{OH} = \frac{4.2}{1 + \frac{13}{500}}\ \text{V} = 4.09\text{V}$$

EXERCISES

Practice Problems I

Direction for questions 1 to 33: Select the correct alternative from the given choices.

1. The output of the following circuit is



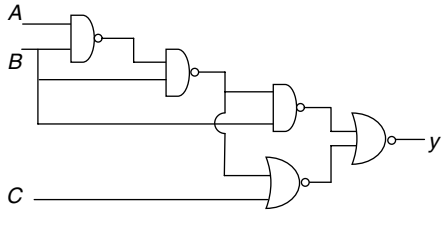
(A) 0 (B) 1 (C) A (D) A^1

2. The circuit that will work as OR gate in positive level will work as _____ gate in negative level logic
(A) NOR gate
(B) NAND gate
(C) Both NAND and NOR gate
(D) AND gate

3. Four logical expressions are given:
(a) $\overline{A}.\overline{B}.\overline{C}.\overline{D}\ \overline{E}.\overline{F}.\overline{G}.\overline{H}$
(b) $\overline{AB}.\overline{CD}.\overline{EF}.\overline{GH}$
(c) $\overline{A}+\overline{B}+\overline{C}+\overline{D}+\overline{E}+\overline{F}+\overline{G}+\overline{H}$
(d) $\left(\overline{A}+\overline{B}\right)\left(\overline{C}+\overline{D}\right)\left(\overline{E}+\overline{F}\right)\left(\overline{G}+\overline{H}\right)$

Two of these expression are equal. They are
(A) c and d (B) b and d (C) a and b (D) a and c

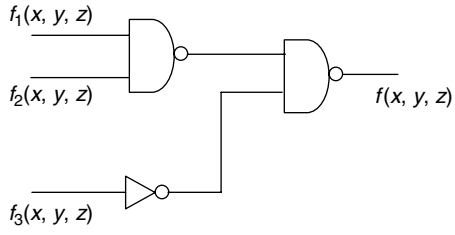
4. For the logic circuit shown in figure, the simplified Boolean expression for the output y is



(A) $A+\overline{B}+C$ (B) $A\,\overline{\ }$
(C) $AB\overline{C}$ (D) $B\overline{C}$

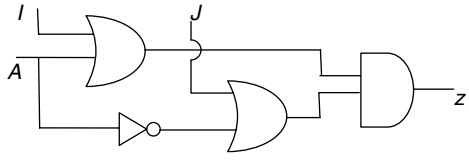
5. In a digital system, there are three inputs A, B, and C. The output should be high when at least two inputs are high. The minimized Boolean expression for the output is
(A) $AB+BC+AC$
(B) $ABC+AB\overline{C}+\overline{A}BC+A\overline{B}C$
(C) $AB\overline{C}+A\overline{B}C+\overline{A}BC$
(D) $A\overline{B}+B\overline{C}+\overline{A}C$

6. Consider the following logic circuit whose inputs are functions f_1, f_2, and f_3 and output is f



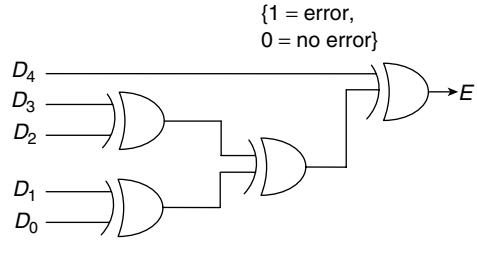
Given that
$f_1(x, y, z) = \sum (0, 1, 3, 5)$
$f_2(x, y, z) = \sum (6, 7)$ and
$f(x, y, z) = \sum (1, 4, 5)$, then F_3 is
(A) Σ (1, 4, 5) (B) Σ (6, 7)
(C) Σ (0, 1, 3, 5) (D) None of these

7. The above mentioned circuit is used to implement the function $z = f(A, B) = \overline{A}+B$. What values are to be selected for I and J?



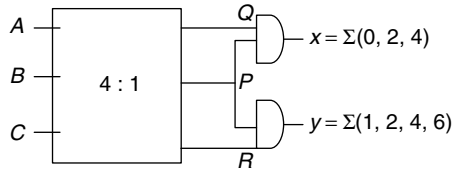
(A) $I = 0, J = B$ (B) $I = 1, J = B$
(C) $I = B, J = 1$ (D) $I = B, J = 0$

8. Find the parity checker output from the following figure, if input is 11111 (D_4 D_3 D_2 D_1 D_0) and 10000 (D_4 D_3 D_2 D_1 D_0)



(A) error, error (B) error, no error
(C) no error, error (D) no error, no error

9. For the given combinational network with three inputs A, B, and C, three intermediate outputs P, Q, and R, and two final outputs $X = PQ = \Sigma(0, 2, 4)$ and $Y = PR = \Sigma(1, 2, 4, 6)$ as shown in the figure. Find the smallest function P (containing minimum number of minterms that can produce the output x and y).



(A) $\Sigma(2, 4)$ (B) $\Sigma(0, 1, 2, 4, 6)$
(C) $\Sigma(3, 5, 7)$ (D) $\Sigma(1, 2, 6)$

10. The standard form of expression $AB + ACD + \bar{A}C$ is

(A) $AB\bar{C}\bar{D} + ABC\bar{D} + AB\bar{C}D + ABCD + A\bar{B}CD + \bar{A}BCD + \bar{A}BC\bar{D} + \bar{A}\,\bar{B}CD + \bar{A}B\bar{C}\bar{D}$

(B) $AB + ACD + \bar{A}C$

(C) $AB\bar{C} + ABC + ABCD + \bar{A}CB + \bar{A}C\bar{B}\bar{D}$

(D) $\bar{A}\bar{B}\bar{C}\bar{D} + ABCD + \bar{A}BC + AB\bar{D} + ABC$

11. Factorize $\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D$

(A) $B + C$ (B) $AB + CD$

(C) $\bar{B}\bar{C}$ (D) AC

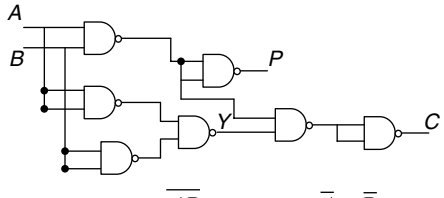
12. The K-map of a function is as shown in the figure. Find the function.

wx \ yz	00	01	11	10
	1			1
	1	1	1	1
	1			1
	1			1

(A) wx (B) $\bar{z}$

(C) $\bar{w}(z + \bar{z}) + \bar{z}w$ (D) $wx + \bar{z}$

13. The Boolean expression for P is



(A) AB (B) $\overline{AB}$ (C) $\bar{A} + \bar{B}$ (D) $A + B$

14. The Boolean expression for the truth table is

A	B	C	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

(A) $B(A + C)(\bar{A} + \bar{C})$ (B) $\bar{B}(A + \bar{C})(\bar{A} + \bar{C})$

(C) $B(A + \bar{C})(\bar{A} + C)$ (D) $\bar{B}(A + C)(\bar{A} + \bar{C})$

15. Simplify (d represents don't care)

C \ AB	00	01	11	10
0	1	d		1
1	1	d		1

(A) $\bar{B}$ (B) $\bar{B} + C$ (C) $\bar{B} + \bar{A}$ (D) $A + \bar{C}$

16. Simplify $\overline{(AB + \bar{C}).(\overline{A + B} + C)}$

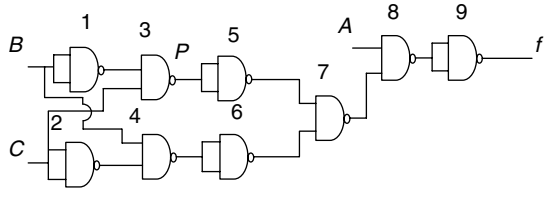
(A) $(\bar{A} + \bar{B} + \bar{C}).(A + B + C)]$

(B) $(\bar{A} + B + C).(A + \bar{B} + \bar{C})$

(C) $(\bar{A} + \bar{B}).(A + B + C)$

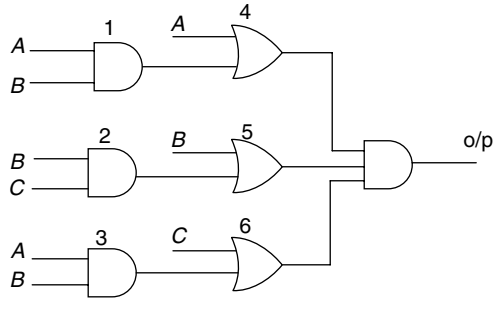
(D) None of these

17. The point P in the figure is stuck at 1. The output f will be



(A) $\overline{ABC}$ (B) $\bar{A}$ (C) $AB\bar{C}$ (D) A

18. Find the function represented by the figure

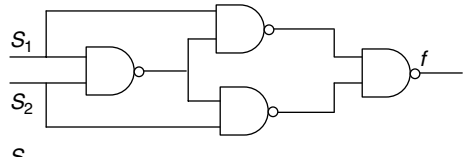


(A) $A + B + C$ (B) AB

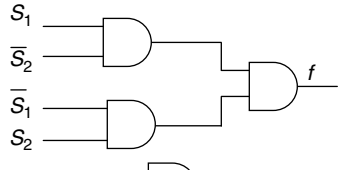
(C) $AB + C$ (D) $B + C$

19. A staircase light is controlled by two switches, one is at the top of the stairs and other at the bottom of stairs. Realization of this function using NAND logic results in which of the following circuits? (Assume S_1 and S_2 are the switches)

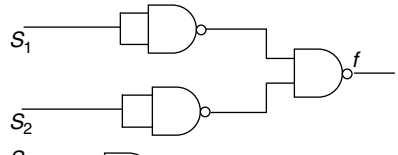
(A)



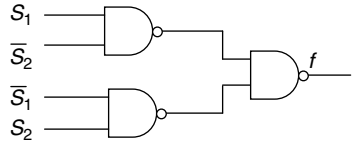
(B)



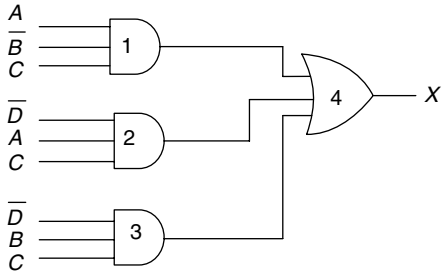
(C)



(D)



20. For the given figure, simplify the expression and find which is the redundant gate?



(A) $ABC + DBC$, 4 (B) $A\bar{B}C + \bar{D}AC$, 3

(C) $\bar{D}AC + \bar{D}BC$, 1 (D) $A\bar{B}C + \bar{D}BC$, 2

21. The function $f = A \oplus B \oplus C \oplus D$ is represented as

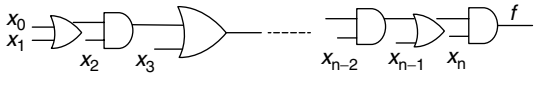
(A) $f(A, B, C, D) = \sum(2, 6, 10, 11, 12, 13, 14)$

(B) $f(A, B, C, D) = \sum(3, 5, 7, 10, 11, 12, 13, 14)$

(C) $f(A, B, C, D) = \sum(1, 2, 6, 8, 10, 12, 13, 14)$

(D) $f(A, B, C, D) = \sum(1, 2, 4, 7, 8, 11, 13, 14)$

22. Find the function represented



(A) $(x_0 + x_1)(x_2 + x_3)(x_4 + x_5) \ldots\ldots\ldots (x_{n-1} + x_n)$

(B) $x_0 + x_1 + x_2 + x_3 + \ldots\ldots + x_n$

(C) $x_0x_2x_4 \ldots\ldots x_n + x_1x_2 \ldots\ldots x_n + x_{n-1}x_n$

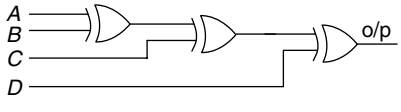
(D) $x_0x_1 + x_2x_3 + \ldots.. + x_{n-1}x_n$

23. The minimum number of NAND gates required to implement $A \oplus B \oplus C$ is

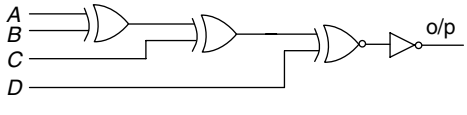
(A) 8 (B) 10 (C) 9 (D) 6

24. Which of the following circuit will generate an odd parity for a 4-bit input? (Assume *ABCD* as input)

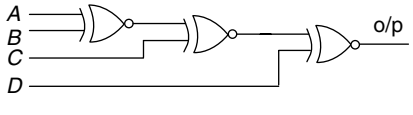
(A)



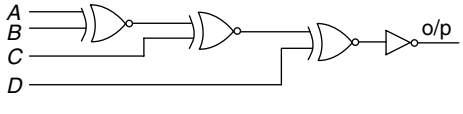
(B)



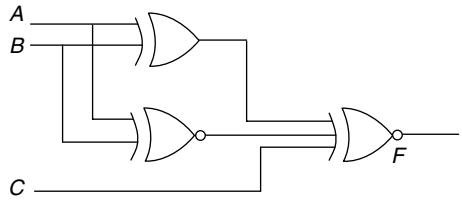
(C)



(D)



25. For the output *F* to be 1 in the circuit, the input combination should be



(A) $A = 1, B = 1, C = 0$ (B) $A = 1, B = 0, C = 0$

(C) $A = 0, B = 1, C = 0$ (D) $A = 0, B = 0, C = 1$

26. The highest noise margin is offered by

(A) TTL (B) ECL (C) I^2L (D) CMOS

27. A LSI IC Package contains ———— logic gates.

(A) 10 (B) 50

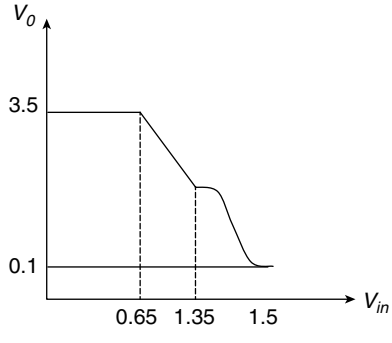
(C) less than 50 (D) More than 100

28. For interfacing two logic gates, the condition is

(A) $V_{OH} > V_{IH}$, $V_{IL} > V_{OL}$ (B) $V_{OH} < V_{IH}$, $V_{IL} < V_{OL}$

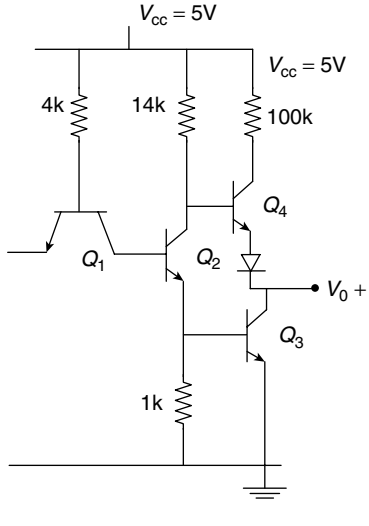
(C) $V_{OH} > V_{IH}$, $V_{IL} < V_{OL}$ (D) $V_{OH} = V_{IH}$, $V_{IL} = V_{OL}$

29. The I/O characteristics of which logic family is specified in the figure.



(A) TTL (B) CMOS (C) I^2L (D) DTL

30. The circuit diagram of a standard TTL NOT gate is shown in the figure. If input is 2.5V, the modes of operation of transistor is



(A) Q_1: reverse active
Q_2: normal active

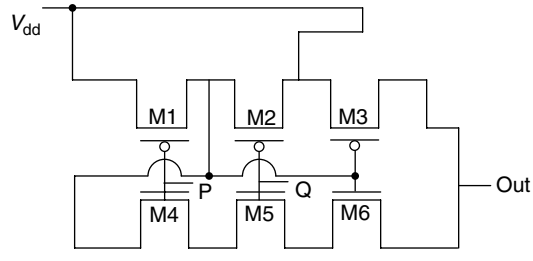
Q_3: saturation
Q_4: cut-off

(B) Q_1: reverse active
Q_2: saturation
Q_3: saturation
Q_4: cut-off

(C) Q_1: normal active
Q_2: cut-off
Q_3: cut-off
Q_4: saturation

(D) Q_1: saturation
Q_2: saturation
Q_3: saturation
Q_4: normal active

31. The logic function implemented by the following circuit at output terminal is



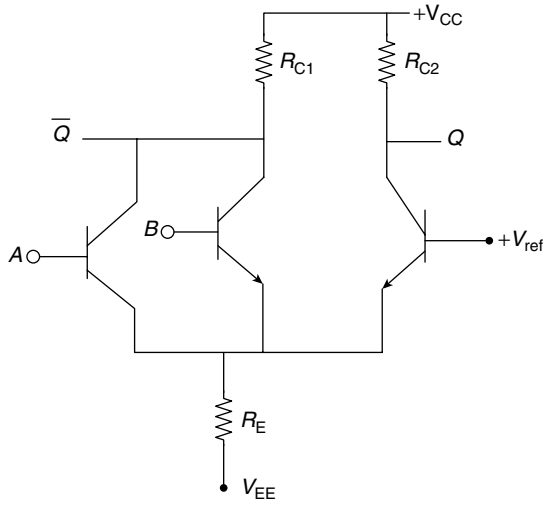
(A) P NOR Q (B) P NAND Q
(C) P OR Q (D) P AND Q

32. Match the options in column 1 with column 2

Column 1	Column 2
(a) TTL	1. Superfast computers
(b) NMOS	2. MSI
(c) CMOS	3. LSI
(d) ECL	4. VLSI

(A) a – 2, b – 3, c – 4, d – 1
(B) a – 3, b – 2, c – 4, d – 1
(C) a – 2, b – 3, c – 4, d – 1
(D) a – 1, b – 3, c – 1, d – 2

33. Which gate is represented by the circuit?



(A) NAND (B) NOR (C) OR (D) AND

Practice Problems 2

Direction for questions 1 to 33: Select the correct alternative from the given choices.

1. An OR gate has six inputs. How many input words are there in its truth table?
(A) 6 (B) 36 (C) 32 (D) 64

2. Sum of product form can be implemented by using
(A) AND–OR (B) NAND–NAND
(C) NOR–NOR (D) Both *A* and *B*

3. Which one of the following is equivalent to the Boolean expression:

$Y = AB + BC + CA$

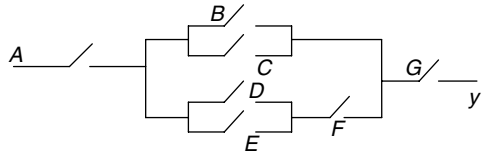
(A) $\overline{AB + BC + CA}$

(B) $(\overline{A}+\overline{B})(\overline{B}+\overline{C})(\overline{A}+\overline{C})$

(C) $\overline{(A+B)(B+C)(A+C)}$

(D) $\overline{(\overline{A}+\overline{B})(\overline{B}+\overline{C})(\overline{C}+\overline{A})}$

4. What Boolean function does the following circuit represents?



(A) $A\,[F + (B + C).\,(D + E)]\,G$
(B) $A + BC + DEF + G$
(C) $A\,[(B + C) + F\,(D + E)]\,G$
(D) $ABG + ABC + F(D + E)$

5. The minimum number of two input NOR gates are required to implement the simplified value of the following equation
$f(w, x, y, z) = \Sigma m(0, 1, 2, 3, 8,9\ 10,11)$
(A) One (B) Two (C) Three (D) Four

6. The output of a logic gate is '1', when all inputs are at logic '0'. Then, the gate is either
(1) NAND or XOR gate
(2) NOR or XOR gate
(3) NOR or XNOR gate
(4) NAND or XNOR gate
(A) 1 and 2 (B) 2 and 3
(C) 3 and 4 (D) 4 and 1

7. If the functions w, x, y, and z are as follows.

$w = R + \overline{P}Q + \overline{R}S$

$x = PQ\overline{R}\overline{S} + \overline{P}Q\overline{R}S + P\overline{Q}\overline{R}\overline{S}$

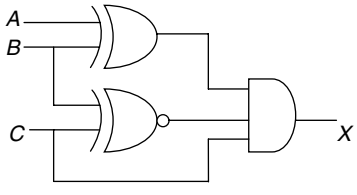
$y = RS + \overline{PR + P\overline{Q} + \overline{P}.\overline{Q}}$

$z = R + S + \overline{PQ + \overline{P}.\overline{Q}.\overline{R} + P.\overline{Q}.\overline{S}}$

(A) $w = z$, $x = y$ (B) $w = z$, $x = \overline{z}$

(C) $w = y$ (D) $w = y = z$

8. For the logic circuit shown in the figure, the required input condition (A, B, C) to make the output (x) = 1 is



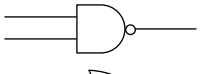
(A) 0, 0, 1 (B) 1, 0, 1 (C) 1, 1, 1 (D) 0, 1, 1

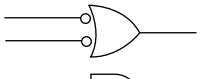
9. Which of the following is a basic gate?

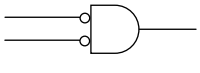
(A) AND (B) XOR

(C) XNOR (D) NAND

10. Which of the following represent the NAND gate?

(a) 

(b) 

(c) 

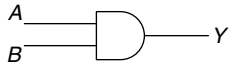
(A) a only (B) a, b, c (C) b, a (D) a, c

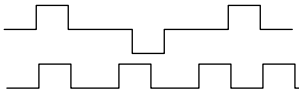
11. The universal gates are

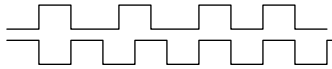
(A) NAND and NOR (B) AND, OR, NOT

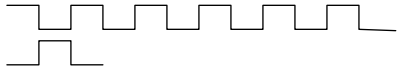
(C) XOR and XNOR (D) All of these

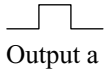
12. In the circuit, the value of input A goes from 0 to 1 and part of B goes from 1 to 0. Which of the following represent output under a static hazard condition?



(a) 

(b) 

(c) 

(d) 

(A) Output a (B) Output b

(C) Output c (D) Output d

13. The consensus theorem states that

(A) $A + \overline{A}B = A + B$

(B) $A + AB = A$

(C) $AB + \overline{A}C + BC = AB + \overline{A}C$

(D) $(A + B).(A + \overline{B}) = A$

14. The dual form of expression

$AB + \overline{A}C + BC = AB + \overline{A}C$ is

(A) $(A + B)\left(\overline{A} + C\right)(B + C) = (A + B)\left(\overline{A} + C\right)$

(B) $\left(A + B\right)\left(\overline{A} + C\right)\left(B + C\right) = \left(\overline{A} + \overline{B}\right)\left(A + \overline{C}\right)$

(C) $\left(\overline{A} + \overline{B}\right)\left(\overline{A} + \overline{C}\right)\left(\overline{B} + \overline{C}\right) = \left(\overline{A} + \overline{B}\right)\left(A + \overline{C}\right)$

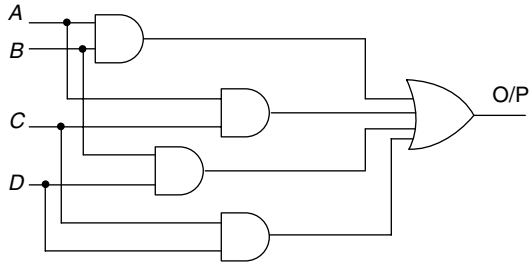
(D) $\overline{A}\overline{B} + A\overline{C} + \overline{B}\overline{C} = \overline{A}\overline{B} + A\overline{C}$

15. The maxterm corresponding to decimal 12 is

(A) $\overline{A} + \overline{B} + C + D$ (B) $A + B + \overline{C} + \overline{D}$

(C) $\overline{A}\overline{B}CD$ (D) $AB\overline{C}\overline{D}$

16. The given circuit is equivalent to



(A) $(A + C)(B + D)$ (B) $AC + BD$

(C) $(A + D)(B + C)$ (D) $(\overline{A} + \overline{B})(\overline{C} + \overline{D})$

17. Minimized expression for Karnaugh map is

C \ AB	00	01	11	10
0	1			1
1	1			1

(A) $AB + C$ (B) $\overline{A}B + C$

(C) $\overline{B}$ (D) $\overline{B} + C$

18. An XOR gate will act as _____ when one of its input is one and as _____ when one of its input is 0.

(A) buffer, buffer (B) buffer, inverter

(C) inverter, buffer (D) inverter, inverter

19. The minimum number of two input NAND gates required to implement $A \odot B$ if only A and B are available

(A) 6 (B) 3 (C) 5 (D) 4

20. Negative logic in a logic circuit is one in which

(A) logic 0 and 1 are represented by GND and positive voltage, respectively

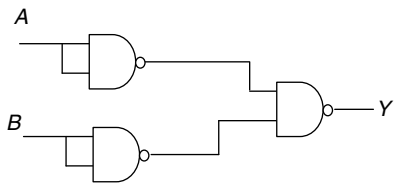
(B) logic 0 and 1 are represented by negative and positive voltage

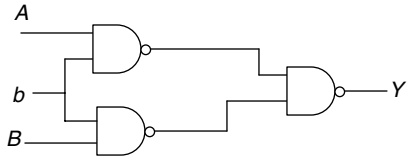
(C) logic 0 voltage level is lower than logic 1 voltage level

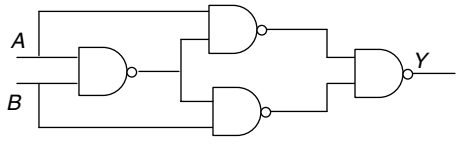
(D) logic 0 voltage level is higher than logic 1 voltage level.

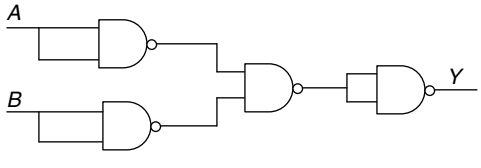
21. If the input to a gate is 8 in number, then its truth table contains ———— input words.
(A) 128 (B) 8 (C) 64 (D) 256

22. The XOR gate implementation using NAND gate is

(A) 

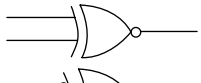
(B) 

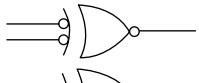
(C) 

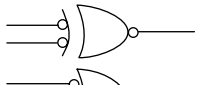
(D) 

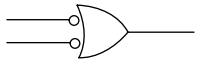
23. The equivalent of AND–OR logic circuit is
(A) NAND–NOR (B) NOR–AND
(C) NAND–NAND (D) NAND–OR

24. The XOR is equivalent to

(A) 

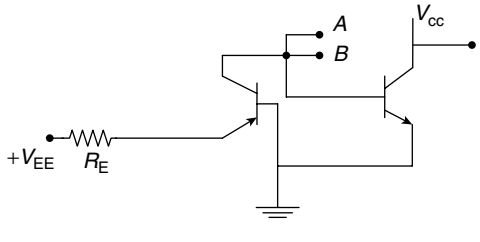
(B) 

(C) 

(D) 

25. Simplify $A\bar{B}C + B + B\bar{D} + AB\bar{D} + \bar{A}C$
(A) B (B) $B + C$ (C) $C + A$ (D) $\bar{A} + B$

26. The gate represented by the circuit is



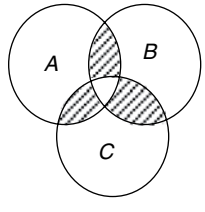
(A) NAND (B) NOR (C) OR (D) AND

27. The full form of I^2L and ECL is
(A) Inter Integrated Logic and Emitter Coupled Logic
(B) Inter Injection Logic and Emitter Combined Logic
(C) Integrated Injection Logic and Emitter Coupled Logic
(D) Integrated Injection Logic and Emission Coupled Logic

28. The most popular TTL family member among digital designers
(A) high speed TTL
(B) standard TTL
(C) low power TTL
(D) low power Schottky TTL

29. The totem pole is standard TTL refer to
(A) output buffer
(B) input emitter stage
(C) open collector output state
(D) phase splitter

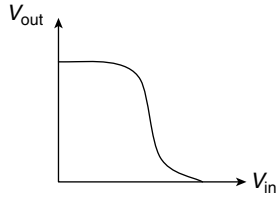
30. Boolean expression for shaded portion is



(A) $ABC + \overline{ABC}$ (B) $AB + BC + CA$
(C) $AB\bar{C} + A\bar{B}C + \bar{A}BC$ (D) $AB\bar{C} + \bar{A}B\bar{C} + \overline{ABC}$

31. The output of the 74 series of TTL gates is taken from a BJT in
(A) totem pole and common collector configuration
(B) either totem pole or open collector configuration
(C) common base configuration
(D) common collector configuration

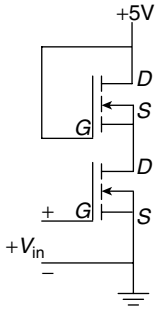
32. The voltage transfer characteristics shown is that of



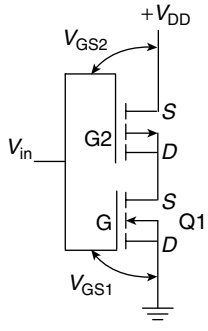
(A) an NMOS inverter with enhancement mode transistor as load.
(B) an NMOS inverter with depletion mode transistor as load.
(C) a CMOS inverter.
(D) a BJT inverter.

33. Which of the following represent NMOS inverter?

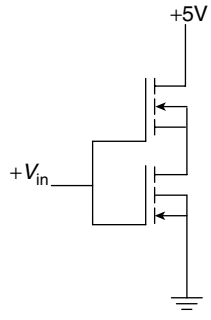
(A)



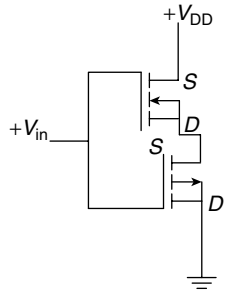
(B)



(C)

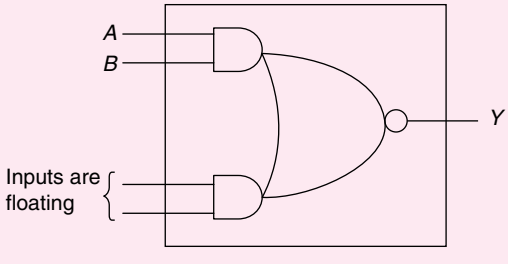


(D)



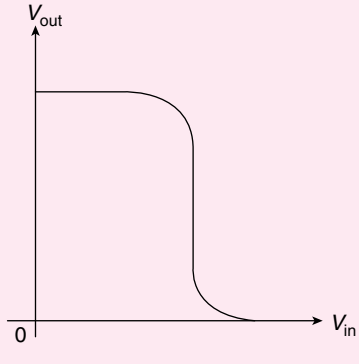
Previous Years' Questions

1. Figure shows the internal, schematic of a TTL AND–OR–Invert (AOI) gate. For the inputs shown in figure, the output Y is **[2004]**



(A) 0 (B) 1 (C) AB (D) $\overline{AB}$

2. Given figure is the voltage transfer characteristic of **[2004]**



(A) an NMOS inverter with enhancement mode transistors as load.
(B) an NMOS inverter with depletion mode transistor as load .
(C) a CMOS inverter.
(D) a BJT inverter.

3. The Boolean expression $AC + B\overline{C}$ is equivalent to **[2004]**

(A) $\overline{A}C + B\overline{C} + AC$
(B) $\overline{B}C + AC + B\overline{C} + \overline{A}C\overline{B}$
(C) $AC + B\overline{C} + \overline{B}C + ABC$
(D) $ABC + \overline{A}B\overline{C} + AB\overline{C} + A\overline{B}C$

4. The Boolean expression for the truth table shown is: **[2005]**

A	B	C	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

(A) $B(A+C)(\overline{A}+\overline{C})$
(B) $B(A+\overline{C})(\overline{A}+C)$
(C) $\overline{B}(A+\overline{C})(\overline{A}+C)$
(D) $\overline{B}(A+C)(\overline{A}+\overline{C})$

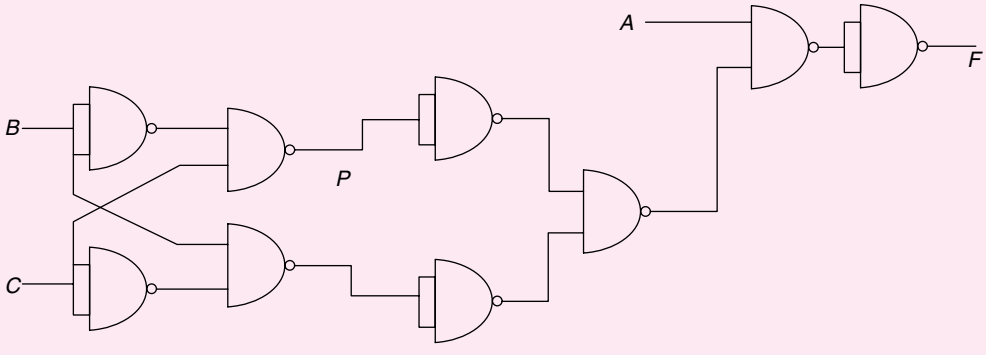
5. Find the number of product terms in the minimized sum-of-product expression obtained through the following K-map (where 'd' denotes don't care states) **[2006]**

1	0	0	1
0	d	0	0
0	0	d	1
1	0	0	1

(A) 2 (B) 3 (C) 4 (D) 5

6. The point P in the following figure is stuck at –1. The output f will be **[2006]**

(A) $\overline{AB\overline{C}}$ (B) $\overline{A}]$ (C) $AB\overline{C}$ (D) A



7. The Boolean function $Y = AB + CD$ is to be realized using only 2-input NAND gates. The minimum number of gates required is: **[2007]**

(A) 2 (B) 3 (C) 4 (D) 5

8. The Boolean expression $Y = \overline{A}\,\overline{B}\,\overline{C}\,D + \overline{A}\,B\,C\,\overline{D} + A\,\overline{B}\,\overline{C}\,D + A\,B\,\overline{C}\,\overline{D}$ can be minimized to **[2007]**

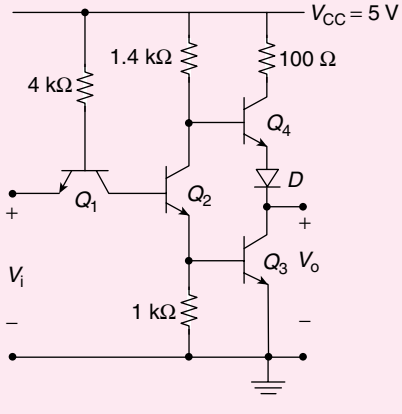
(A) $Y = \overline{A}\,\overline{B}\,\overline{C}\,D + \overline{A}\,B\,\overline{C} + A\,\overline{C}\,D$

(B) $Y = \overline{A}\,\overline{B}\,\overline{C}\,D + B\,C\,\overline{D}\,A\,\overline{B}\,\overline{C}\,D$

(C) $Y = \overline{A}\,B\,C\,\overline{D} + \overline{B}\,\overline{C}\,D + A\,\overline{B}\,\overline{C}\,D$

(D) $Y = \overline{A}\,B\,C\,\overline{D} + \overline{B}\,\overline{C}\,D + A\,B\,\overline{C}\,\overline{D}$

9. The circuit diagram of a standard TTL NOT gate is shown in the figure. When V_i = 2.5 V, the modes of operation of the transistors will be: **[2007]**



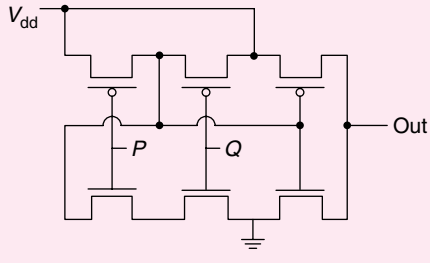
(A) Q_1: reverse active; Q_2: normal active; Q_3: saturation; Q_4: cut-off

(B) Q_1: reverse active; Q_2: saturation; Q_3: saturation; Q_4: cut-off

(C) Q_1: normal active; Q_2: cut-off; Q_3: cut–off; Q_4: saturation

(D) Q_1: saturation; Q_2: saturation; Q_3: saturation; Q_4: normal active

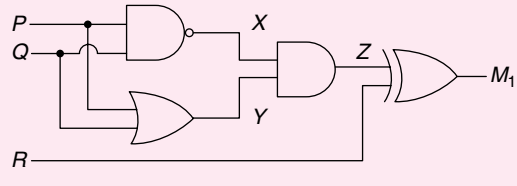
10. The logic function implemented by the following circuit at the terminal OUT is **[2008]**



(A) P NOR Q (B) P NAND Q

(C) P OR Q (D) P AND Q

11. Which of the following Boolean expression correctly represents the relation between P, Q, R, and M_1? **[2008]**



(A) $M_1 = (P \text{ OR } Q) \text{ XOR } R$

(B) $M_1 = (P \text{ AND } Q) \text{ XOR } R$

(C) $M_1 = (P \text{ NOR } Q) \text{ XOR } R$

(D) $M_1 = (P \text{ XOR } Q) \text{ XOR } R$

12. The full form of the abbreviations TTL and CMOS in reference to logic families are **[2009]**

(A) Triple Transistor Logic and Chip Metal Oxide Semiconductor

(B) Tristate Transistor Logic and Chip Metal Oxide Semiconductor

(C) Transistor Transistor Logic and Complementary Metal Oxide Semiconductor

(D) Tristate Transistor Logic and Complementary Metal Oxide Silicon

13. If $X = 1$ in the logic equation $\left[X + Y\left\{\overline{Y} + \left(\overline{Z} + X\overline{Y}\right)\right\}\right]\left\{\overline{X} + \overline{Z}\left(X + Y\right)\right\} = 1$, then **[2009]**

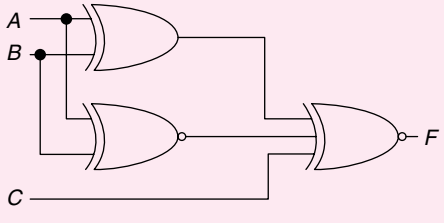
(A) $Y = Z$ (B) $Y = \overline{Z}$ (C) $Z = 1$ (D) $Z = 0$

14. Match the logic gates in Column A with their equivalents in Column B. **[2010]**

Column A	Column B
P	1
Q	2
R	3
S	4

(A) P–2, Q–4, R–1, S–3 (B) P–4, Q–2, R–1, S–3
(C) P–2, Q–4, R–3, S–1 (D) P–4, Q–2, R–3, S–1

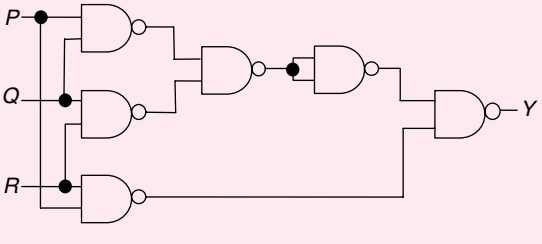
15. For the output F to be 1 in the logic circuit shown, the input combination should be



[2010]

(A) $A = 1, B = 1, C = 0$ (B) $A = 1, B = 0, C = 0$
(C) $A = 0, B = 1, C = 0$ (D) $A = 0, B = 0, C = 1$

16. The output Y in the following circuit is always '1' when **[2011]**

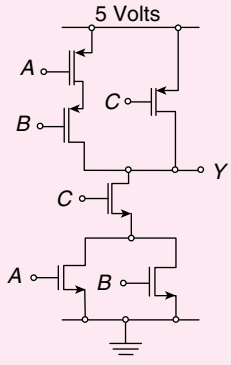


(A) two or more of the inputs P, Q, R are '0'
(B) two or more of the inputs P, Q, R are '1'
(C) any odd number of the inputs P, Q, R is '0'
(D) any odd number of the inputs P, Q, R is '1'

17. In the sum of products function $f(X, Y, Z) = \Sigma(2, 3, 4, 5)$, the prime implicants are **[2012]**

(A) $\bar{X}Y,\ X\bar{Y}$
(B) $\bar{X}Y, X\bar{Y}\,\bar{Z}, X\,\bar{Y}\ Z]$
(C) $\bar{X}\,Y\ \bar{Z}, \bar{X}\ YZ, X\bar{Y}$
(D) $\bar{X}\ Y\ \bar{Z}, \bar{X}\ Y\ Z,\ X\,\bar{Y}\,\bar{Z}, X\,\bar{Y}\ Z$

18. In the circuit shown **[2012]**

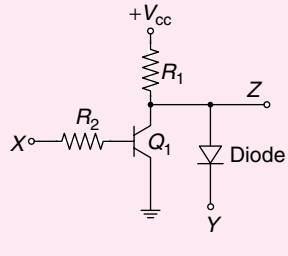


(A) $Y = \bar{A}\,\bar{B} + \bar{C}$ (B) $Y = (A + B)\,C$
(C) $Y = \left(\bar{A} + \bar{B}\right)\bar{C}$ (D) $Y = AB + C$

19. A bulb and a staircase has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches irrespective of the state of the other switch. The logic of switching of the bulb resembles **[2013]**

(A) an AND gate (B) an OR gate
(C) an XOR gate (D) a NAND gate

20. In the following circuit, Q_1 has negligible collector-to-emitter saturation voltage and the diode drops negligible voltage across it under forward bias. If V_{cc} is +5 V, X and Y are digital signals with 0 V as logic 0 and V_{cc} as logic 1, then the Boolean expression for Z is **[2013]**

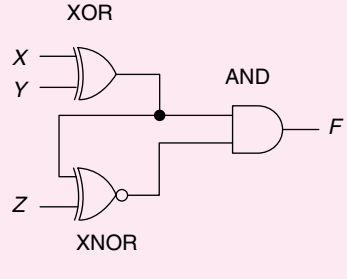


(A) XY (B) $\overline{XY}$ (C) $X\overline{Y}$ (D) $\overline{X\overline{Y}}$

21. The Boolean expression $(X + Y)(X + \bar{Y}) + \overline{\left(X\bar{Y}\right) + \bar{X}}$ simplifies to **[2014]**

(A) X (B) Y (C) XY (D) $X + Y$

22. The output F in the digital logic circuit shown in the figure is **[2014]**



(A) $F = \overline{X}YZ + X\overline{Y}Z$ (B) $F = \overline{X}Y\overline{Z} + X\overline{Y}\ \overline{Z}$

(C) $F = \overline{X}\ \overline{Y}\ Z + XYZ$ (D) $F = \overline{X}\ \overline{Y}\ \overline{Z} + XYZ$

23. Consider the Boolean function, $F(w, x, y, z) = wy + xy + \overline{w}xyz + \overline{w}\,\overline{x}\ y + xz + \overline{x}\ \overline{y}\,\overline{z}$. Which one of the following is the complete set of essential prime implicants? **[2014]**

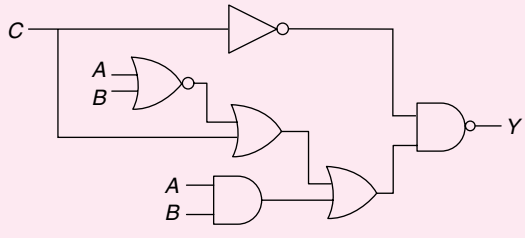
(A) $w, y, xz, \overline{x}\ \overline{z}$ (B) w, y, xz

(C) $y, \overline{x}\ \overline{y}\ \overline{z}$ (D) $y, xz, \overline{x}\ \overline{z}$

24. For an n-variable Boolean function, the maximum number of prime implicants is **[2014]**

(A) $2(n-1)$ (B) $n/2$ (C) 2^n (D) $2^{(n-1)}$

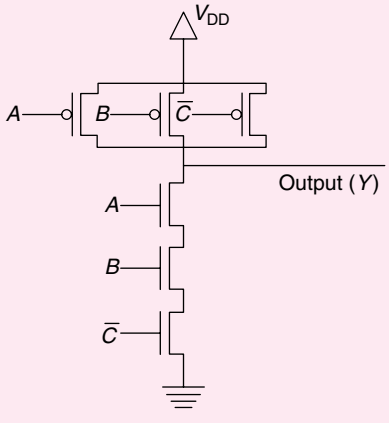
25. In the circuit shown in the figure, if $C = 0$, the expression for Y is **[2014]**



(A) $Y = A\overline{B} + \overline{A}B$ (B) $Y = A + B$

(C) $Y = \overline{A} + \overline{B}$ (D) $Y = AB$

26. Find the output (Y) of the circuit shown in the figure **[2014]**



(A) $\overline{A} + \overline{B} + C$ (B) $A + \overline{B} \bullet \overline{C} + A \bullet \overline{C}$

(C) $\overline{A} + B + \overline{C}$ (D) $A \bullet B \bullet \overline{C}$

27. The Boolean expression $F(X, Y, Z) = \overline{X}Y\overline{Z} + X\overline{Y}\overline{Z} + XY\overline{Z} + XYZ$ converted into the canonical product of sum (POS) form is **[2015]**

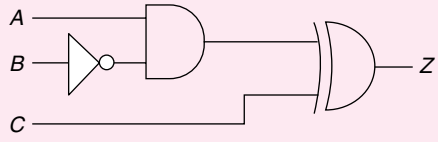
(A) $(X + Y + Z)(X + Y + \overline{Z})(\overline{X} + Y + \overline{Z})$

(B) $(X + \overline{Y} + Z)(\overline{X} + Y + \overline{Z})(\overline{X} + \overline{Y} + Z)(\overline{X} + \overline{Y} + \overline{Z})$

(C) $(X + Y + Z)(\overline{X} + Y + \overline{Z})(X + \overline{Y} + Z)(\overline{X} + \overline{Y} + \overline{Z})$

(D) $(X + \overline{Y} + \overline{Z})(\overline{X} + Y + Z)(\overline{X} + \overline{Y} + Z)(X + Y + Z)$

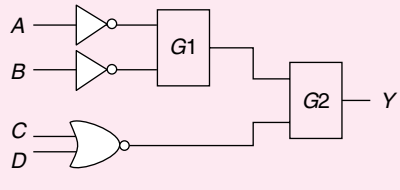
28. All the logic gates shown in the figure have propagation delay of 20 ns. Let $A = C = 0$ and $B = 1$ until time $t = 0$. At $t = 0$, all the inputs flip (i.e., $A = C = 1$ and $B = 0$) and remain in that state. For $t > 0$, output $Z = 1$ for a duration (in ns) of **[2015]**



29. A three-input majority gate is defined by the logic function $M(a, b, c) = ab + bc + ca$. Which one of the following gates is represented by the function $M\left(\overline{M(a,b,c)}, M\left(a,b,\overline{c}\right), c\right)$? **[2015]**

(A) three-input NAND gate
(B) three-input XOR gate
(C) three-input NOR gate
(D) three-input XNOR gate

30. In the figure shown, the output Y is required to be $Y = AB + \overline{C}\,\overline{D}$. The gates G1 and G2 must be, respectively. **[2015]**



(A) NOR, OR (B) OR, NAND

(C) NAND, OR (D) AND, NAND

31. A function of Boolean variables X, Y and Z is expressed in terms of the min-terms as

$$F(X, Y, Z) = \Sigma(1, 2, 5, 6, 7)$$

Which one of the product of sums given below is equal to the function $F(X, Y, Z)$? **[2015]**

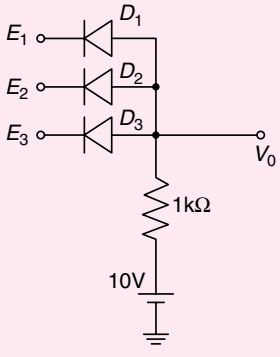
(A) $(\overline{X} + \overline{Y} + \overline{Z}).(\overline{X} + Y + Z).(X + \overline{Y} + \overline{Z})$

(B) $(X + Y + Z).(X + \overline{Y} + \overline{Z}).(\overline{X} + Y + Z)$

(C) $(\overline{X} + \overline{Y} + Z).(\overline{X} + Y + \overline{Z}).(X + \overline{Y} + Z).$
$(X + Y + \overline{Z}).(X + Y + Z)$

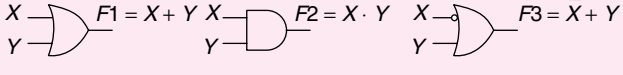
(D) $(X + Y + \overline{Z}).(\overline{X} + Y + Z).(\overline{X} + \overline{Y} + Z).$
$(\overline{X} + \overline{Y} + Z).(\overline{X} + \overline{Y} + \overline{Z})$

32. In the circuit shown, diodes D_1, D_2, and D_3 are ideal, and the inputs E_1, E_2, and E_3 are '0 V' for logic '0' and '10 V' for logic '1'. What logic gate does the circuit represent? **[2015]**



(A) 3-input OR gate (B) 3-input NOR gate
(C) 3-input AND gate (D) 3-input XOR gate

33. A universal logic gate can implement any Boolean function by connecting sufficient number of them appropriately. Three gates are shown. **[2015]**



Gate 1 Gate 2 Gate 3

Which one of the following statements is TRUE?
(A) Gate 1 is a universal gate.
(B) Gate 2 is a universal gate.
(C) Gate 3 is a universal gate.
(D) None of the gates shown in a universal gate.

34. Following is the k – map of a Boolean function of five variables P, Q, R, S and X. The minimum sum of product (SOP) expression for the function is: **[2016]**

X=0

RS \ PQ	00	01	11	10
00	0	0	0	0
01	1	0	0	1
11	1	0	0	1
10	0	0	0	0

X=1

RS \ PQ	00	01	11	10
00	0	1	1	0
01	0	0	0	0
11	0	0	0	0
10	0	1	1	0

(A) $\bar{P}\,\bar{Q}\,S\,\bar{X} + P\bar{Q}\,S\,\bar{X} + Q\bar{R}\,\bar{S}\,X + QR\,\bar{S}\,X$
(B) $\bar{Q}\,S\,\bar{X} + Q\,\bar{S}\,X$
(C) $\bar{Q}\,S\,X + Q\,\bar{S}\,\bar{X}$
(D) $\bar{Q}\,S + Q\bar{S}$

Answer Keys

Exercises

Practice Problems 1

1. B	**2.** D	**3.** B	**4.** C	**5.** A	**6.** A	**7.** B	**8.** A	**9.** B	**10.** A
11. C	**12.** D	**13.** A	**14.** A	**15.** A	**16.** A	**17.** D	**18.** B	**19.** A	**20.** D
21. D	**22.** C	**23.** A	**24.** C	**25.** D	**26.** D	**27.** D	**28.** A	**29.** A	**30.** B
31. D	**32.** C	**33.** B							

Practice Problems 2

1. D	**2.** D	**3.** D	**4.** C	**5.** A	**6.** C	**7.** B	**8.** D	**9.** A	**10.** C
11. A	**12.** D	**13.** A	**14.** A	**15.** A	**16.** C	**17.** C	**18.** C	**19.** C	**20.** D
21. D	**22.** C	**23.** C	**24.** B	**25.** B	**26.** A	**27.** C	**28.** D	**29.** A	**30.** C
31. B	**32.** C	**33.** A							

Previous Years' Questions

1. A	**2.** C	**3.** D	**4.** A	**5.** A	**6.** D	**7.** B	**8.** D	**9.** A	**10.** D
11. D	**12.** C	**13.** D	**14.** D	**15.** D	**16.** B	**17.** A	**18.** A	**19.** C	**20.** B
21. A	**22.** A	**23.** D	**24.** D	**25.** A	**26.** A	**27.** A	**28.** 40	**29.** B	**30.** A
31. B	**32.** C	**33.** C	**34.** B						