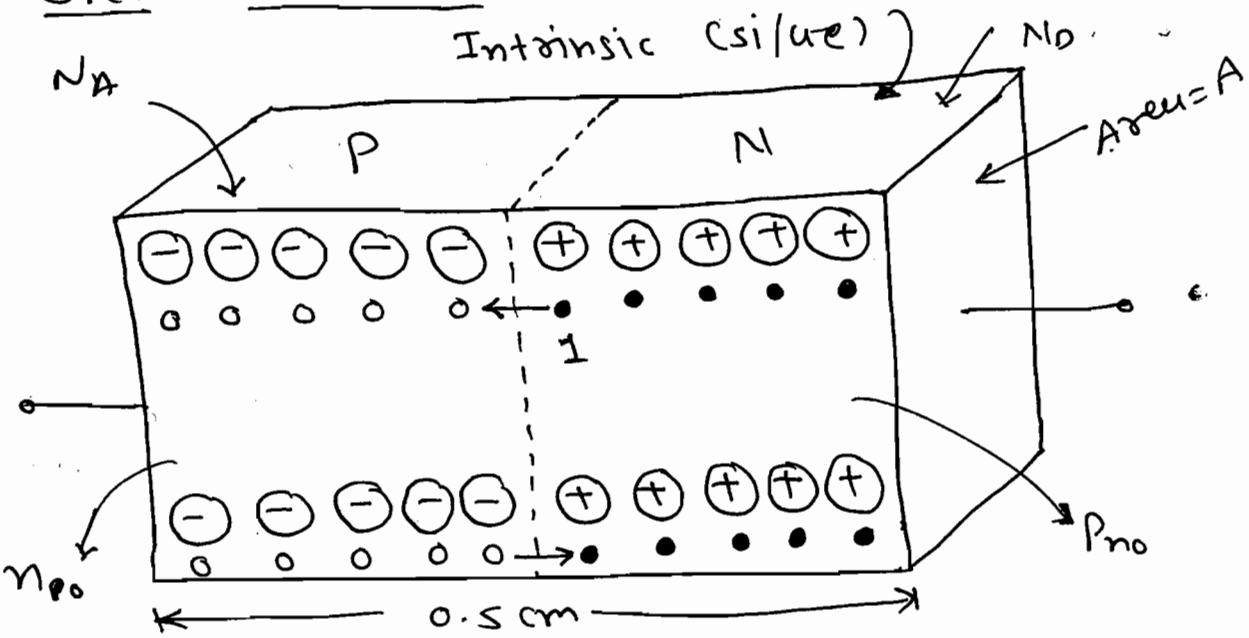
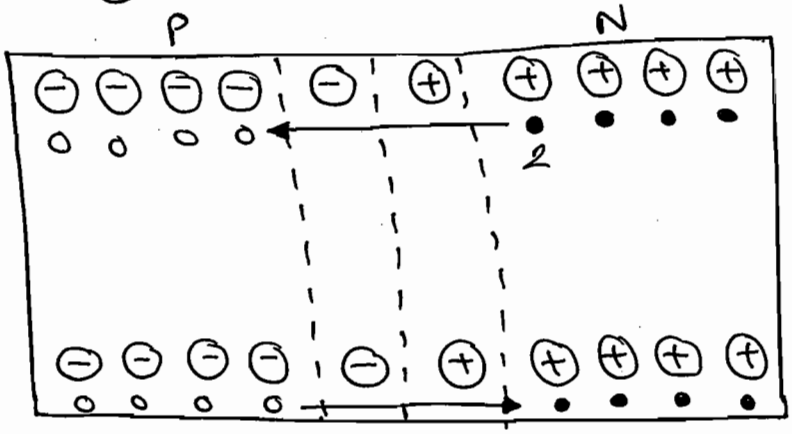
✡ P-N Junction Diode:

✱ Open circuited P-N ~~Junction~~ Diode:

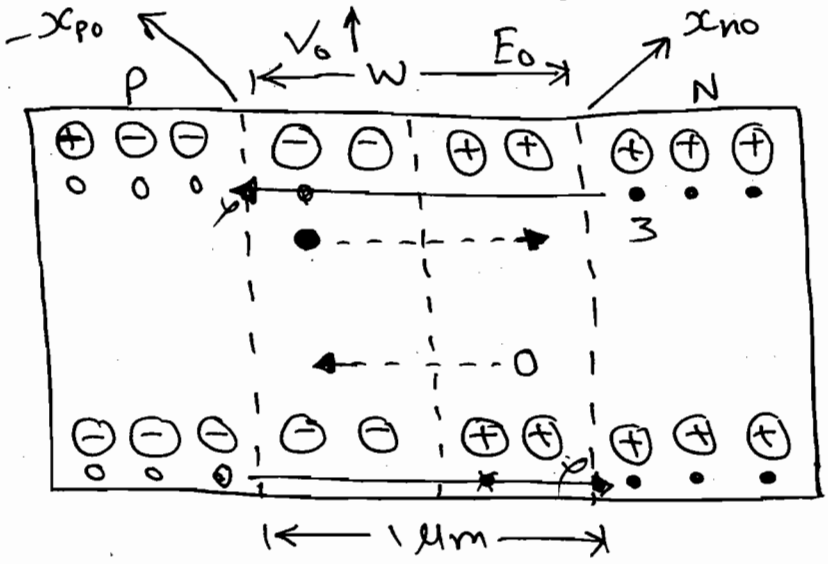


(A) Without Barrier.



(B)

DR | SCR | TR (I.I)



(C) With Barrier.

n_{po}, p_{no} : Initial thermally generated minority carrier concentration.

⊕. : Donor atom with excess electron (Nutral).

⊕ : Donor Ion (+ve charge).

• : Excess electron.

⊖$_o$: Acceptor atom with excess hole. (Nutral).

⊖ : Acceptor Ion (-ve charge).

○ : Excess Hole.

⇒ Fig- Ⓐ shows internal structure of an open circuited P-N Diode which is just then created.

* First explanation for formation of barrier.

⇒ In fig - Ⓐ due to difference in Concentration diffusion of charge Carriers start. Hence EHP recombination occurs hence +ve & -ve ions get created at centre hence fig- Ⓐ becomes Ⓑ. In fig- Ⓑ Past diffusion Opposites Present diffusion Indirectly. Though opposition exist since Concentration gradient of charge carrier is large

with difficulty diffusion may continue. Hence again recombination occurs and again Ions get created. Hence fig-(B) becomes (C). As diffusion continues opposition to further diffusion increases. Hence after some time diffusion comes to halt. (fig-(C)).

→ The central +ve & -ve immobile ions (I.I) opposse diffusion hence called barrier. The size of barrier (1μm) is very small compare to size of diode (0.5cm). Barrier is not having charge carriers. & hence called depletion region (D.R). Barrier is the only region having Ions hence called space charge region (SCR). Barrier is separating two Nutral areas hence called Transition region (T.R).

→ W : width of depletion region

x_{no}, x_{po} : Penetration of depletion region into n, p sides.

→ From fig-(C) $\boxed{W = x_{no} - (-x_{po}) = x_{no} + x_{po}}$ —(1)

⇒ Two Electrodes

DIODE

* Application:

① Switch.

② Voltage Variable Capacitor.

→ Barrier opposes the flow of majority carriers but supports the flow of minority carriers

* Direction of Flow of charge carrier. | Type of Current | Direction of current.

⇒ ← | e^- diffusion | → (X)

⇒ → | Hole diffusion | → (X)

⇒ - - - - -> | e^- DRIFT | <- - - - - (Y)

⇒ <- - - - - | Hole DRIFT | <- - - - - (Y)

⇒ Majority Carrier gives diffusion current (Solid line).

⇒ Minority carriers give drift current (dotted line).

→ X : Net diffusion current (e^- + hole diffusion).

→ Y : Net Drift current (e^- + hole drift).

→ Z : Net current = X − Y.

* Second explanation for formation of Barrier:

⇒ Drift current opposses diffusion current But if drift less than diffusion, diffusion continuous. If diffusion continuous then EHP recombination occurs and ions get created at centre which attract minority carrier and increases drift current. As long as drift is less than diffusion, diffusion continuous. As long as diffusion continuous, drift goes on increases. At some time drift and diffusion become equal in magnitude but since opposite in diction net current becomes zero. i.e. diffusion comes to a halt. (fig ⓒ).

→ Accross +ve and -ve ions existing inside depletion region internally electric flux lines get developed which induced a voltage V_0 (or) electric field E_0 which are responsible for drift current.

→ Open circuited Contact Potential,

$$V_0 = KT \ln (N_D N_A / n_i^2) \text{ (V)} \quad \text{---} (2).$$

→ Open circuited electric field intensity,

$$E_0 = -\frac{qN_D x_{no}}{\epsilon} = -\frac{qN_A \cdot x_{po}}{\epsilon} \text{ (V/m)} \quad (3).$$

⇒ Total -ve charges last in the depletion region of n-side is equal to total +ve charges lost in the depletion region of P-side.

$$N_D x_{no} A\!\!\!/ \ell\!\!\!/ = N_A x_{po} A\!\!\!/ \ell\!\!\!/.$$

$$\Rightarrow \boxed{N_D x_{no} = N_A \cdot x_{po}} \quad \text{---} (4).$$

$$\Rightarrow \boxed{x_{no} = \frac{\omega N_A}{N_D + N_A}} \quad \text{---} (5) \qquad \boxed{x_{po} = \frac{\omega N_D}{N_D + N_A}} \quad \text{---} (6)$$

$$\Rightarrow \boxed{W = \sqrt{\frac{2\epsilon V_B}{q}\left[\frac{1}{N_D} + \frac{1}{N_A}\right]}} \quad -(7).$$

$\Rightarrow$ Penetration of depletion region into n-side is proportional to dopping of p-side. and vice-versa.

$V_B = V_0 - V$ (+ve $\rightarrow$ F.B., -ve $\rightarrow$ R.B.)

V_0 : Built in Potential (or) Barrier (or) Contact Pot.

V : applied Voltage

Note - (1):

$\Rightarrow$ Depletion region penetrates equally into n- & p-sides for equal doppings & it penetrates unequally for unequal doppings.

$N_D = N_A \longrightarrow x_{no} = x_{po}$.

$N_D \neq N_A \longrightarrow x_{no} \neq x_{po}$.

Note - (2):

$\Rightarrow$ Depletion region penetrates more into lightly dopped side.

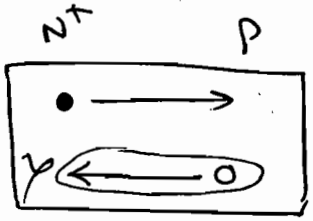
$N_D > N_A \longrightarrow x_{po} > x_{no}$.

Note - (3)

$\Rightarrow$ penetration of depletion region into heavily dopped side of a single sided (or) one sided diode can

be neglected.

→ In one sided diode, one side is heavily dopped compared to other side hence most of the current is given by only one side. i.e. heavily dopped side.

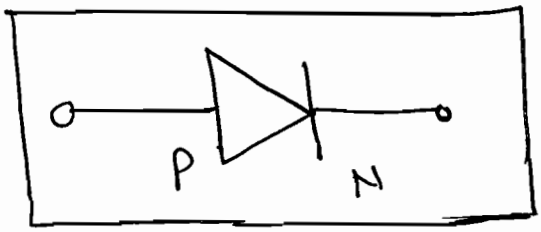
→ 

$$x_{p0} = \frac{W N_D}{N_D + N_A} \simeq W$$

$N_D >> N_A$

$W = x_{n0} + x_{p0}$

→ $\boxed{x_{n0} \simeq 0}$

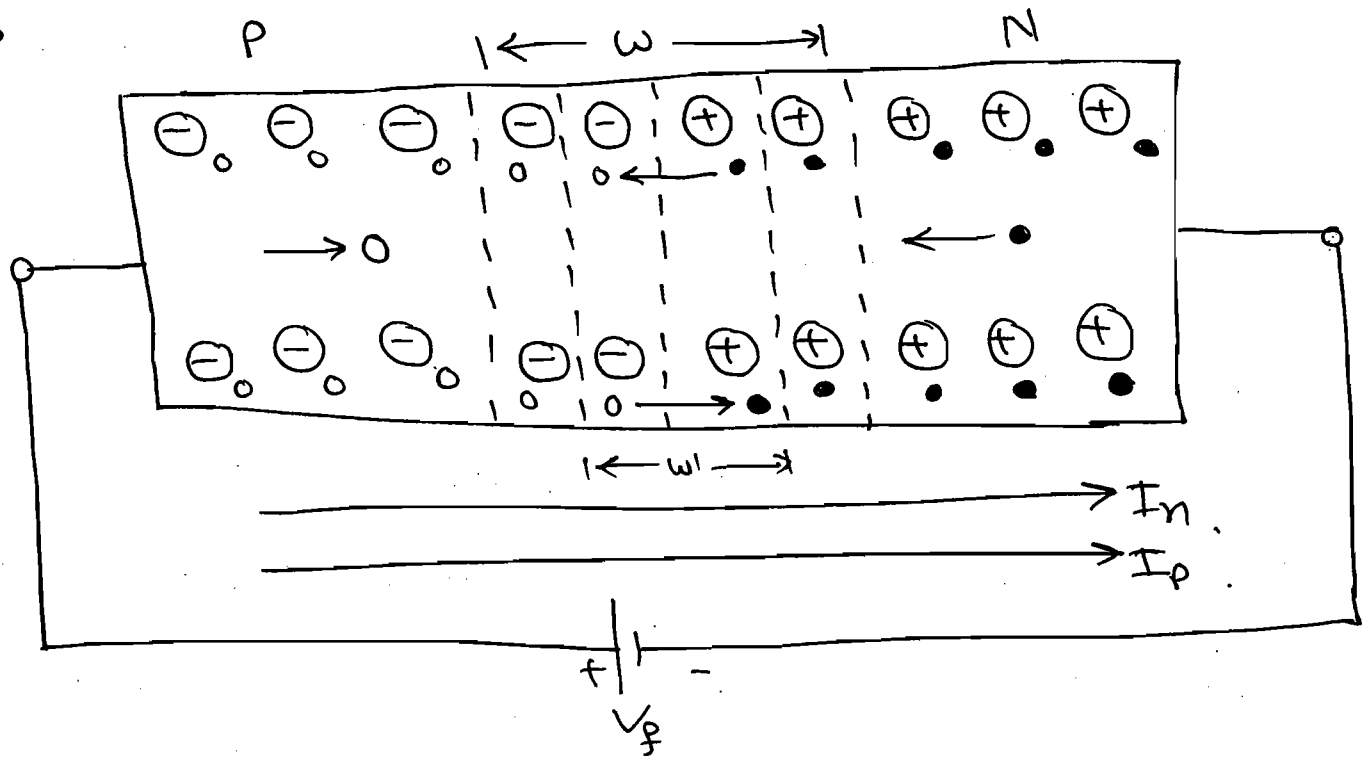
→ 

→ A circuit symbol should identify the no. of terminals and names of terminal.

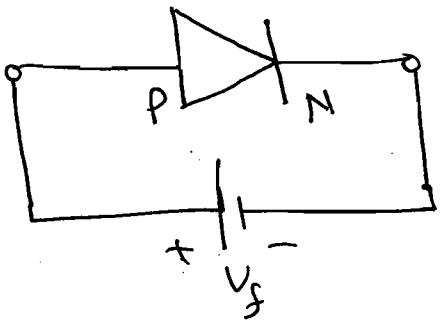
→ Vertical line represents N, triangular place represent P. The direction of arrow shows the direction of current when the diode is forward biased.

* Forward Biased:

=>



=>



=> If the Voltage given to p-side is more positive than n-side then diode is said to be Forward biased.

=> Due to Polarities of forward biased Charge carriers get repplied and entre into open circuited depletion region due to which immobile ions get back their lost charge carriers become nutral and move to undepleted

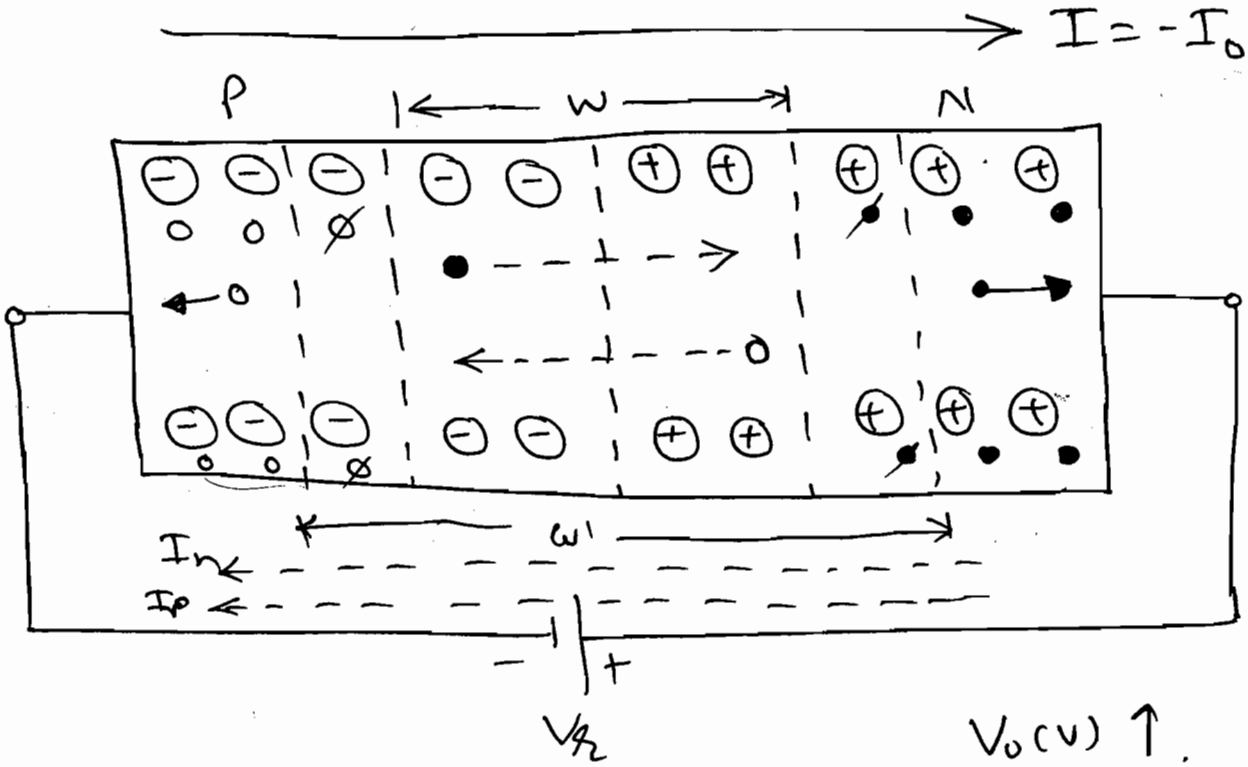
region hence width of depletion region decreases (W') compared to open circuit (W). Due to decrease in ions V_0 (V) and E_0 (eV) decrease by V_γ.

⇒ Cut-in Voltage (or) Offset Voltage (or) break-point Voltage (or) threshold Voltage (or) firing point Voltage V_γ is defined as minimum forward bias to be given across a P-N junction for current to exist.

⇒ Majority Carrier diffusion supports flow of currents. Hence magnitude of current is large i.e (mA (or) A) and the direction is from P to N.

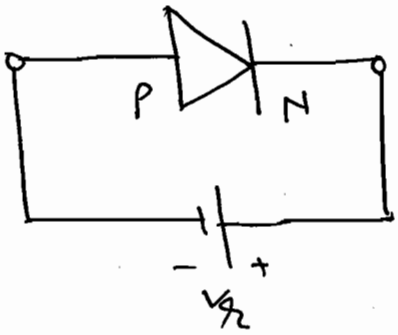
⇒ To the left and right drift current exist. To the centre diffusion current exist. But diffusion is important. Using which central barrier can be crossed which was opposing current in open circuit case.

* Reverse Biased:



$V_0(V) \uparrow$.

$E_0(V) \uparrow$.



⇒ Due to Polarities of reverse biased natural atoms adjusted to open circuited depl region loose charge carriers become immobile ions and move to depletion region hence width of depletion region increases (W') compared to open circuit (W).

⇒ Due to increase in Ions V_0 (Volts) and E_0 (eV) increase by V_R.

→ Minority Carrier drift Support flow of current hence less current, μA for Ge and nA for Si flows. Direction is N to P.

→ Increase in reverse bias, increases width of depletion region but thermally generated minority carriers are Constant. Hence, reverse current is independent of reverse Voltage called <u>Reverse Saturation current I_o</u>. i.e.

$$\frac{dI_o}{dV} = 0.$$

→ I_o physically flows from N-to-P but shown P-N. hence negative.

⇒ Increase in temp. increases EHP generation and minority Concentration hence I_o increases. i.e.

$$\frac{dI_o}{dT} > 0$$

* Volt - Ampere (V-I) characteristics:

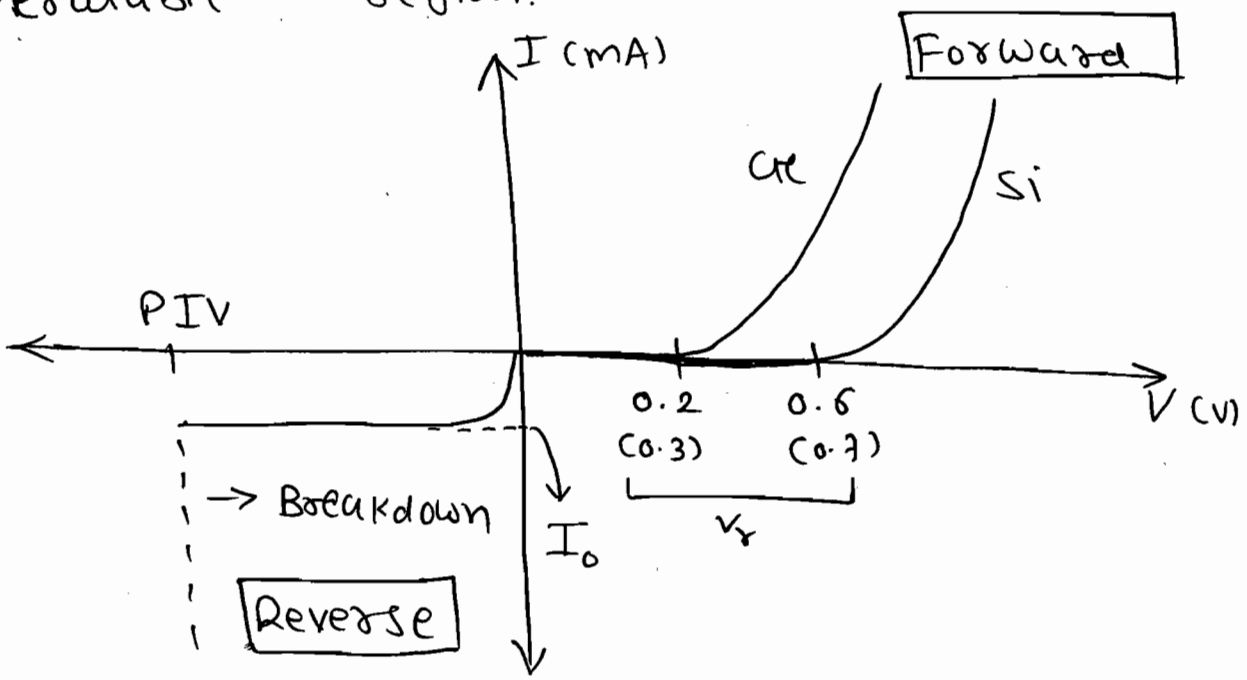
⇒ I is defined as current flowing through the diode from P- to N.

⇒ V is defined as Voltage across terminals of Diode with positive at P side.

⇒ Peak - Inverse Voltage (P_{IV}) is defined as maximum reverse bias that can be safely applied across a P-N diode.

⇒ Dotted line in the graph is non-operatable region.

⇒

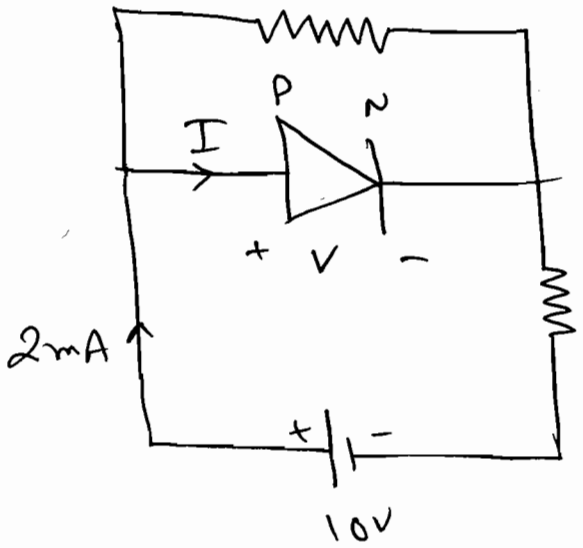


⇒ $$I = I_0 \left(e^{V/\eta V_T} - 1 \right).$$

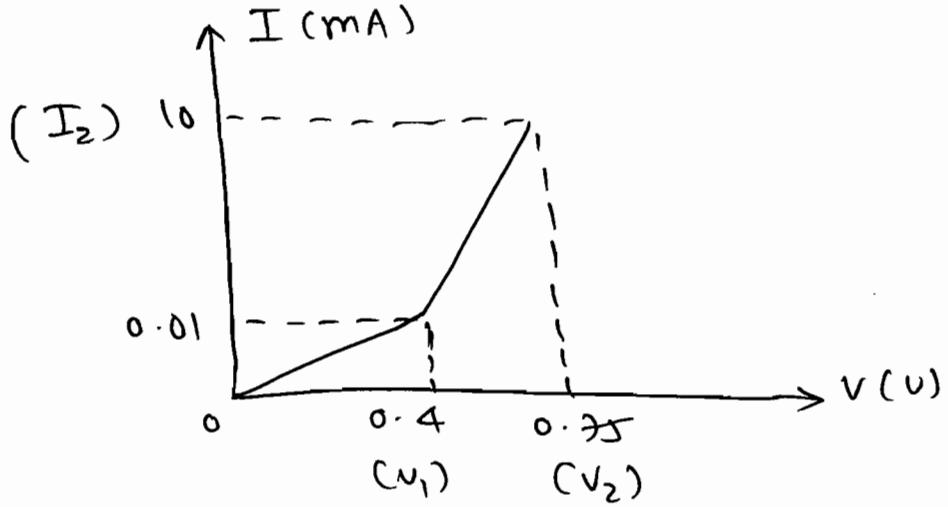
$\eta = 1$ Ge.
$= 2$ Si.

FB : V = +ve : If $e^{V/nV_T} >> 1$ Then $I = I_0 e^{V/nV_T}$

RB : V = -ve : if $e^{V/nV_T} << 1$ then $I = -I_0$.



Q Given V-I characteristics of P-N Diode. Comment on weither it is Si or ge Diode?



Soln: Current eqn of diode is modified to a ratio

$$\frac{I_2}{I_1} = \frac{I_0 \left(e^{V_2/nV_T} - 1\right)}{I_0 \left(e^{V_1/nV_T} - 1\right)}.$$

$$\therefore \frac{10}{0.01} = \frac{e^{V_2/\eta V_T}}{e^{V_1/\eta V_T}} \quad (\because \text{neglect } -1)$$

$$\therefore 1000 = e^{\frac{(V_2 - V_1)}{\eta V_T}}$$

$$\therefore 1000 = e^{\frac{0.35}{\eta \times V_T}}$$

$$\therefore 6.9 = 0.35 \times \frac{1}{\eta \times 0.026}$$

$$\eta = \frac{13.46}{6.9}$$

$$\therefore \boxed{\eta = 1.95} \approx 2 \text{ is matches for silicon.}$$

So, Diode is made up of silicon.

Note:

→ For Practical application ~~is preferred~~ Si diode is preferred than ge diode due to following reason.

① I_0 of Ge (μA) > I_0 of Si (nA)

→ Hence si diode act as better switch.

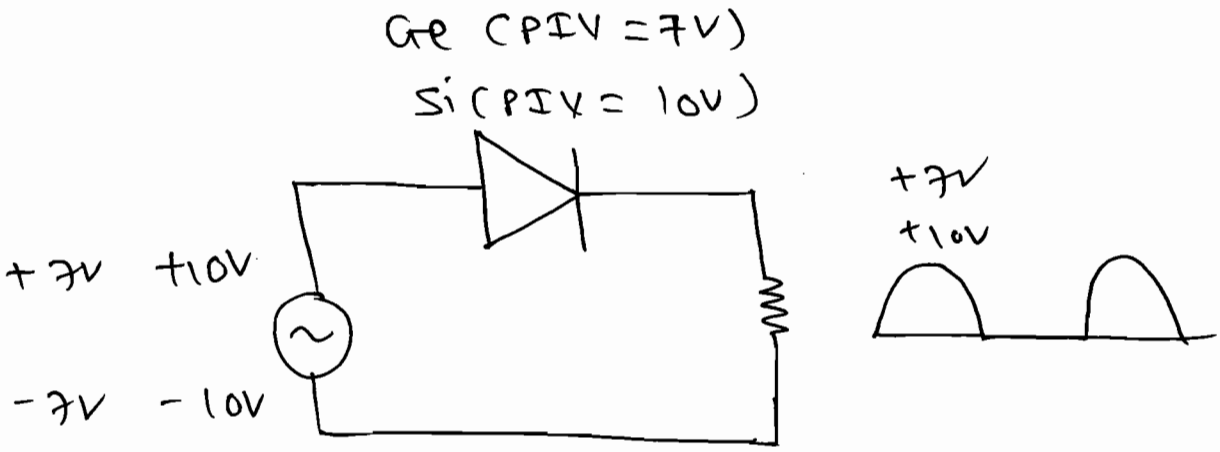
② E_g of Ge < Si.

→ Hence, si diode gives better operatable thermal range.

	Switch	
	Ge	Si
300 k :	✓	✓
400 k :	X	✓
500 k :	X	X

③ PIV of Ge < silicon.

→ Hence, Si diode gives better operatable range.



④ For Si Diode abundant raw material available.

→ Reasons ①, ② & ③ are called primary reason and ④ is secondary reason.

→ The above explanation is valid for any electronic device as specially high power devices like SCR, DIAC, TRIAC etc. Will be made up of Si since Si can withstand higher temp.

* Diode Resistances:

→ DC (or) Static Resistance,

$$R_{DC} = \frac{V}{I}$$

→ Ac (or) Dynamic Resistance,

→ $r_{ac} = \frac{dV}{dI} = \frac{1}{\text{TAN}\,\theta} = \frac{1}{\tan\theta}$.

→ $r_{ac} = (\eta V_T / I)$ ⟶ For F.B. only.

$r_{ac} = \frac{\eta V_T}{I_0} \cdot e^{-V/\eta V_T}$ ⟶ (For F.B & V = +ve, R.B. V = -ve)

Q A ge diode has $I_0 = 30\mu A$ at 125°C. Find dynamic resistance under. Pass

(i) Forward biased of 0.2 V.

(ii) Reverse biased of 0.2 V.

Soln:

$$r_{ac} = \frac{\eta V_T}{I_0} \cdot e^{-V/\eta V_T}$$

$\eta = 1$, ~~$V_T = 0.026$~~ , $I_0 = 30\mu A$

Note: $V_T = 0.026$ V is valid only at 27°C. At 125°C $V_T = \frac{T°K}{11,600}$

$$\therefore \quad V_T = \frac{273 + 125}{11,600}$$

$$V_T = 0.0343 \text{ V}$$

(i) $V = +0.2\text{V}$

$$R_{acf} = \frac{\eta V_T}{I_0} \cdot e^{\frac{V}{-\eta V_T}}$$

$$= \frac{1 \times 0.0343}{30 \times 10^{-6}} \cdot e^{-\frac{0.2}{1 \times 0.0343}}$$

$$\boxed{R_{acf} = 3.356\ \Omega}$$

(ii) $V = -0.2\text{ V}$.

Remember

$$\therefore \quad R_{acr} = \frac{1 \times 0.0343}{30 \times 10^{-6}} \cdot e^{\frac{0.2}{1 \times 0.0343}}$$

$$\boxed{R_{acr} = 3.89 \times 10^5\ \Omega}$$

$$\therefore \boxed{R_{acr} = 389.5\ \text{K}\Omega}$$

Q The reverse biased saturation current of a silicon P-N diode is 1 μA. determine its a.c. resistance if 0.4 V of forward biase is applied.

Soln:

$$R_{ac} = \frac{\eta V_T}{I}$$

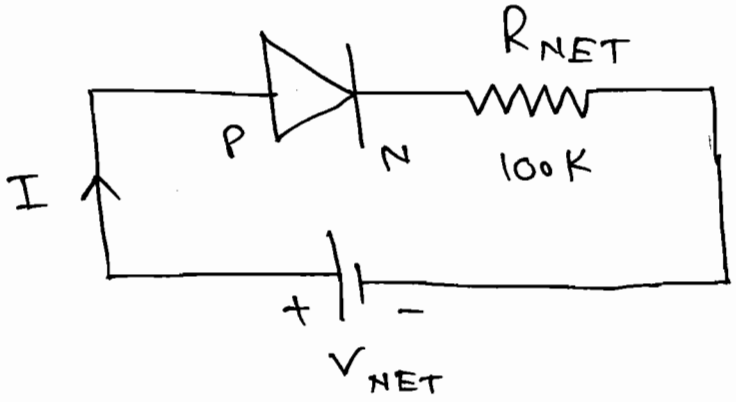
$$\Rightarrow R_{ac} = \frac{n V_T}{I_0 \left(e^{V/nV_T} - 1\right)}$$

$$= \frac{2 \times 0.026}{10^{-6} \times \left(e^{\frac{0.4}{2 \times 0.026}} - 1\right)}$$

$$\therefore \boxed{R_{ac} = 23.74\ \Omega}$$

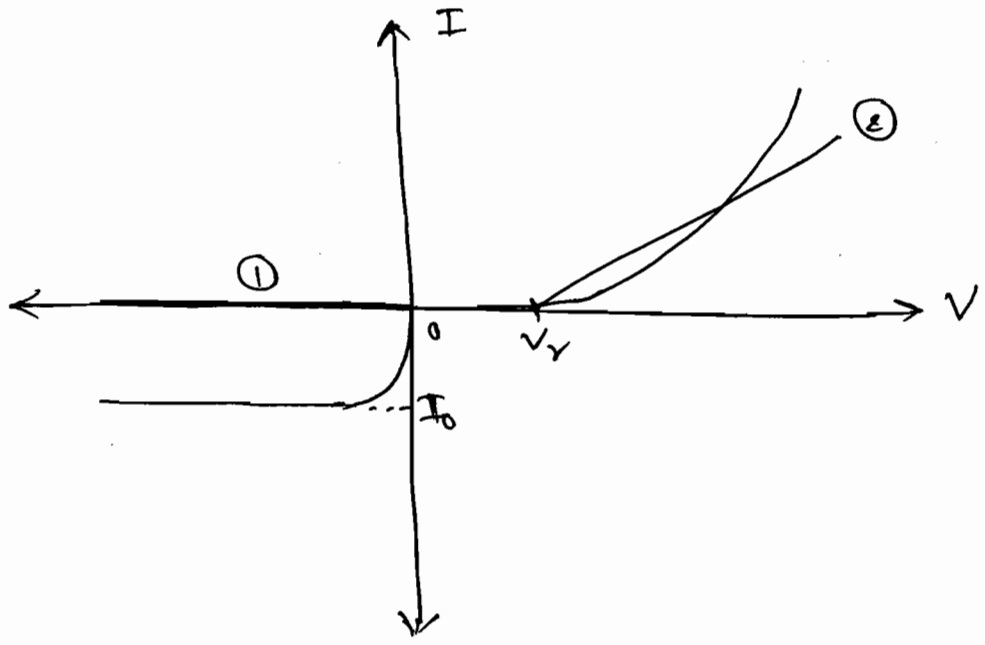
* Equivalent circuit:

⇒



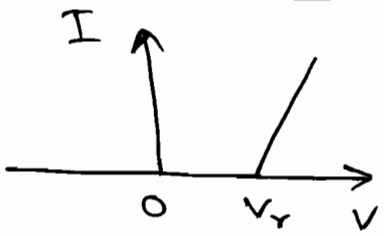
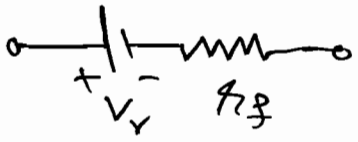
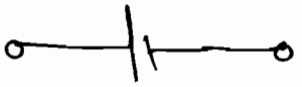
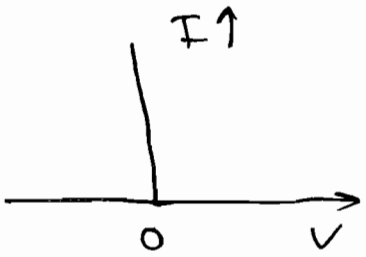
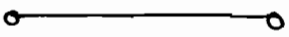
⇒ R_{NET}, V_{NET} : Resistance, Voltage of a N/W.

⇒



V vs I

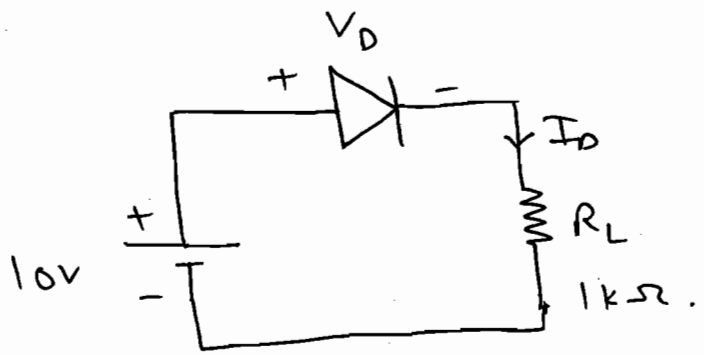
*

Name	Characteristics	equivalent Ckt	Condⁿ
① Piecewise Linear model			~~$R_{NET} \gg r_f$~~
② Simplified piecewise linear model			$R_{NET.} \gg r_f$
③ Ideal model			$R_{NET.} \gg r_f$ $V_{NET.} \gg V_r$

⇒ In the above equivalent ckt +ve of V_r should match with P-side of diode.

⇒ The above eqⁿ ckt are valid only for forward biased diode for a reverse bias diode eqⁿ ckt in all the three model is open ckt.

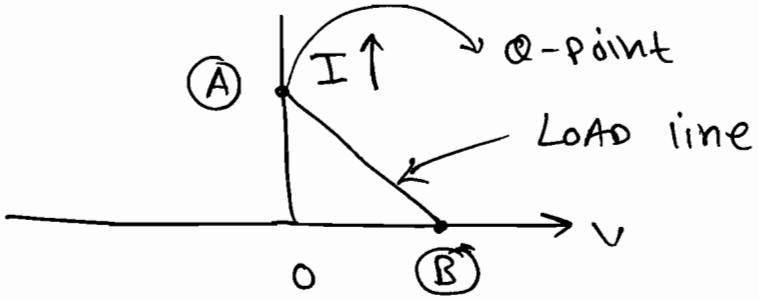
[a] Determine Q-point in the given ckt. Assume ideal diode.



Soln:

Note:

→ Q-point is defined as intersection of load line with V-I chara.



By KVL,

$\therefore \quad 10 = V_D + 1000\, I_D.$

→ $V_D = 0$

So, $10 = 0 + 1000\, I_D$

$$\boxed{I_D = 10mA} \quad (:A).$$

→ $I_D = 0.$

So, $\boxed{V_D = 10V} \quad (:B).$

⇒ Slope of AB line is controlled by load R/k R_L. hence called load line.

Q-Point $= (V_{DQ}, I_{DQ}) = (0, 10mA).$

Q) A diode whose V-I characteristics as shown in fig-a is connected as in fig-b calculate I'.

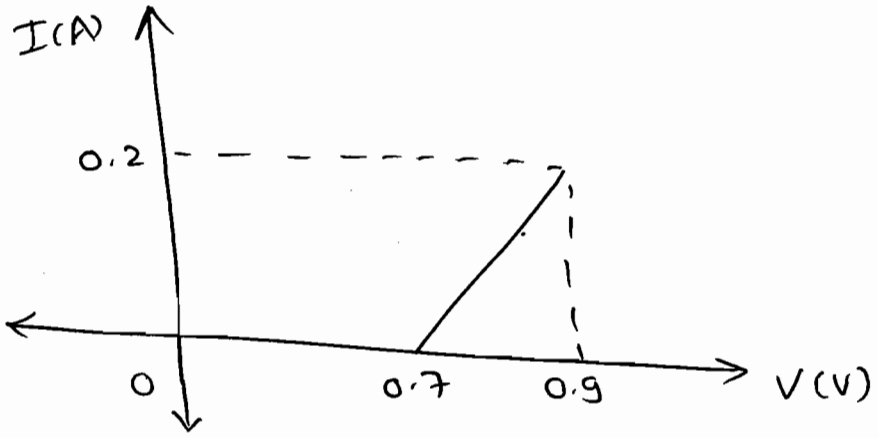
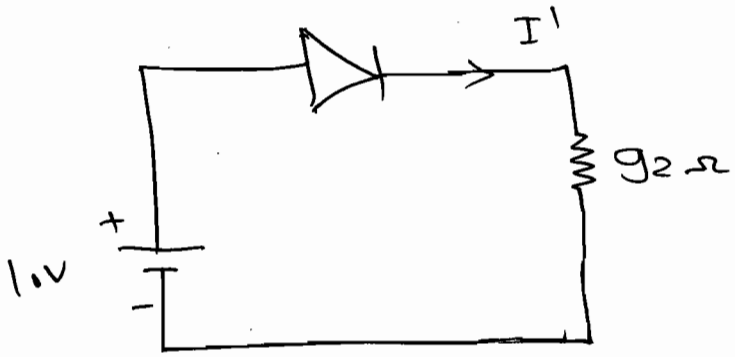


fig-(a)

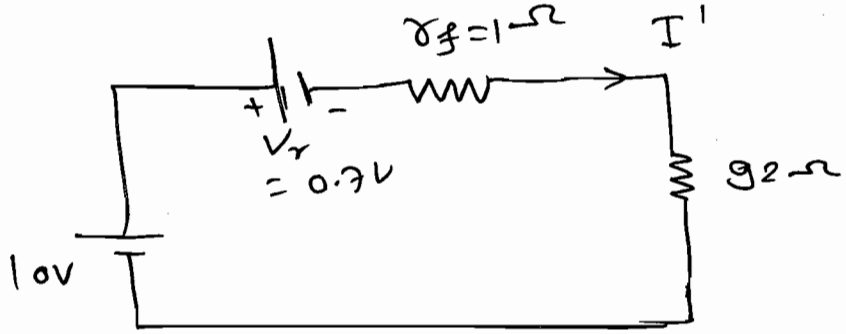


Soln:

$V_\gamma = 0.7\ V$

$$R_f = \frac{(0.9 - 0.7)\ V}{(0.2 - 0)\ A} = \frac{0.2}{0.2} = 1\ \Omega.$$

eqn ckt:



By KVL, $10 - 0.7 = I'(1 + 92)$.

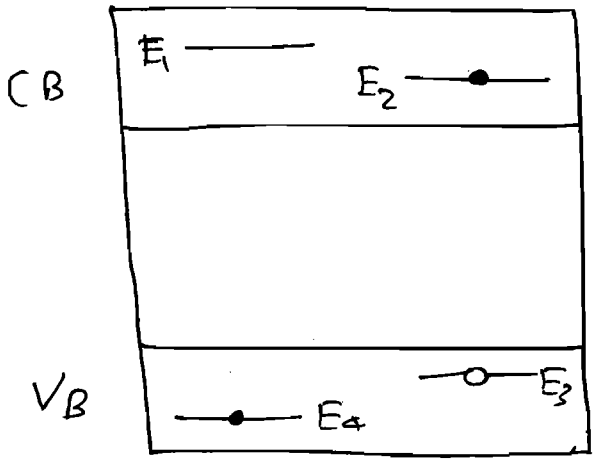
$$\therefore I' = 9.3/93 = 0.1\ A$$

$I' = 0.1A$

* Fermi level:

⇒ Existing electron in conduction band and non-existing electron in valance band both can support current. Hence to comment on conductivity of a semiconductor we should be able to know the existance (or) non-existance of electron at a given energy level. To comment on this, Fermi diruct distribution (or) Fermi dirac probability distribution is define as.

$$f(E) = \frac{1}{1 + e^{(E-E_F)/KT}} \quad \text{——— (1)}.$$



$f(E_1) = 0.$

$f(E_2) = 1.$

$f(E_3) = 0.$

$f(E_4) = 1.$

⇒ $f(E)$ Probability of existance of electron at an allowed energy level E

$(0 \leq f(E) \leq 1)$.

→ E_F : Fermi energy level (imaginary).

Comments on 50% occupancy.

→ K : Boltzman constant in eV/°K.

T : Temp. in °K.

* Fermi level in Intrinsic semiconductor

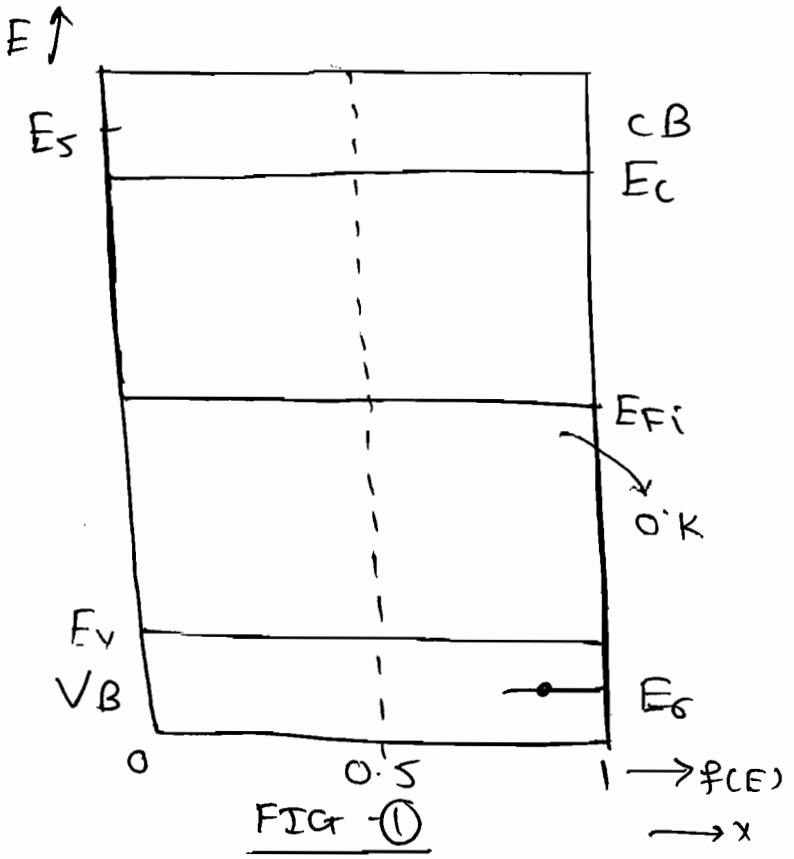


FIG - ①

⇒ $T = 0°k$

$E > E_F \longrightarrow f(E) = \frac{1}{1+e^{+\infty}} = 0.$

$E < E_F \longrightarrow f(E) = \frac{1}{1+e^{-\infty}} = 1.$

⇒ $T \neq 0°k$

$E = E_F \longrightarrow f(E) = \frac{1}{1+e^{0}} = \frac{1}{2}$ (OR) 50%

→ At 300°k EHP generation occurs and electron goes to conduction band leaving a hole in valance band as in fig-②

⇒

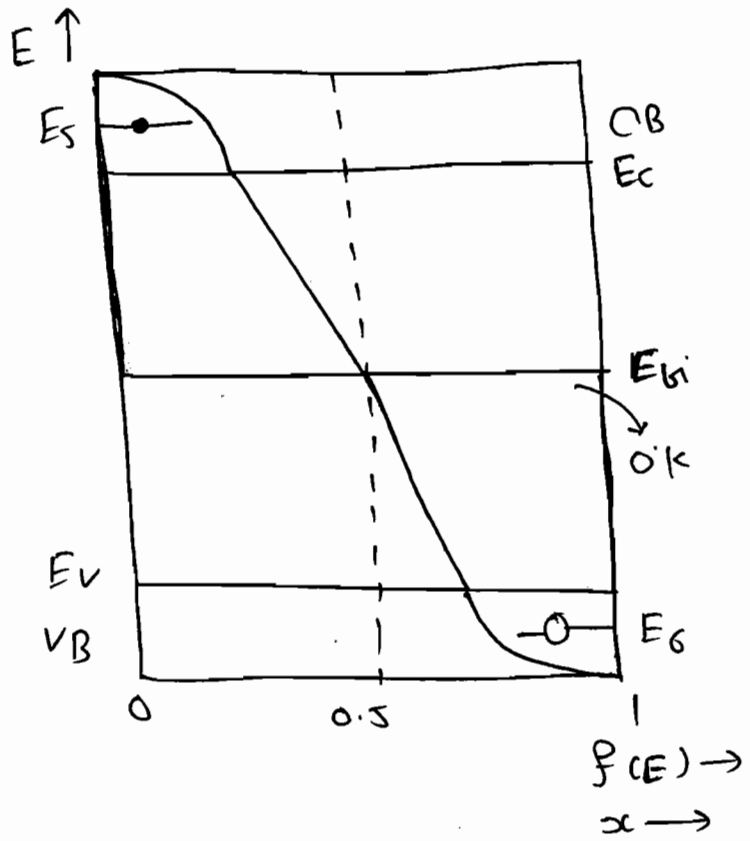


Fig-②

→ By integrating f(E) fⁿ along with other term with $E > E_C$ we get free electron concentration n

$$n = N_C \, e^{-(E_C - E_F)/kT} \quad \text{——— ②}$$

where

$$N_C = 2 (2\pi m_n \bar{K} T / h^2)^{3/2}$$

$$= 4.8 \times 10^{15} (m_n T / m)^{3/2} \ cm^{-3} \quad \text{— ③}$$

→ $1 - f(E)$ is Prob. of non existance of electron at an energy level E in conduction band (or) valance band. It is also prob. of existance of hole at an energy level E in valance band only.

⇒ By integrating $1 - f(E)$ b^n along with some other terms with $E \leq E_V$ we get hole concentration p,

→ $$p = N_V \cdot e^{-(E_F - E_V)/kT} \quad \text{——— (4)}$$

→ $$N_V = 2 (2\pi m_p kT / h^2)^{3/2}$$

$$= 4.82 \times 10^{15} (m_p T/m)^{3/2} \ cm^{-3} \quad \text{— (5).}$$

→ N_c, N_v : Densities of energy states, at Conduction, valance Band. They are Constants. dependent on temp. and independent of dopping.

→ m_n, m_p : effective mass of electron, hole.

→ m : mass of electron.

→ k : Boltzman constant in eV/°K.

→ $\bar{k}$: Boltzman constant in J/°K.

→ T : Temp. in °K.

→ h : plank's Constant.

⇒ For intrinsic semiconductor $n = p$. Substitute in (2) & (4) we get,

$$E_{Fi} = \left(\frac{E_c + E_v}{2}\right) - \frac{KT}{2} \ln\left(\frac{N_c}{N_v}\right) \quad \text{— (6)}$$

⇒ If $m_n = m_p$, then

$$E_{fi} = \frac{(E_c + E_v)}{2} \quad \text{——— (7)}$$

i.e. intrinsic fermi level lies at the centre of forbidden band if $m_n = m_p$.

→ It lies above (0/) below the centre if $m_n \neq m_p$.

→ Substituting (2) & (4) in +/(2), to $n \cdot p = n_i^2$ we get.

→ $$E_G = KT \ln\left(\frac{N_C \cdot N_V}{n_i^2}\right) \quad \text{— (8)}$$

* Fermi level in Extrinsic Semiconductor

→ At room temp. probability of existance of electron in conduction band of n-type semiconductor is more than prob. of existance of electron in Conduction band of intrinsic Semi-Conductor. Hence, fermi level moves closer to Conduction band in n-type then intrinsic.

⇒ For n-type Semiconductor $n_n \simeq N_D$.

from eqn - (2)

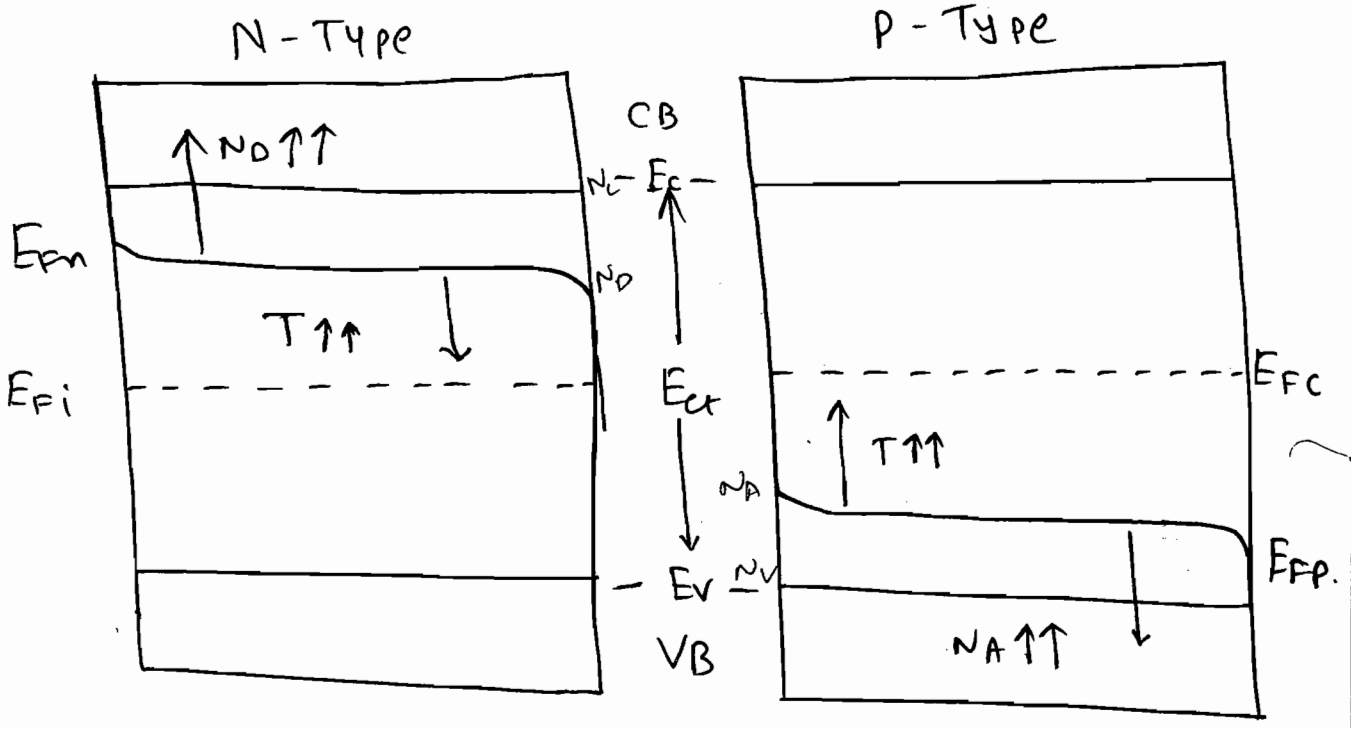
$$E_{Fn} = E_c - KT \ln\left(N_c/N_D\right) \quad \text{— (9)}$$

⇒ For p-type semiconductor $P_p \simeq N_A$.

from eqn - (4)

$$E_{Fp} = E_V + KT \ln\left(N_V/N_A\right) \quad \text{— (10)}$$

→ As dopping concentration increases in n-type ~~coinsi~~ (p-type). Fermi level moves closer and closer to conduction band (valance band) and may coinside with edge of Conduction band E_c (edge of valance band E_v) and may even penetrate into Conduction band (valance band).



⇒ <u>N- Type:</u>

(300°k)

$$E_{Fn} = E_c - kT \ln\left(\frac{N_c}{N_D}\right).$$

N_D : $N_D < N_c \longrightarrow E_{Fn} < E_c$.

$N_D \uparrow$: $N_D = N_c \longrightarrow E_{Fn} = E_c$.

$N_D \uparrow\uparrow$: $N_D > N_c \longrightarrow E_{Fn} > E_c$.

→ As Temp. increases Fermi level moves closer to centre of forbidden band in both n- & p-type semiconductors.

→

$$E_{Fn} - E_{Fi} = kT \ln (N_D/n_i) \quad \text{— (11)}$$

$$E_{Fi} - E_{Fp} = kT \ln (N_A/n_i). \quad \text{— (12)}$$

Q In a P-type semiconductor fermi level lies 0.04 ev above valance band. find New location of fermi level if acceptor Concentration is doubled.

Soln: Equating p_p to N_A in eqn - (1) we get.

$$N_A = N_V \cdot e^{-(E_F - E_V)/kT}$$

$$\therefore \frac{N_{A_1}}{N_{A_2}} = \frac{e^{-(E_{FP_1} - E_V)/kT}}{e^{-(E_{FP_2} - E_V)/kT}}$$

$$\therefore N_{A_2} = 2N_{A_1}$$

$$2 = e^{-\left(\frac{E_{FP_2} - E_V}{kT}\right) + \left(\frac{E_{FP_1} - E_V}{kT}\right)}$$ (0.4 ev)

$$e^{-\frac{0.04ev}{0.026}} \times 2 = e^{-\frac{(E_{FP_2} - E_V)}{kT}}$$

$$\therefore e^{-\frac{(E_{FP_2} - E_V)}{kT}} = 2 \times 0.2145.$$

$$\therefore \quad 2.33 = e^{\frac{(E_{FP2} - E_V)}{KT}}.$$

$$\therefore \quad \boxed{E_{FP2} - E_V = 0.022 \text{ eV}.}$$

Ans: New fermi level lies 0.022 eV above E_V.

(8) In n-type semiconductor Fermi level lies 0.3eV below E_C at 300°K. find new location of fermi level at 330°K. Assume N_C to be constant.

Soln:

$$E_C - E_{Fn} = 0.3 \text{eV}.$$

from eqn (9)

$$E_C - E_{Fn} = KT \ln\left(\frac{N_C}{N_D}\right).$$

$$\therefore \quad \frac{E_C - E_{Fn2}}{E_C - E_{Fn1}} = \frac{KT_2 \ln\left(\frac{N_C}{N_D}\right)}{KT_1 \ln\left(\frac{N_C}{N_D}\right)}$$

$$\therefore \quad \frac{E_C - E_{Fn2}}{0.3 \text{ eV}} = \frac{330}{300}$$

$$\therefore \quad \boxed{E_C - E_{Fn2} = 0.33 \text{eV}.}$$

Ans: New fermi level lies 0.33 eV below E_C.

☆ Fermi Level in open circuited P-N Diode :-

⇒ Fermi level is constant throughout the length of open circuited P-N diode.

⇒ Fermi level constant for an open circuited P-N Diode is valid at any P-N junction of any electronic device it is not constant for Forward biased (or) Reverse biased.

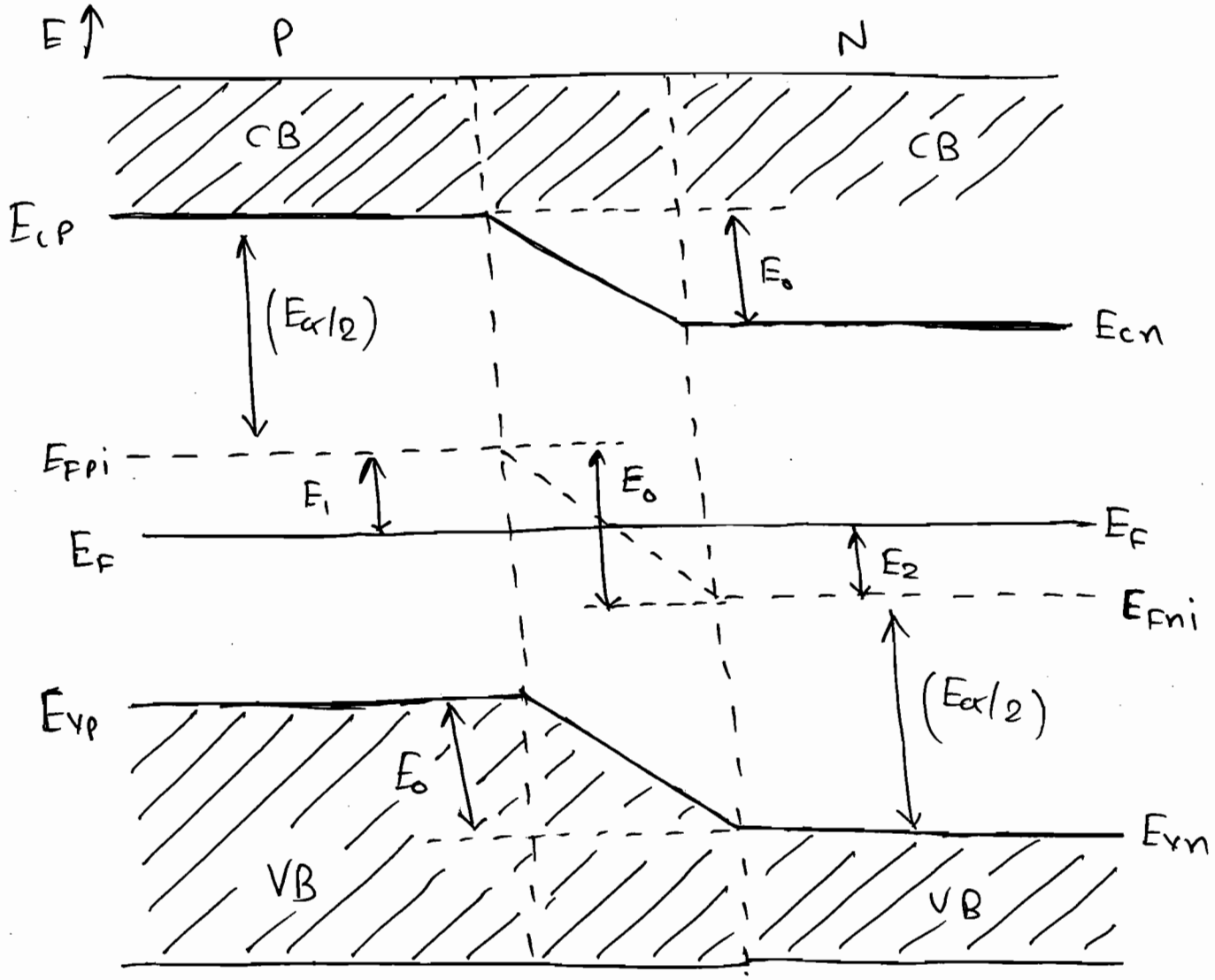
⇒ E_o (electron volts) (eV). is defined as Shift between edges of conduction band and valance band of P & N sides.

⇒ V_o (V) & E_o (eV) (or) Numerically equivalent

$$E_o(eV) = E_1 + E_2 = KT \ln\left(N_D N_A / n_i^2\right).$$

$$= E_{cp} - E_{cn} = E_{vp} - E_{vn}.$$

⇒



⇒ Using eqn- (11) & (12) of fermi level discussion.

$$E_1 = kT \ln (N_A/n_i)$$

$$E_2 = kT \ln (N_D/n_i).$$

Q) For a germenium diode calculate fermi-level position in p-region. w.r.t. intrinsic fermi level. given,

$N_D = 10^{16}\ cm^{-3}$

$N_A = 3 \times 10^{18}\ cm^{-3}$.

$n_i = 2.5 \times 10^{13}\ cm^{-3}$.

Soln:

$$E_i = kT \ln\left(\frac{N_A}{n_i}\right).$$

$$\therefore E_i = 0.026 \ln\left(\frac{3\times10^{18}}{2.5\times10^{13}}\right).$$

$$\boxed{E_i = 0.304 \text{ eV}.}$$

[a] In a P-N diode width of depletion region under open ckt conn is 0.334 μm. Calculate penetration of depletion region into P-side and E_0 & electric field intensity given

$$N_D = 10^{16} \text{ cm}^{-3}.$$

$$N_A = 4\times10^{18} \text{ cm}^{-3}.$$

$$\epsilon = 104.93 \times 10^{-14} \text{ F/m}.$$

Soln:

$$x_{p0} = \frac{W \cdot N_D}{N_D + N_A}.$$

$$\therefore x_{p0} = \frac{0.334 \times 10^{-6} \times 100 \times 10^{16}}{10^{16} + 400\times10^{16}}$$

$$x_{p0} = 0.0833 \times 10^{-6}$$

$$\therefore x_{p0} = 0.0833 \times 10^{-6}$$

$$\boxed{x_{p0} = 8.33 \times 10^{-8} \text{ cm}.}$$

$$\Rightarrow E_0 = -\frac{q \cdot N_A \cdot x_{p0}}{\epsilon}$$

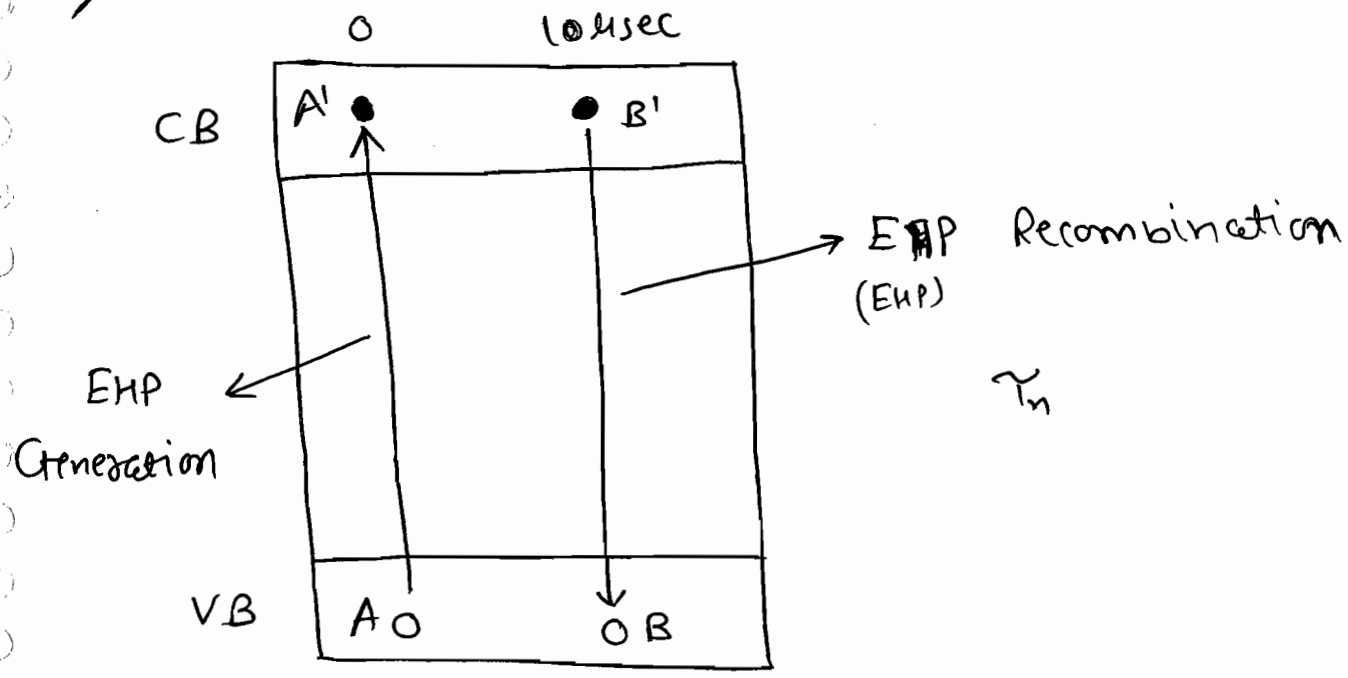
$$= \frac{-1.6\times10^{-19} \times 4\times10^{18} \times 8.33\times10^{-8}}{104.93\times10^{-14}}$$

$\therefore E_0 = -0.5 \times 10^5$ eV/km.

$\therefore$ $\boxed{E_0 = -50 \text{ KV/cm.}}$

* Generation and Recombination of Charge Carriers :

$\Rightarrow$



$\Rightarrow$ During EHP generation a bound e^- becomes free and a hole is created both of them support current.

$\Rightarrow$ During EHP recombination one free e^- becomes bound and one hole disappears hence current decreases.

$\Rightarrow$ Life-time for e^-, hole τ_n, τ_p is defined as duration of time during which an e^-, hole support current

⇒ Diffussion length for e^-, hole L_n, L_p is defined as distance travelled by an e^-, hole during their corresponding life times given by L_n, =

$$\boxed{L_n = \sqrt{D_n T_n}} \quad \&$$

$$\boxed{L_p = \sqrt{D_p T_p}}.$$

* Variation of minority Carrier concentration.

⇒ P_{no} : Initial thermally generated minority Carrier Concentration.

⇒ $P_n'(t)$, $P_n'(x)$: excess hole concentration at any time t, distance x generated due to illumination. (light rays).

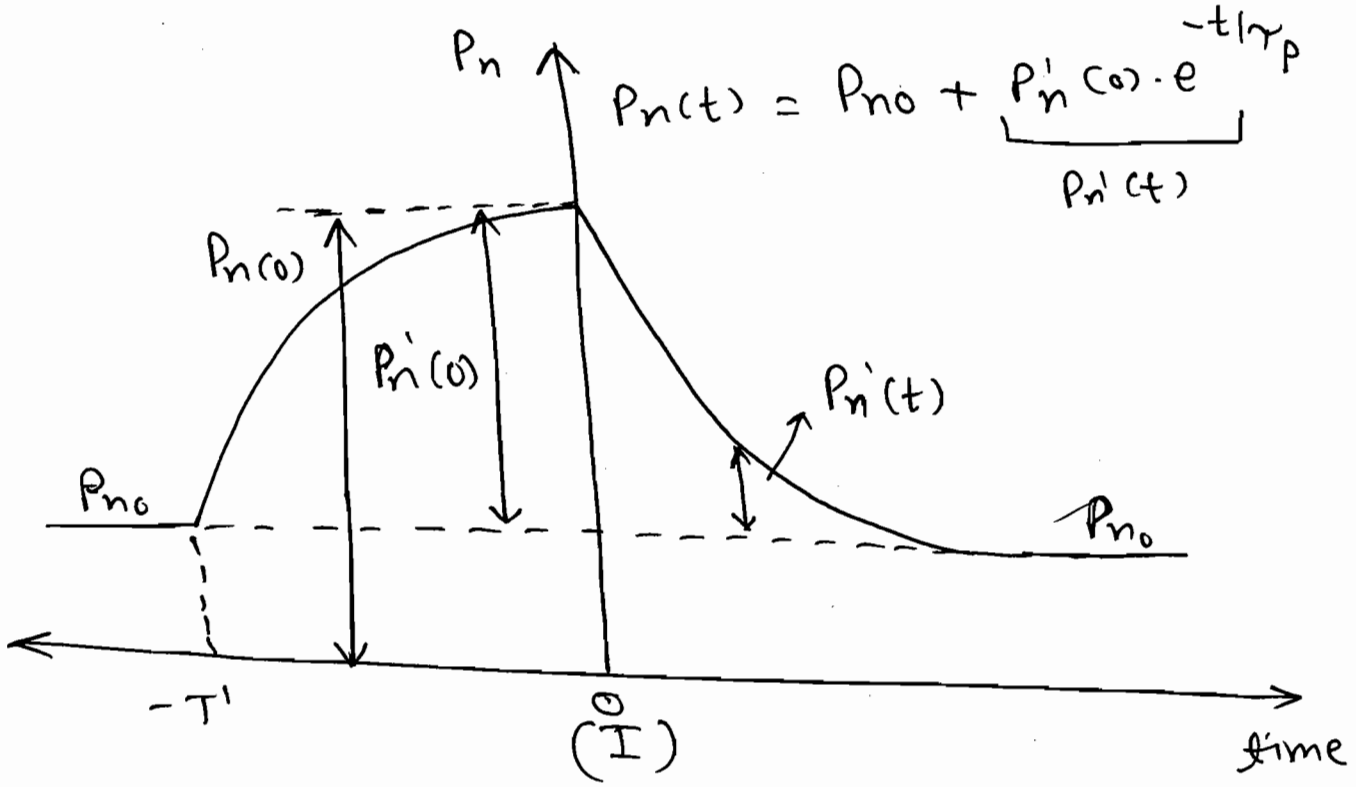
⇒ $P_n(t)$, $P_n(x)$: total hole concentration at any time t, distance x.

⇒ In fig-Ⓐ & Ⓑ, an n-type semiconductor is considered in which due to room

temp. EHP generation has occurred and P_{no} holes are generated.

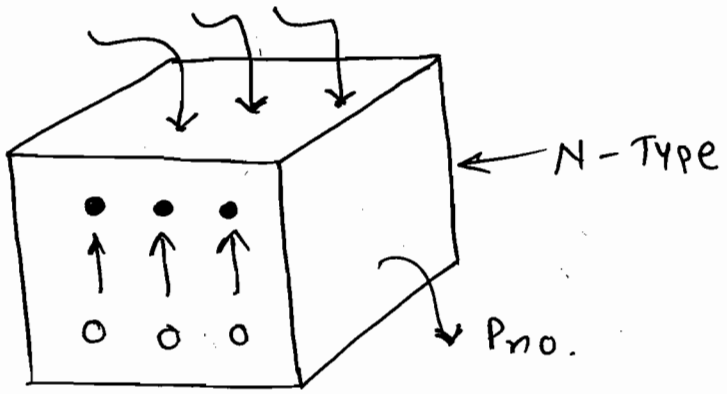
⇒ Fig-(A) :- with time:

→



OFF ← Illumination.

→



(II)

→ ON to a n-type semiconductors having P_{no} holes. Some illumination is allowed to fall uniformaly starting from atime of $-T'$ due to which again EHP

generation occurs and again holes are generated which get added to P_{no}. ~~em~~ hence hole concentration increases.

→ At a time of 0 sec, illumination is switched off. A hole recombine after τ_p sec. Hence hole concentration decreases.

→ A hole generated due to illumination once recombine can not regenerate because illumination is switched off. whereas a hole generated due to room temp. after recombination regenerates since temp. is in on condition. Hence decreases in concentration stops at P_{no}.

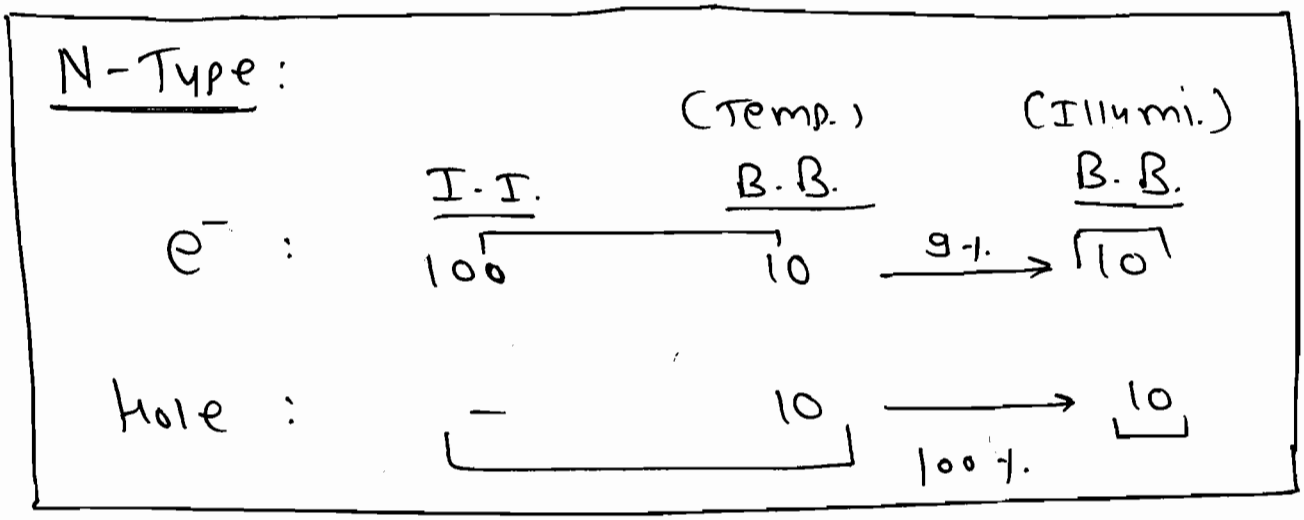
$$P_n(t) = P_{no} + P'_n(0)\, e^{-t/\tau_p}$$

$$t=0: \quad P_n(0) = P_{no} + P'_n(0) \cdot e^{-0} = P_{no} + P'_n(0).$$

$$t=\infty: \quad P_n(\infty) = P_{no} + P'_n(0) \cdot e^{-\infty} = P_{no}.$$

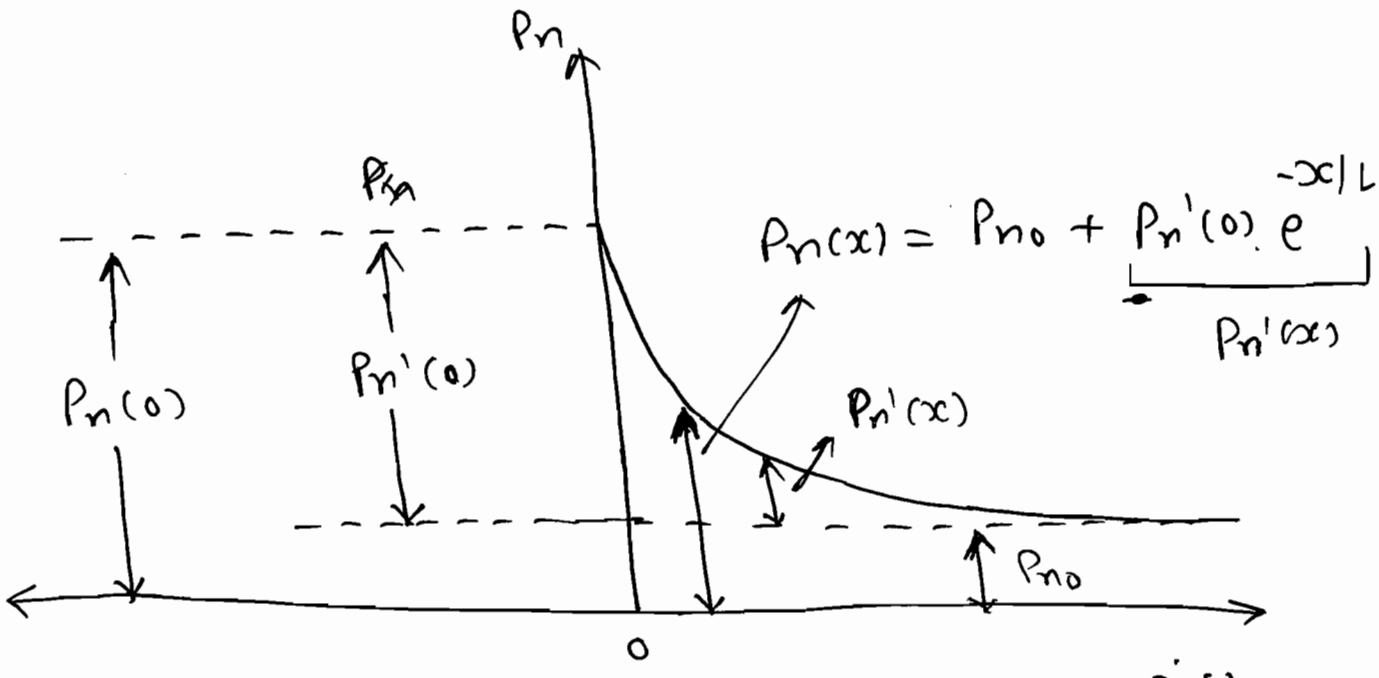
→ % increase in minority carrier Concentration ↓ due to illumination is very much greater than % increase in majority carrier

Concentration.

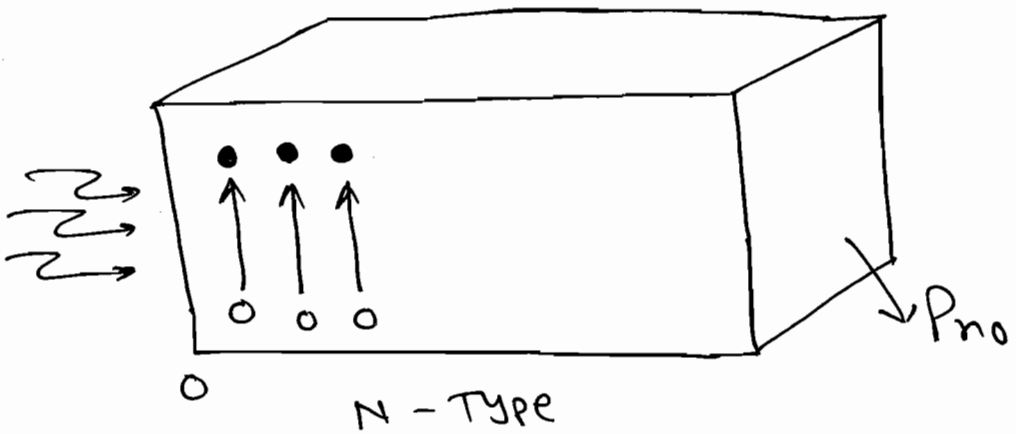


⇒ Fig- (B) with distance:

⇒ ON to an n-type semiconductor having P_{no} holes some illumination is allow to fall only at left side. Centered at distance zero. and matches with origin. Due to which again EHP generation occurs and again holes are generated which get added to P_{no}. Hence hole concentration increases to left side, due to difference in concentration hole diffusse from higher to lower concentrated area. after travelling L_p distance a hole recombines hence hole concentration decreases.



(I).



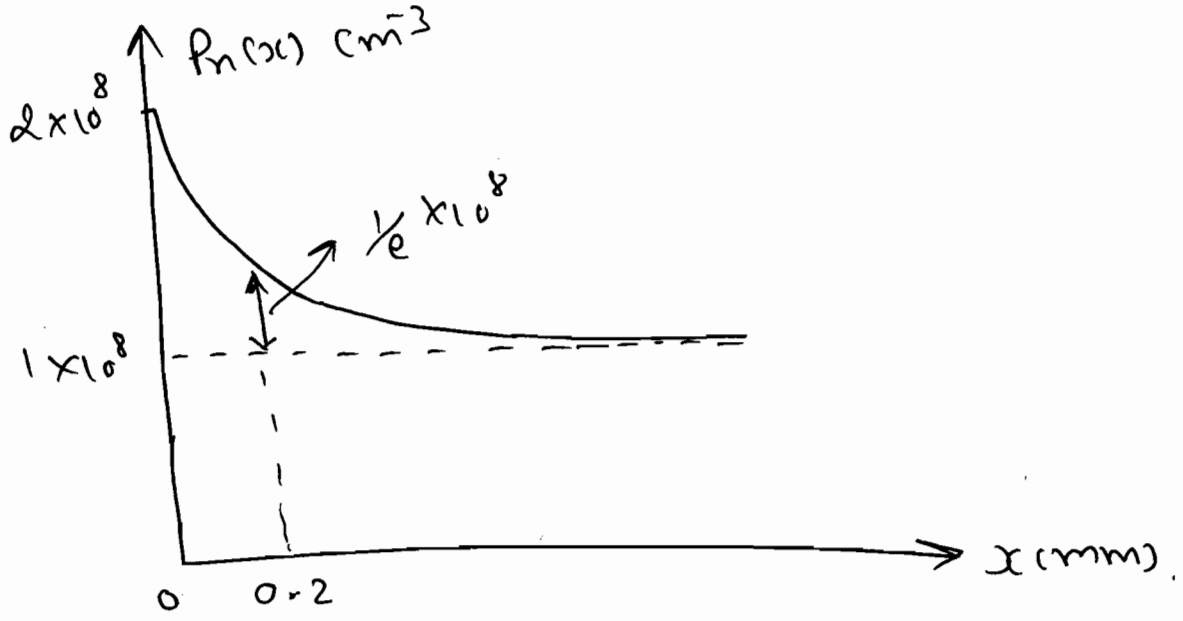
N - Type

(II)

Q An N-type silicon bar is illuminated at one end ($x = 0$). the minority carrier concentration variation is as shown given $n_i = 1.5 \times 10^{10}\ cm^{-3}$. calculate

(A) e^- Concentration.

(B) Diffussion length for holes.



Soln: (A) $n_{no} = n_i^2 / p_{no}$.

$$= \frac{(1.5\times10^{10})^2}{1\times10^8}$$

$$\boxed{n_{no} = 2.25\times10^{12}\ \text{cm}^{-3}.}$$

(B) $L_p = ?$

$$p_n'(x) = p_n'(0)\, e^{-x/L_p}.$$

$x = 0.2$mm : $\frac{1}{e}\times10^8 = (2\times10^8 - 1\times10^8)\, e^{-0.2\text{mm}/L_p}$.

$$\Rightarrow \boxed{L_p = 0.2\text{mm}.}$$

Q What fraction drift current is due to electrons in pure germenium given

$\mu_n = 3800$ cm^2/v-sec

$\mu_p = 1800$ "

Soln: drift current $I = n q \mu_n E A + p q \mu_p E A$. — (2)

→ Pure germenium ⇒ Intrinsic

hence, $n = p = n_i$.

$$\rightarrow \frac{I_n}{I_n + I_p} \times 100 \quad \text{—— ①}.$$

→ Substitute I_n and I_p form eqn - ② into ①.

$$\frac{I_n \times 100}{I_n \times I_p} = \frac{n_i \cdot q \cdot \mu_n EA \times 100}{n_i q \mu_n EA + n_i q N_p EA}$$

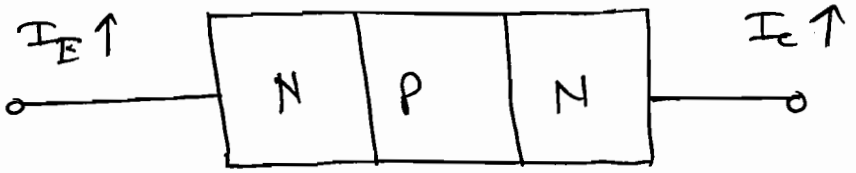
$$= \frac{\mu_n \times 100}{\mu_n + \mu_p}$$

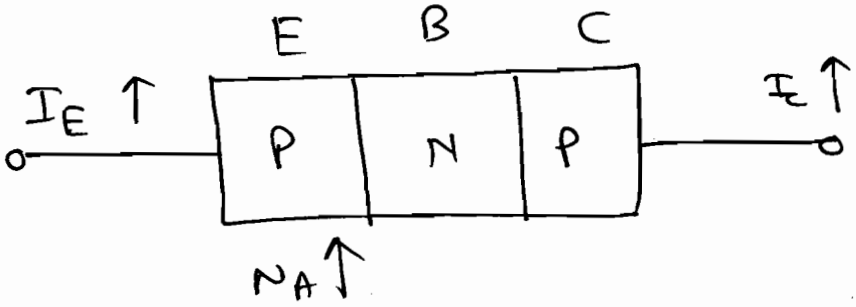
$$= \frac{3800}{3800 + 1800} \times 100$$

$$= \boxed{67.85\ \%}$$

Note:

→ For Practical application N-type devices like n-p-n transistor, n-channel JFET, induced n-channel MOSFET etc are prefered over Corresponding P-type devices since n-type devices work-out cheaper.





$\Rightarrow$ $I = \underbrace{n q \mu_n E A}_{I_{E(NPN)}} + \underbrace{p q \mu_p E A}_{I_{E(PNP)}}$. (COST) ↑

$I_{E(NPN)} > I_{E(PNP)}$.

Q Calculate change in contact potential if dopping on n-side is increased by a factor of 1000 and dopping on p-side is unaffected.

Soln:

$$V_0 = KT \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right)$$

$$V_0 = 0.026 \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right).$$

$$\rightarrow V_{02} - V_{01} = KT \ln\left(\frac{N_{A2} \cdot N_{D2}}{n_i^2}\right) - KT \ln\left(\frac{N_{A2} \cdot N_{D1}}{n_i^2}\right).$$

$$= KT\left[\ln\left(N_{D2} \cdot N_{A2}/n_i^2\right) - \ln\left(\frac{N_{D1} \cdot N_{A1}}{n_i^2}\right)\right].$$

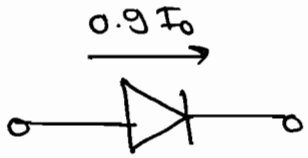
$$\therefore V_{O2} - V_{O1} = KT \ln\left(\frac{N_{O2} \cdot N_{A2}}{n_i^2} \times \frac{n_i^2}{N_{O1} \cdot N_{A1}}\right).$$

$$\therefore V_{O2} - V_{O1} = KT \ln\left(\frac{1000\, N_{O1}}{N_{O1}}\right). \quad (\because N_{A1} = N_{A2}).$$

$$\therefore \boxed{V_{O2} - V_{O1} = 0.179 \text{ V}.}$$

Q Calculate a voltage across a Si diode if 90% reverse saturation current is flowing in forward bias

Soln:



$$I = I_0 \left(e^{V/\eta V_T} - 1\right).$$

$$\therefore 0.9\, I_0 = I_0 \left(e^{V/2 \times 0.025} - 1\right).$$

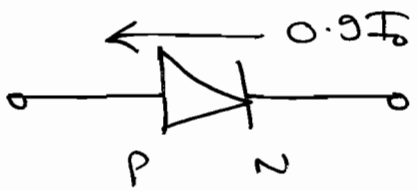
$$1.9 = e^{\frac{V}{0.052}}.$$

$$\therefore \boxed{V = 0.03337 \text{ V}}$$

$$\Rightarrow \boxed{V = 33.37 \text{ mV}}$$

Q find voltage at which reverse current in a Ge diode will reach 90% of its saturation value.

Soln:



$$\therefore \quad I = I_0 \left(e^{V/nV_T} - 1 \right).$$

$$\therefore \quad -0.9 I_0 = I_0 \left(e^{V/nV_T} - 1 \right).$$

$$\boxed{V = -59.86 \text{ mV}}$$

Note: while substituting a value for an entity, substitute along with sign while calculating the value of an entity dont disturb the existing sign.

✡ ZENER DIODE:

→ V_z : Knee (or) breakdown Voltage.

$I_{z(min)}$: Knee (or) minimum current.

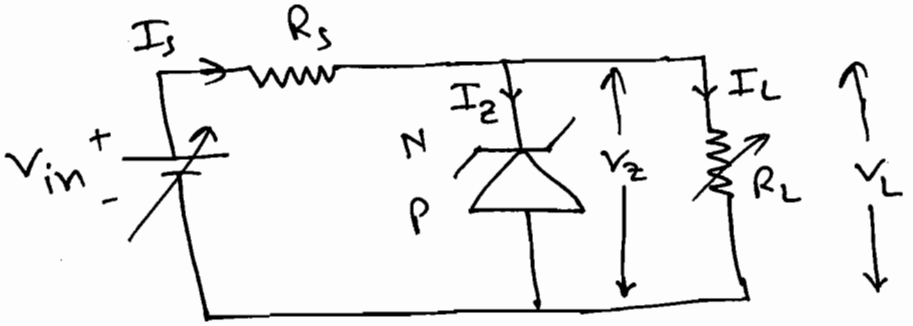
R_z : dynamic reverse breakdown Resistance.

NBO : Non breakdown.

→ Zener diode is named after its inventor C. Zener. In the ckt symbol, z differentiates zener diode from PN. diode. The direction of arrow shows the direction of flow of current when the diode is forward biay. PN, zener and Tunnel diodes are two terminal devices, Identical in Construction with only difference in doping Concentration.

→ In PN 1 IN 10^8, In zener 1 IN 10^5 and In Tunnel 1 IN 10^3. the forward and Reverse Chara. of zener diode are identical to forward and reverse Char. of PN diode except that zener diode can be operated in Revers BD whereas P-N diode should not be operated in Reverse B.D.

⇒



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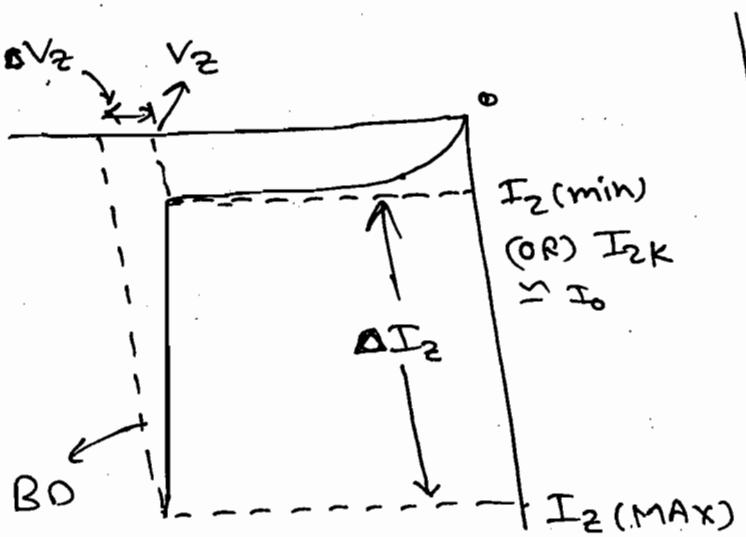
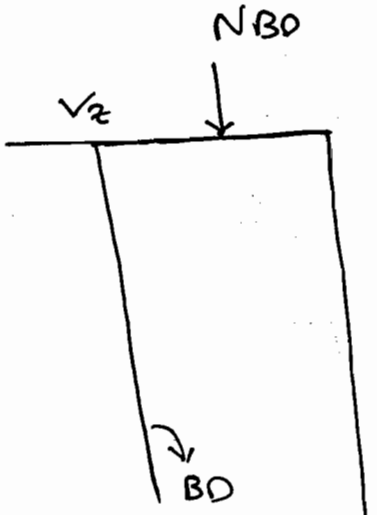


Practical

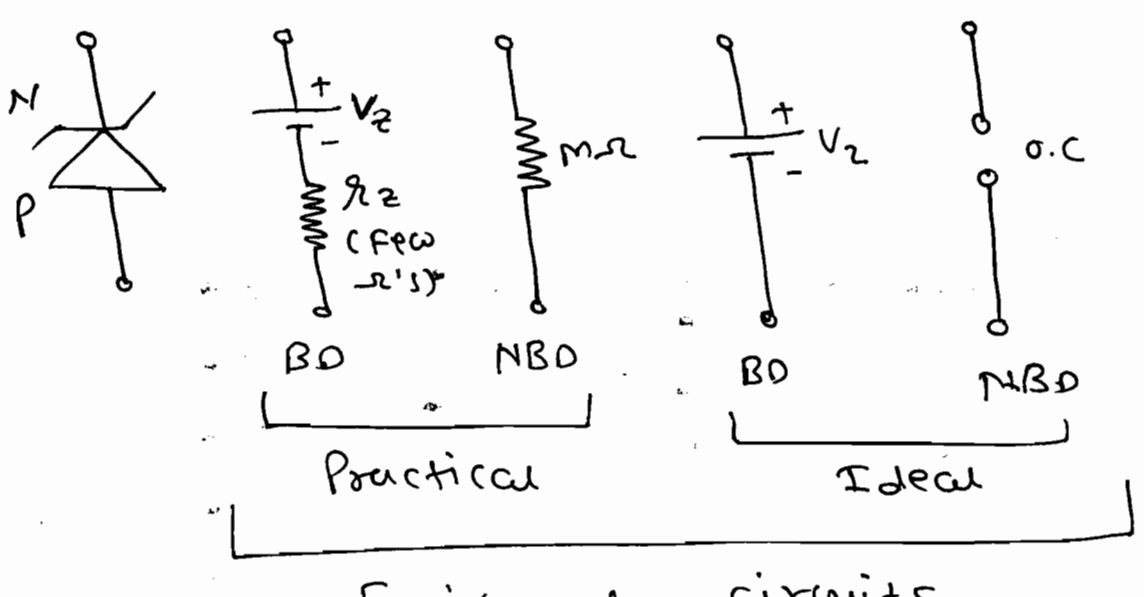
$R_z = \Delta V_z / \Delta I_z$



Ideal

$R_z = 0$.

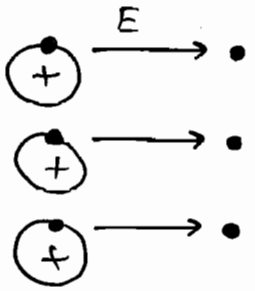
⇒



Equivalent circuits.

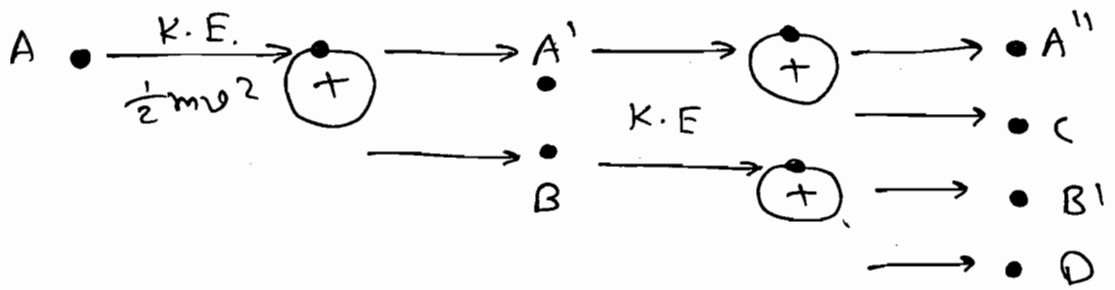
⇒ Zener Breakdown:

→ Due to applied reverse biased a large electric field gets developed across Zener diode which pulls out charge carrier by breaking covelent bonds and making atoms ions called field ionization. Vouming charge carrier thus generated are responsible for large current. This breakdown occurs in relatively more dopped step junction diodes at $V_z < 6V$ with $\frac{dV_z}{dt} = -0.1\ \%/^\circ C$



⇒ Avalanch Break down:

→ ~~Ion~~



⇒ 1 → 2 → 4 → 8 → 16 → ...

Carrier multiplication → Impact Ionization.

Avalanch multiplication.

→ A thermally generated charge carrier gets attracted towards opposite polarities of applied reverse biased gain kinetic energy and collieds with an atom on the way and transfer its kinetic energy to a valance shell electron of the atom and push that electron to conduction band and makes it free thus one free carrier becomes two. The process repeate further and due to carrier (or) avalanch multipiication voluminus carriers are generated which are responsible for large current. Due to collission an atom becomes ion called Impact Ionization. This breakdown occurs in relatively less dopped linear junction diodes at $V_z > 6V$. with $\frac{dV_z}{dT} = +0.1\ \%/^{\circ}C$.

1.

⇒ In the above equivalent ckt, +ve of V_z should matched with n-side of diode.

⇒ The above equivalent ckt are valid only for reversed biased zener

diode. for a forward bias zener diode use any of the three forward biased eqn ckt of P-N Diode.

* Voltage Regulator:

⇒ A Voltage regulator should maintain constant Voltage across terminals of load irrespective of fluctuation in load (or) Supply.

⇒ A Zener diode can act act as Voltage regulator if it is operated in reverse breakdown for which the following Condition to be satisfied.

(i) Current throgh zener diode should be greater than (or) eqnal to I_{Zmin}.

(ii) Voltage across terminals of zener diode should be V_Z, BD Voltage.

⇒ Fixed Input Variable load:

R_L : $I_{S(fix)} = I_Z + I_L$: $V_L = I_L . R_L$

R_L : $I_{S(fix)} = I_Z \uparrow + I_L \downarrow$: $V_L = (I_L) \cdot (R_L \uparrow)$

R_L :

$\Rightarrow$

R_L: $I_{S(fix)} = I_Z + I_L$: $V_L = I_L \cdot R_L$

$R_L \uparrow$: $I_{S(fix)} = I_Z \uparrow + I_L \downarrow$: $V_L = (I_L \downarrow)(R_L \uparrow)$

: $I_Z < I_{Z(max)}$.

$R_L \downarrow$: $I_{S(fix)} = \not{I}_Z \downarrow + I_L \uparrow$: $V_L = (I_L \uparrow)(R_L \downarrow)$

: $I_Z \geq I_{Z(min)}$.

$\Rightarrow$ Vin is fixed, R_L can vary hence I_S is fixed.

$\rightarrow$ For a given R_L, $I_{L(fix)} = I_Z + I_L$ with $V_L = I_L \cdot R_L$. Say R_L increases then I_L decreases. hence I_Z increases by equal amount since I_S is fixed.

$\rightarrow$ Though I_L increases, voltage across ideal zener in breakdown, V_Z is constant hence $V_L = V_Z$ is constant

(or) increased R_L and decreased I_L counter each other to make $V_L = I_L \cdot R_L$ constant.

⇒ Variable input fixed load:

→ V_{in}: $I_s = I_z + I_{L(fix)}$; $V_L = I_L \cdot R_L$.

$V_{in}\uparrow$: $I_s\uparrow = I_z\uparrow + I_{L(fix)}$: $V_L = I_L \cdot R_L$

: $I_z < I_{z(max)}$.

$V_{in}\downarrow$: $I_s\downarrow = I_z\downarrow + I_{L(fix)}$: $V_L = I_L \cdot R_L$.

: $I_z \geq I_{z(min)}$.

⇒ V_{in} can vary & R_L is fixed. hence I_L is fixed.

→ for a given R_L, $I_s = I_z + I_{L(fix)}$ with $V_L = I_L \cdot R_L$. Say V_{in} increases then I_s increases hence I_z increases by equal amount making I_L fixed. Current always prefers least resistive path and resistance of ideal Zener in BD is zero.

→ Though I_z increases voltage across ideal zenear in break down V_z is constant. Hence $V_L = V_z$ is constant

(or) since I_L & R_L are fixed,

$V_L = I_L \cdot R_L$. is constant.

* Procedure to Solve Numericals: Imp.

(i) Identify whether Zener diode is ideal (or) Practical.

(ii) If the diode is FB replace by any of the three FB equivalent ckt of P-N Diode.

(iii) If the diode is reverse biased verify BD status and replace by appropriate equivalent ckt.

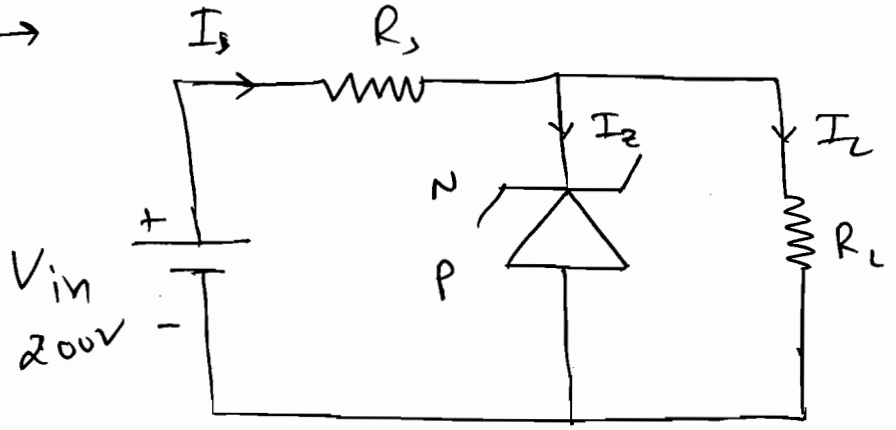
(iv) Apply KCL (or) KVL.

Q A 50 V, 5 to 40 mA Zener diode is used as shown in a regulator ckt

(A) Calculate R_s to allow Voltage regulation from $I_L = 0$ to I_{Lmax}. also calculate I_{Lmax}.

(B) If R_s is set as found in Part-(A) and I_L is fixed at 25mA find the permissible range of V_{in} for Zener diode to act as regulator safely.

→



Soln:

given data:

→ $V_z = 50V.$

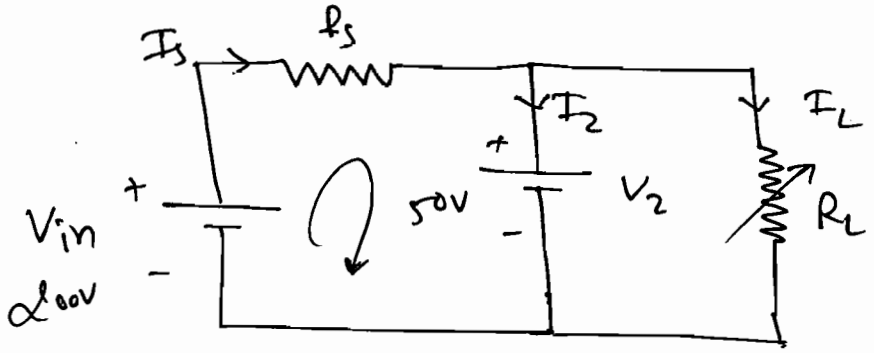
$I_{z(min)} = 5mA.$

$I_{z(max)} = 40mA.$

If $R_z = 0\ \Omega$ ↓ Ideal.

(A) Fixed input Variable load.

→ zener diode is in BD. replace with by its eqn ckt. (voltage source V_z).



→ $I_{s(fix)} = I_{z(max)} + I_{L(min)}$

$= 40 + 0 = 40mA.$

By KVL, $200 = I_s \cdot R_s + 50$

$V_{in} = I_{s(fix)} \cdot R_s + V_z.$

$$\Rightarrow R_S = \frac{(200 - 50)}{40mA} = 3.75\,k\Omega$$

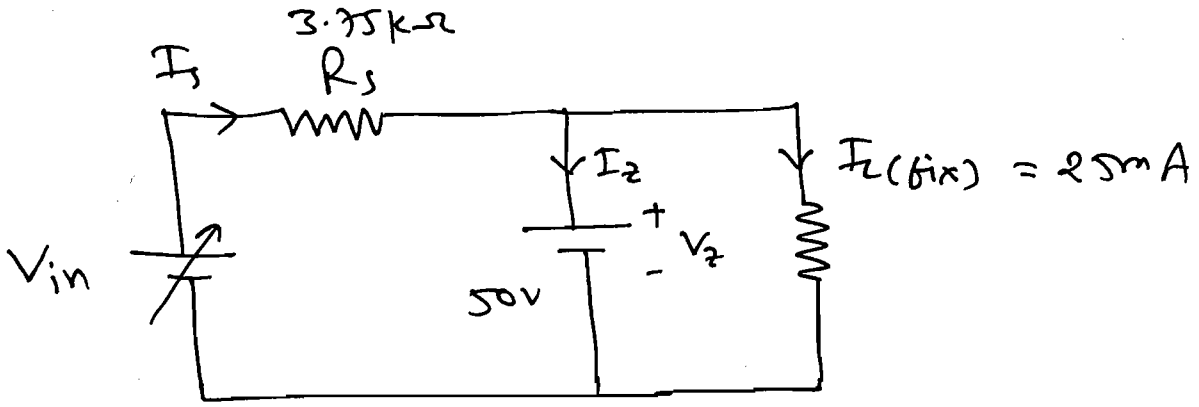
$$\boxed{R_S = 3.75\ k\Omega}$$

$$\Rightarrow I_{S(fix)} = I_{Z(min)} + I_{L(max)}.$$

$$\therefore 40 = (5) + I_{L(max)}$$

$$\Rightarrow \boxed{I_{L(max)} = 35mA}$$

(B) Variable input fixed load:



$$\Rightarrow I_{S(min)} = I_{Z(min)} + I_{L(fix)}$$

$$= 5mA + 25mA = 30\,mA.$$

$$\Rightarrow I_{S(max)} = I_{Z(max)} + I_{L(fix)}$$

$$= 40 + 25 = 65\,mA.$$

$$\therefore V_{in(min)} = I_{S(min)} \cdot R_S + V_Z.$$

$$V_{in(min)} = (30 \times 3.75) + 50$$

$$V_{in(min)} = 162.5\ V$$

$\therefore V_{in(max)} = (65 \times 3.75) + 50.$

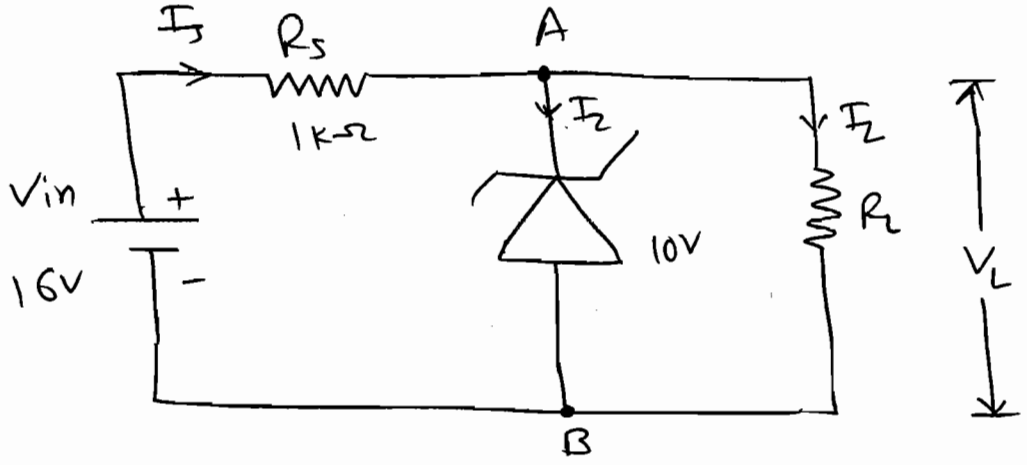
$$\boxed{V_{in(max).} = 293.75\ V}$$

So, range of V_{in} is 162.5 V to 293.75 V.

Q For the given zener diode ckt. calculate V_L given

(A) $R_L = 1.2K\Omega$

(B) $R_L = 3K\Omega$



Soln:

$I_{Z(min)} = 0, \quad R_Z = 0$

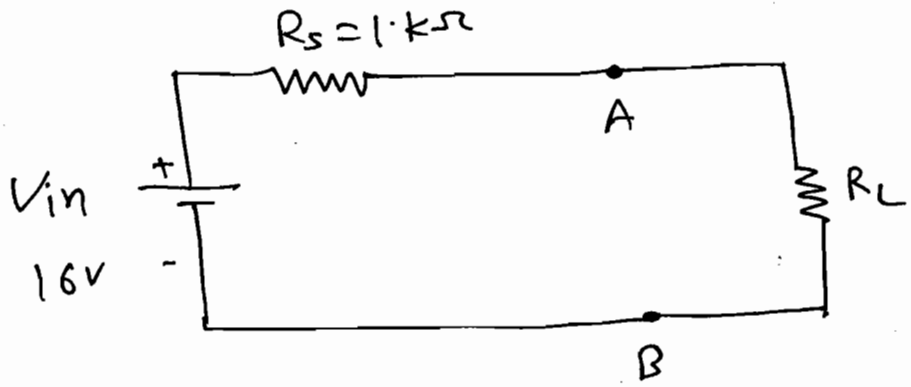
$V_Z = 10V$

for a zener diode to go into BD the following two conditions are to be satisfied.

① Current through zener diode should be greater than (or) equal to $I_{Z(min)}$ which is already satisfied

since $I_{Z(min)} = 0$.

(2) Voltage across terminals of Zener diode should be V_Z, BD voltage. To verify this physically remove Zener diode from CKt and measure V_{AB}. as shown.



$$V_{AB} = \frac{R_L \times 16}{R_L + R_S}.$$

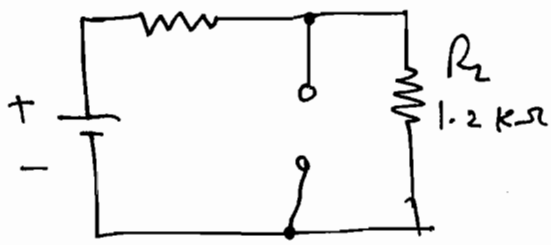
$$\therefore V_{AB} = \frac{16 \times R_L}{1K + R_L}.$$

(A) $R_L = 1.2\,K$

$V_{AB} = 8.73\ V.$

→ Zener diode is not in BD replace it by its equivalent, O.C.

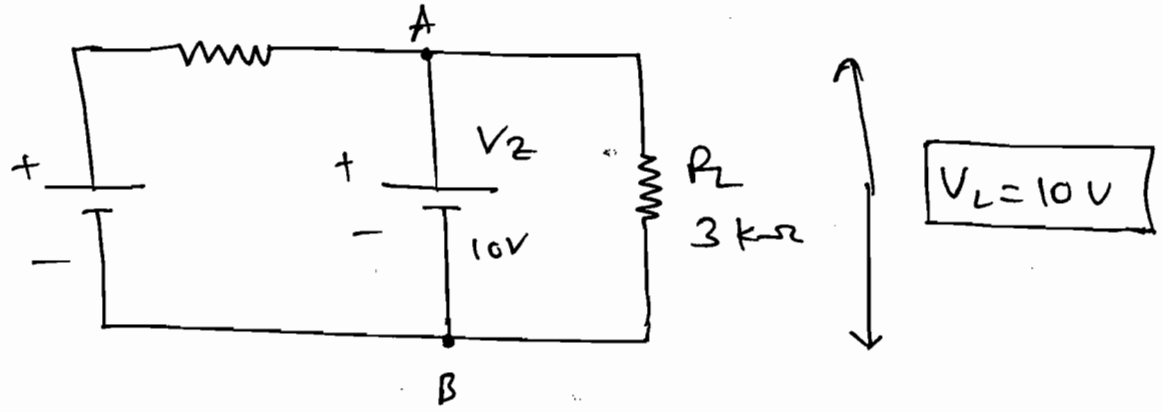
$$\boxed{V_L = V_{AB} = 8.73V}$$



(B) $R_L = 3k$

→ $V_{AB} = 12V$

→ Zener diode is in BD. replace it by its equivalent, Voltage source V_z



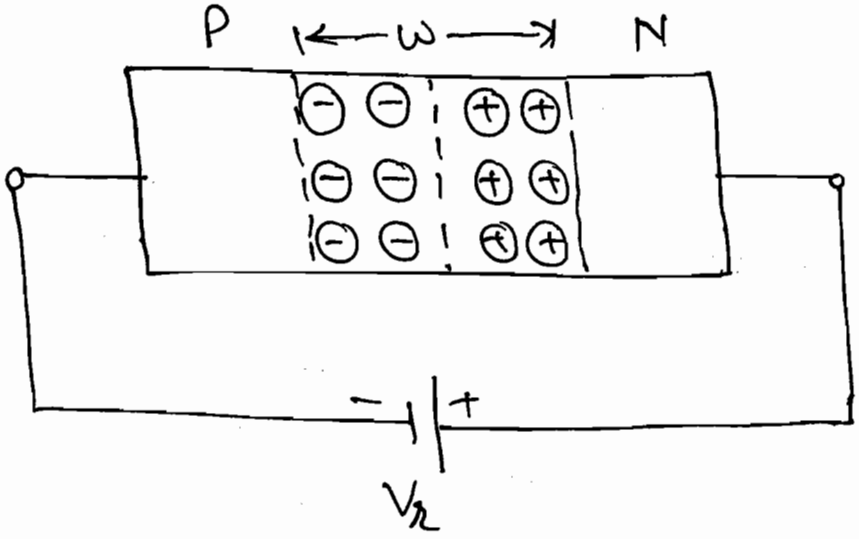
* Transition region (or) Depletion region (or) Space charge region (or) Barrier.

Capacitance C_T :

⇒ Change in reverse bias changes in depletion width and ions of depletion region. Hence a non-zero value of $\frac{dq}{dt}$ is exibuted by depletion region which is by defination Capacitance Called depletion region Capacitance.

⇒ $C_T = \epsilon A / w$.

⇒



⇒ ω is proportional to $V_j^{1/2}$

⇒ $\omega \propto V_j^{1/2}$ for step (or) abrupt j^n.

⇒ $\omega \propto V_j^{1/3}$ for linear (or) Graded j^n.

where, j^n voltage. $V_j \approx V_0 - V_d$.

where, V_0 : open circuited contact potential.

& V_d : Voltage across diode.

(V_d is -ve for RB).

$$\therefore C_T = \sqrt{\frac{q \epsilon A^2}{2\left(\frac{1}{N_D} + \frac{1}{N_A}\right)(V_0 - V_d)}}$$

→ Transition Capacitance at Zero bias,

$$C_{T_0} = C_T \big|_{V_d = 0}$$

$$\rightarrow \boxed{C_T = \frac{C_{TO}}{\left(1 - \frac{V_d}{V_o}\right)^{m_T}}}$$

$m_T = 0.5$ for Step junction. &
$= 0.33$ for linear "

⇒ Change in reverse bias changes width of depletion region and capacitance. Hence it can be used as voltage variable capacitor (or) Varicap. (or) Varactor diode:

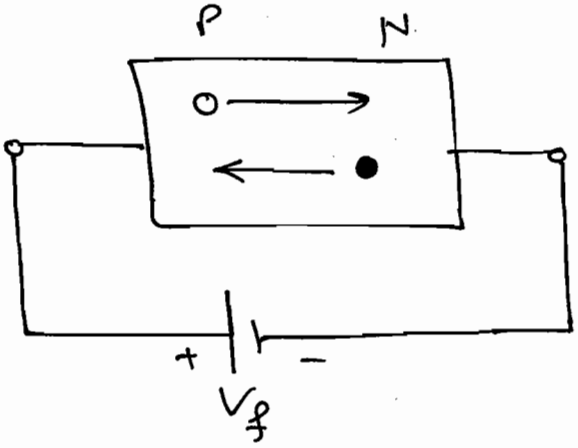
= * Diffussion Capacitance:

⇒ Change in forward bias changes magnitude of diffussing charges and current. Hence, a non-zero value of $\frac{dQ}{dV}$ is exibitted by diffussing charges which is by defination capacitance called Diffussion Capacitance.

$$\boxed{C_D = \frac{\tau I}{\eta V_T}}$$ where,

$\tau = \tau_p + \tau_n$.

$\Rightarrow$



$$\frac{dQ}{dx} \neq 0.$$

$$C_D = \frac{\tau I}{\eta V_T}.$$

Where, $\tau = \tau_p + \tau_n$.

Q A silicon diode has a diffusion capacitance of 1 μF when carrying a current of 1mA. Assuming $N_A \gg N_D$. Calculate τ_p.

Soln: $N_A \gg N_D$. hence C_D eqn gets modified to

$$C_{DP} = \frac{\tau_p . I}{\eta V_T}.$$

$$\tau_p = \frac{1 \times 10^{-6} \times 2 \times 0.026}{1 \times 10^{-3}}$$

$$\boxed{\tau_p = 52\ \mu s}$$

Q A step junction si diode with $V_o = 0.637$ V has transition capacitance at zero bias of 0.5 PF. Calculate C_T at the reverse

of 5 V.

Soln: Here, $C_{To} = 0.5\ PF$

$$C_T = \frac{C_{TO}}{\left(1 - \frac{V_a}{V_o}\right)^{m_T}}$$

$$= \frac{0.5 \times 10^{-12}}{\left(1 - \frac{(-5V)}{0.637}\right)^{0.5}}$$

$$\therefore \boxed{C_T = 0.168\ PF}$$

[a] A reverse biased diode is having a junction voltage of 8V and junction capacitance 15PF. If junction voltage is increase to 12V capacitance drops to 13.5 PF find whether it is abrupt (or) graded junction.

Soln: Assumption: Abrupt junction.

$\omega \propto V_j^{1/2}$, ϵ & A are constant

hence $C_T \propto \frac{1}{V_j^{1/2}}$.

$$\therefore \quad \frac{C_{T_2}}{C_{T_1}} = \left(\frac{V_{j1}}{V_{j2}}\right)^{1/2}$$

$$\therefore \quad \frac{C_{T_2}}{C_{T_1}} = \left(\frac{8}{12}\right)^{1/2} =$$

$$\therefore \quad C_{T_2} = 0.82 \times C_{T_1}$$

$$C_{T_2} = 12.25 \text{ PF}.$$

→ C_{T_2} is not equal to 13.5 PF. hence it is not abrupt i.e. it is graded junction.

* Effect of Temperature on Reverse Saturation Current I_o.

⇒ Increase in temp. increases EHP generation and minory Concentration hence I_o increases i.e. $\frac{dI_o}{dt} > 0$.

$$\therefore \quad \boxed{I_o = \frac{A q D_p p_{no}}{L_p} + \frac{A q D_n n_{po}}{L_n}.}$$

⇒ From the above eqn after analysis we get,

$$\Rightarrow \boxed{\frac{1}{I_o}\cdot\frac{dI_o}{dt} = \frac{m}{T} + \frac{E_{go}}{\eta T V_T}}$$

Where, $m = 1.5$ for Si

$= 2$ for Ge.

$$\left.\begin{aligned}\frac{1}{I_o}\cdot\frac{dI_o}{dt} &= 8\ \%/^\circ C \text{ for Si} \\ &= 11\ \%/^\circ C \text{ for Ge}\end{aligned}\right] \text{ At } 300^\circ K.$$

⇒ Practically for both diodes rise is found to be $7\ \%/^\circ C$.

⇒ I_o gets doubled for every $10^\circ C$ rise temp. i.e.

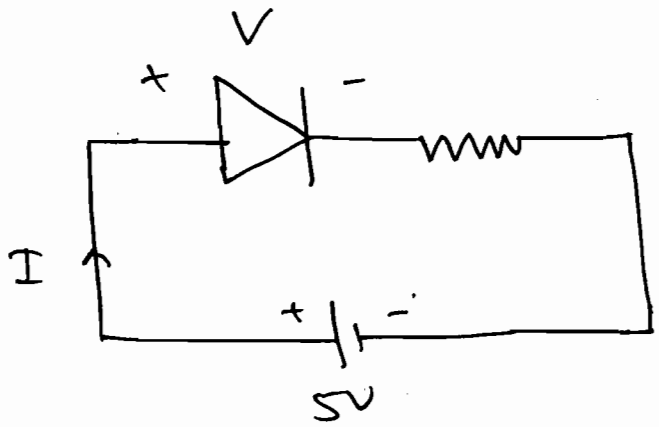
$$\boxed{I_{o2} = I_{o1}\cdot 2^{(T_2 - T_1)/10.}}$$

~~$I_{o2} = I_{o1} \times 2$~~

* Effect Temp. on Voltage:

⇒ For $1^\circ C$ rise in temp. to maintain Constant Current through diode decrease Voltage across diode by $2.5\ mV$ i.e. $\boxed{\frac{dV}{dT} = -2.5\ mV/^\circ C.}$

⇒



$$I = I_0 \left(e^{V/\eta V_T} - 1\right)$$

⇒ From Current eqn of diode after analysis we get,

$$\frac{dV}{dT} = \frac{V - (E_{g0} + m\eta V_T)}{T}$$

$$= -2.1 \text{ mV}/^\circ\text{C} \rightarrow \text{Ge}$$

$$= -2.3 \text{ mV}/^\circ\text{C} \rightarrow \text{Si}$$

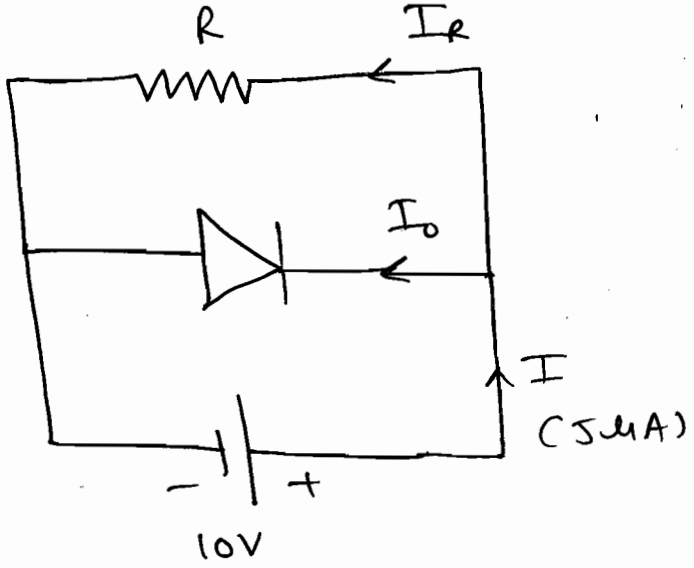
} At 300°k.

Note:

⇒ The above value of $\frac{dV}{dT}$ is valid only for forward bias.

Q The Current I of circuit was found to be increasing by 7%/°C rise in temp. Calculate I_0 assuming Ge diodes reverse sat. currents temp co-efficient is 11%/°C.

$\Rightarrow$



Soln:

given data,

$$\frac{1}{I}\cdot\frac{dI}{dt} = 7\,\%/^\circ C$$

$$\frac{1}{I_o}\cdot\frac{dI_o}{dt} = 11\,\%/^\circ C$$

By, KCL $\quad I = I_o + I_R.$

$$\frac{dI}{dT} = \frac{dI_o}{dT} + \frac{dI_R}{dT}\cdot \quad (\because R = \text{const}^n \Rightarrow I_R = \text{const}^n).$$

$$\therefore \quad I\left(\frac{1}{I}\cdot\frac{dI}{dT}\right) = I_o\left(\frac{1}{I_o}\cdot\frac{dI_o}{dT}\right).$$

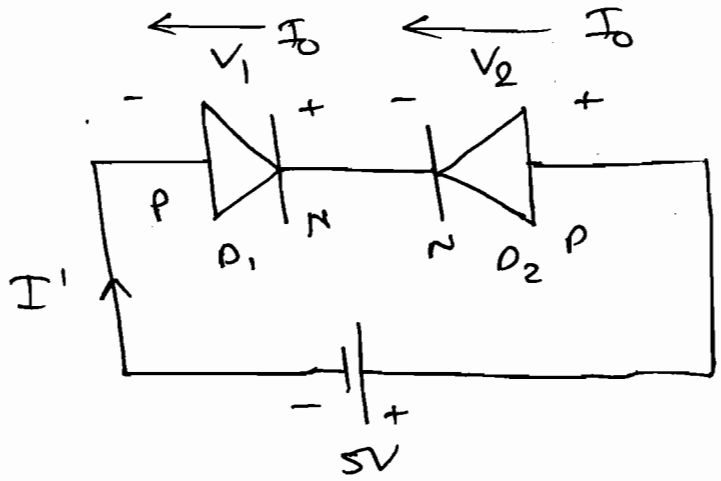
I: $5\mu A$ $\quad \left(\frac{1}{I}\cdot\frac{dI}{dT}\right)$: 0.07 $\quad \left(\frac{1}{I_o}\cdot\frac{dI_o}{dT}\right)$: 0.11

$$\therefore \quad I_o = \frac{5 \times 0.07}{0.11}$$

$$\therefore \quad \boxed{I_o = 3.18\,\mu A.}$$

[Q] Two Ge diode connected as shown.

Calculate V_1, V_2 & I'.



Soln:

[D]: $I = I_0 \left(e^{V/nV_T} - 1 \right)$.

$\therefore I_0 = I_0 \left(e^{\frac{V}{nV_T}} - 1 \right)$.

$\therefore 2 = \not{2} \, e^{V/nV_T}$

$V = \boxed{18.\text{mV.} = V_2.}$

By KVL, $5 = V_1 + V_2$.

$\therefore V_1 = 5 - V_2$

$\therefore \boxed{V_1 = +4.982}$

Note: → While giving answer for a voltage consider the polarities given in problem statement.

→ while giving answer for a current consider the direction shown in prob. statement.

→ $\boxed{I' = -I_0}$

(a) The reverse saturation current density of a Ge diode is 1 mA/m². Find the voltage to be applied across it in forward bias to get a current density of 10^5 mA/m².

Soln: divide $I = I_0(e^{V/nV_T} - 1)$ by cross-sectional area A,

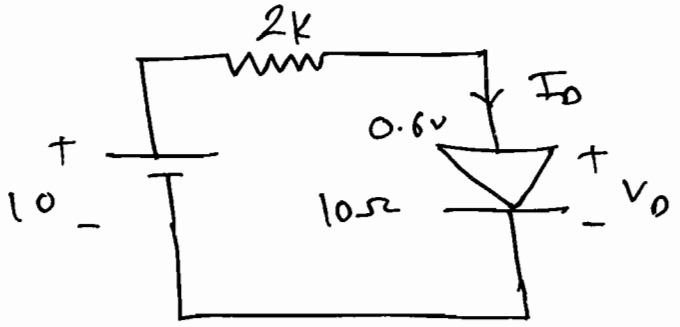
$$\therefore \frac{I}{A} = \frac{I_0}{A}\left(e^{\frac{V}{nV_T}} - 1\right).$$

$$\Rightarrow \boxed{J = J_0\left(e^{\frac{V}{nV_T}} - 1\right).}$$

$$\therefore 10^5 = 1\left(e^{\frac{V}{1\times 0.026}} - 1\right).$$

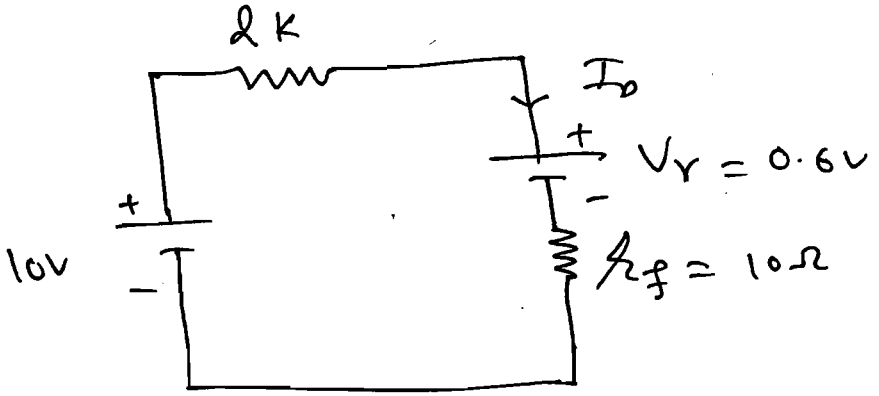
$$\therefore \boxed{V = 0.3\ V.}$$

(a)



Calculate I_D & V_D in the given Ckt.

Soln:



$$I_D = \frac{10 - 0.6}{2k + 10} = 4.67 mA.$$

$$\therefore \boxed{I_D = 4.67 mA.}$$

$$\therefore V_D = V_r + I_D R_f$$

$$= 0.6 + (4.67 \times 10^{-3} \times 10)$$

$$\therefore \boxed{V_D = 0.646 V}$$

☆ Tunnel (Esaki) Diode:

→ $E_{Fn} = E_c - KT \ln (N_c/N_D)$.

$E_{FP} = E_v + KT \ln (N_v/N_A)$.

$E_{Cr} = KT \ln (N_c \cdot N_v / n_i^2)$.

$E_o = KT \ln (N_D \cdot N_A / n_i^2)$.

⇒ Heavy Dopping: (Tunnel)

$N_D > N_C$

$N_A > N_v$

$E_{Fn} > E_c$

$E_{FP} < E_v$

$E_o > E_{Cr}$

Normal Doping: (PN).

$N_c > N_D$

$N_v > N_A$

$E_{Fn} < E_c$

$E_{FP} > E_v$

$E_{Cr} > E_o$

⇒

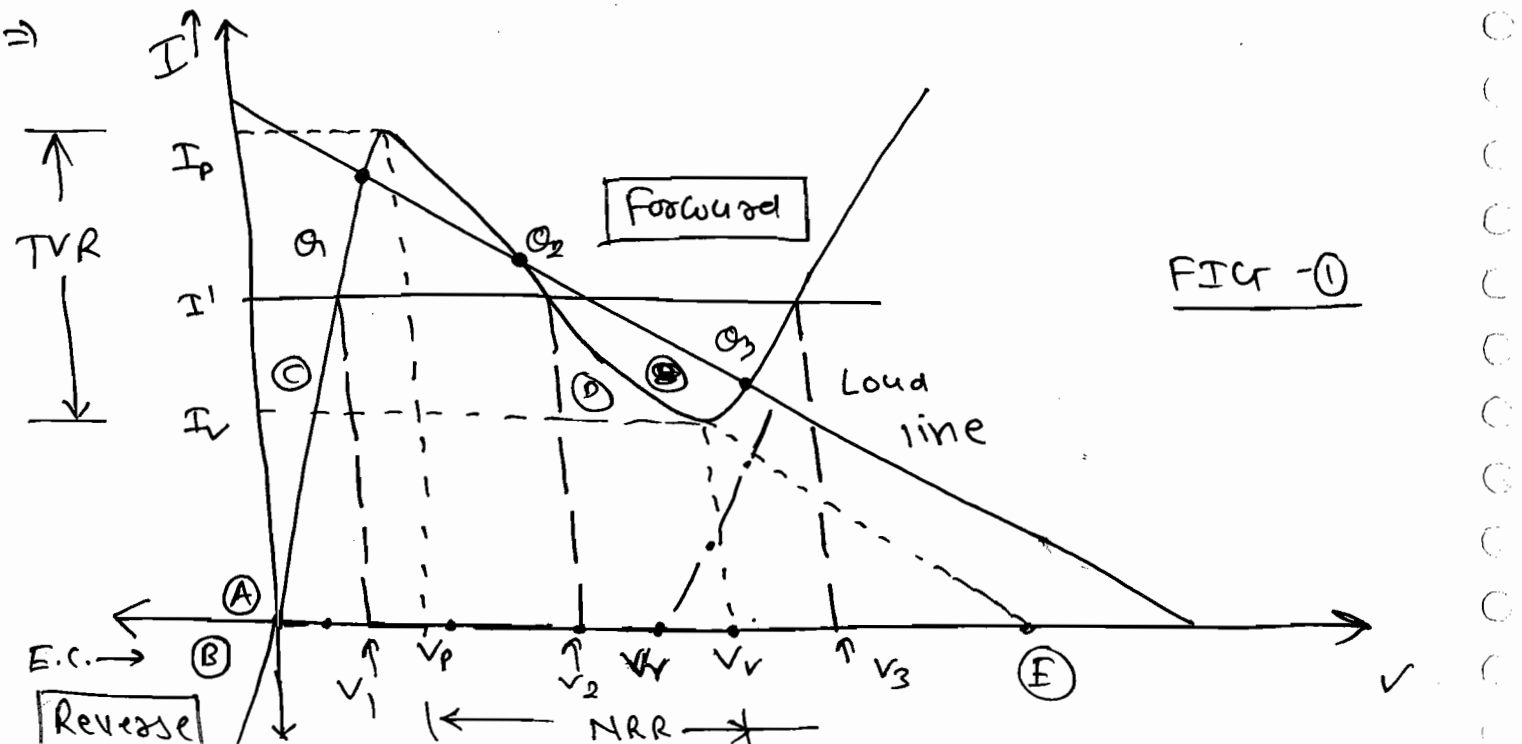


FIG -①

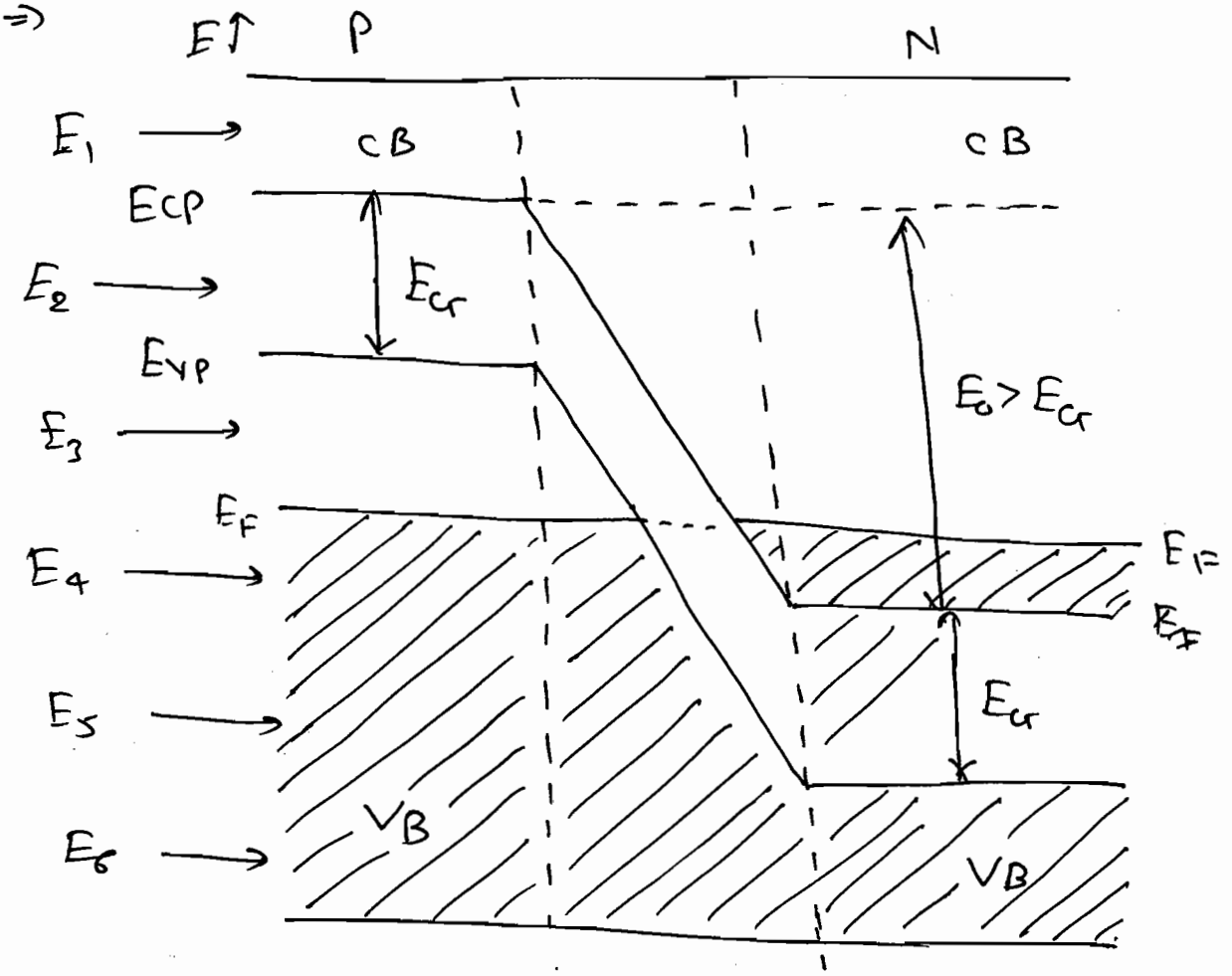
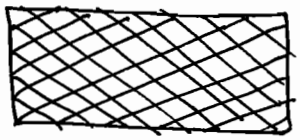


Fig-(A) : Open circuit.

⇒ Due to heavy doping of the order of $1:10^3$ (or) $1:10^{20}\ cm^{-3}$ width of depletion region decreases to as small as 100 A° at such narrow depletion region according to quantam mechanics a special effect called tunneling is observed based on it the diode is design. It was proposed by a Esaki.

→ ▭ → Empty State. (electron - doesn't exist.)

⇒ ▨ → Filled State (electron exists).

⇒  → Filled states parallel to empty states.

→(i) Width of depletion region should be very narrow (100Å) ✓

→(ii) At one side of diode filled states should exists. at the other side at the same energy empty state should exists.

→ If the above two conditions are satisfy then electrons tunnels from filled to empty state.

* Open circuit:

⇒ From fig- Ⓐ it can be observed that second condition of tunneling is not satisfied hence tunnelling is not possible. Hence current is zero.

⇒ V & I are zero. hence fig- Ⓐ matches with point Ⓐ of fig- Ⓘ.

* Reverse bias:

⇒ Due to Reverse bias width of depletion

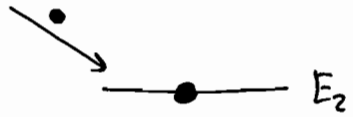
region and ions of depletion region increases hence V_o (Volts) and E_o (eV) increase by applied reversed bias.

$E_o = E_{cp} - E_{cn}$ is increasing implies N-side levels shift down hence fig. (A) becomes (B).

→ In fig - (B) top filled states of Valance band of P-side became parallel to bottom empty state of Conduction band of n-side. hence e^- tunnel from P to n and produce current from n-to P.

V & I are -ve hence fig - (B) matches with point - (B). as reverse bias increases n-side levels shift down more and more hence volume of tunneling and reverse current increases. i.e. excellent Conduction (E.C) is possible.

⇒ E_1 ——•



E_2 ——• ⇒ Diffussion

(-) E_3 ——• → ——• E_3 (+) ⇒ Drift

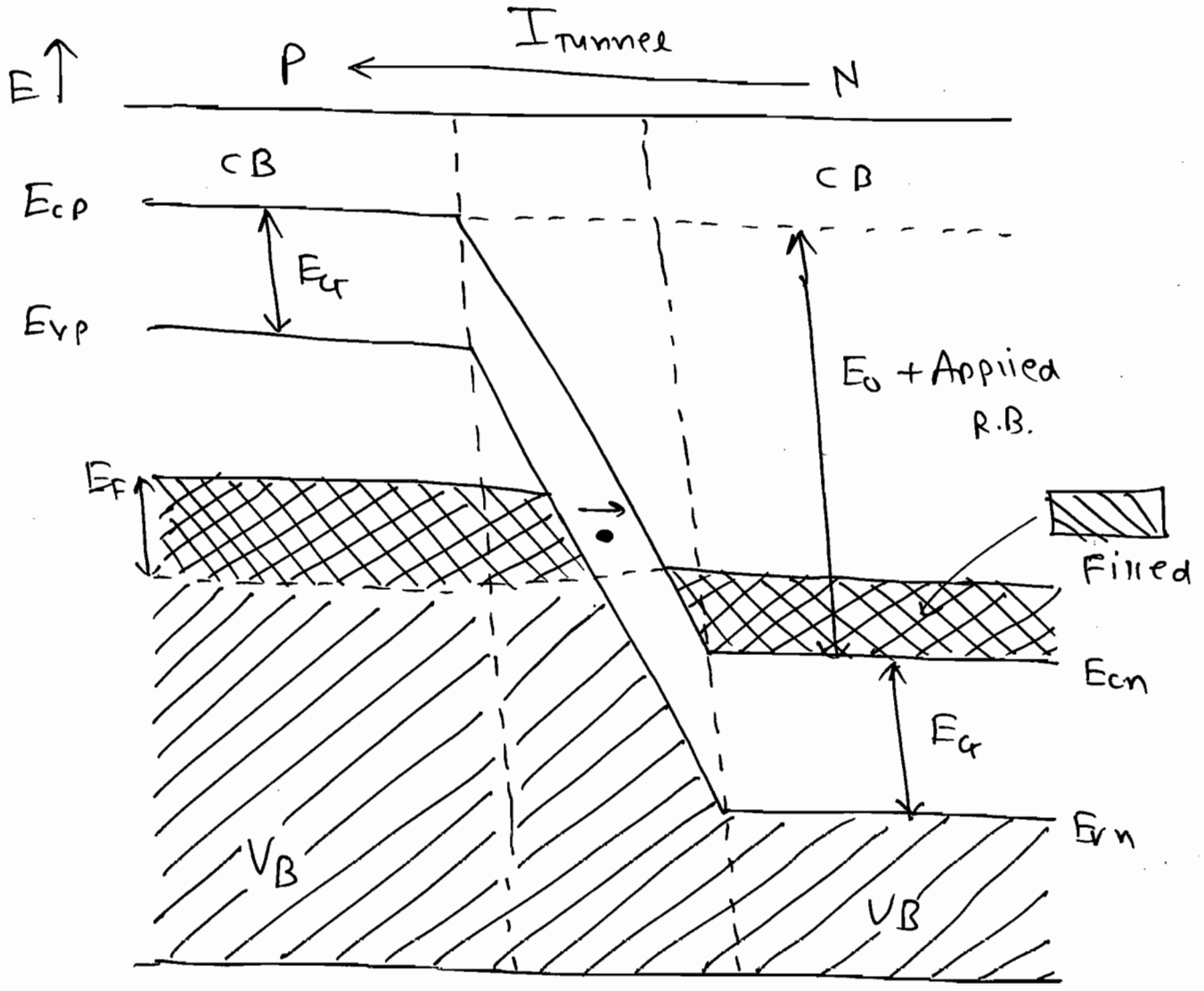


Fig- (B)

Note:

→ In a P-N diode $E_g > E_o$ hence energy of e^- is more than energy of hill hence to go from one side to other side of diode electron climbs down (diffussion) energy hill.

→ In a Tunnel diode $E_o > E_g$ hence energy of e^- is less than energy of hill hence to go from one side to other side electron penetrates (Tunnels) through barrier.

⇒ Due to forward bias width of depletion region and ions of depletion region decreases hence V_0 (V) and E_0(eV) decrease by applied forward bias.

$E_0 = E_{cp} - E_{cn}$ is decreasing implies n-sides levels move up. Hence fig - (A) becomes (C).

⇒ In fig - (C) Top filled state of Conduction band of n become parallel to bottom empty states of p hence second Condition of tunneling is satisfied hence electrons tunnel from N to P and produce current from P to N.

⇒ V & I are +ve hence fig - (C) matches with point (C). as forward bias increases forward current starts from 0 (point - (A)), increases (point - (C)) later on reaches a maximum (I_p), decreases (point - (D)) and finally becomes zero (point - (E)).

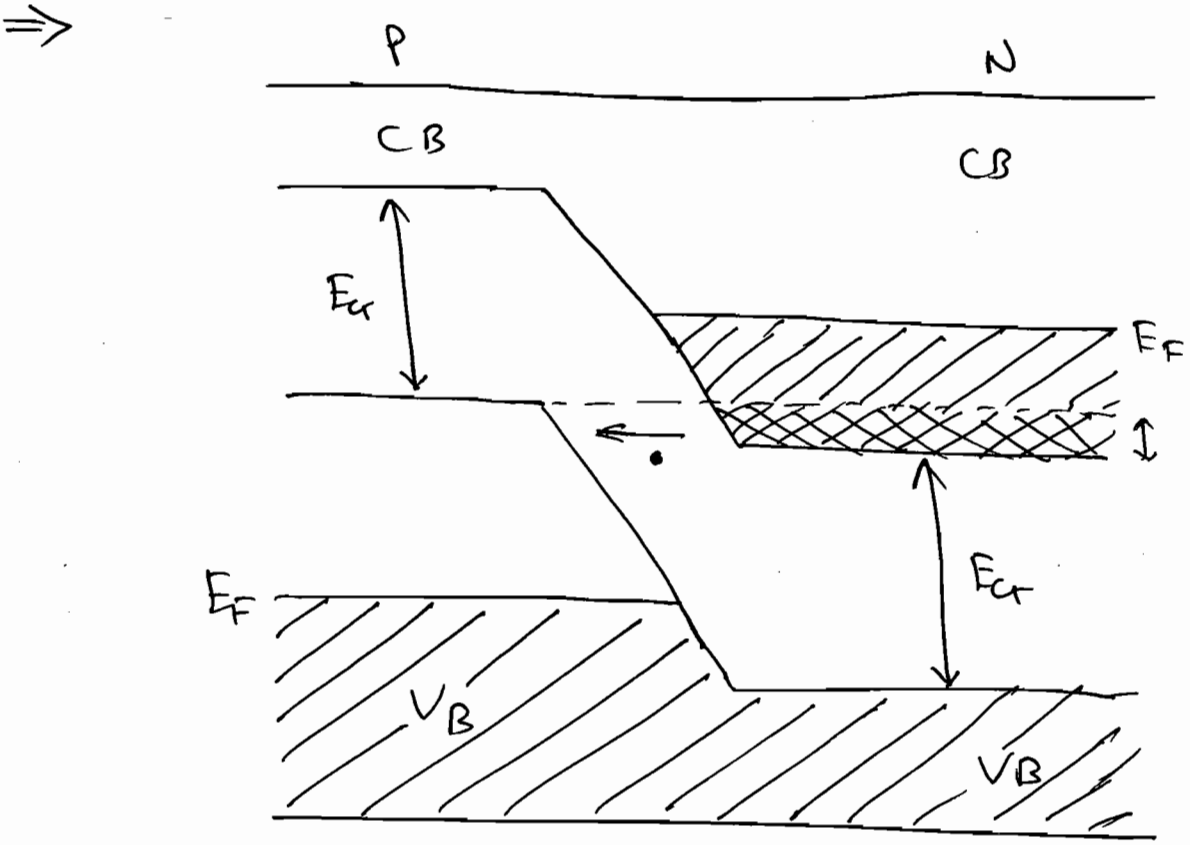


FIG-(A) FB ↑↑

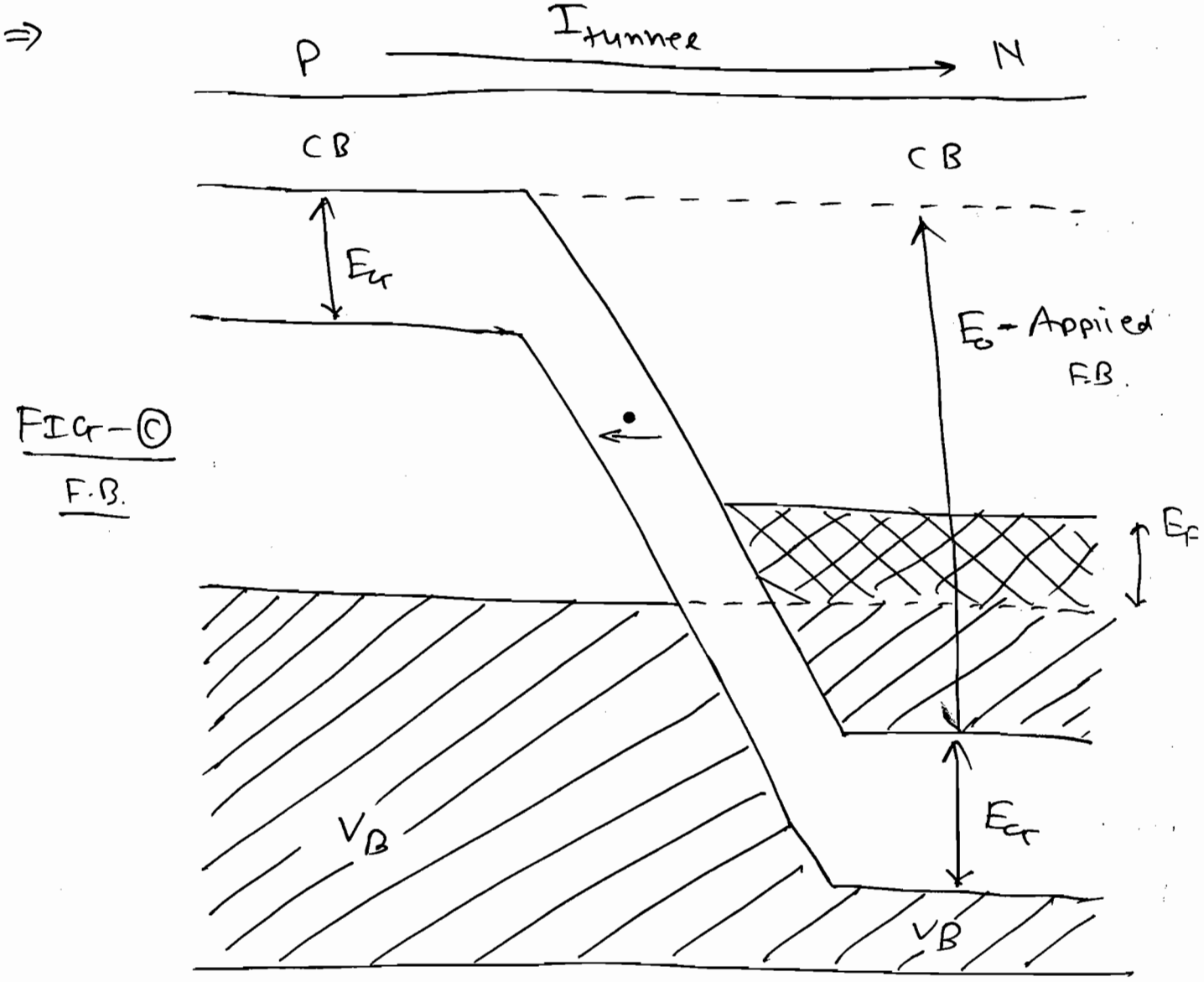


FIG-(C)
F.B.

⇒

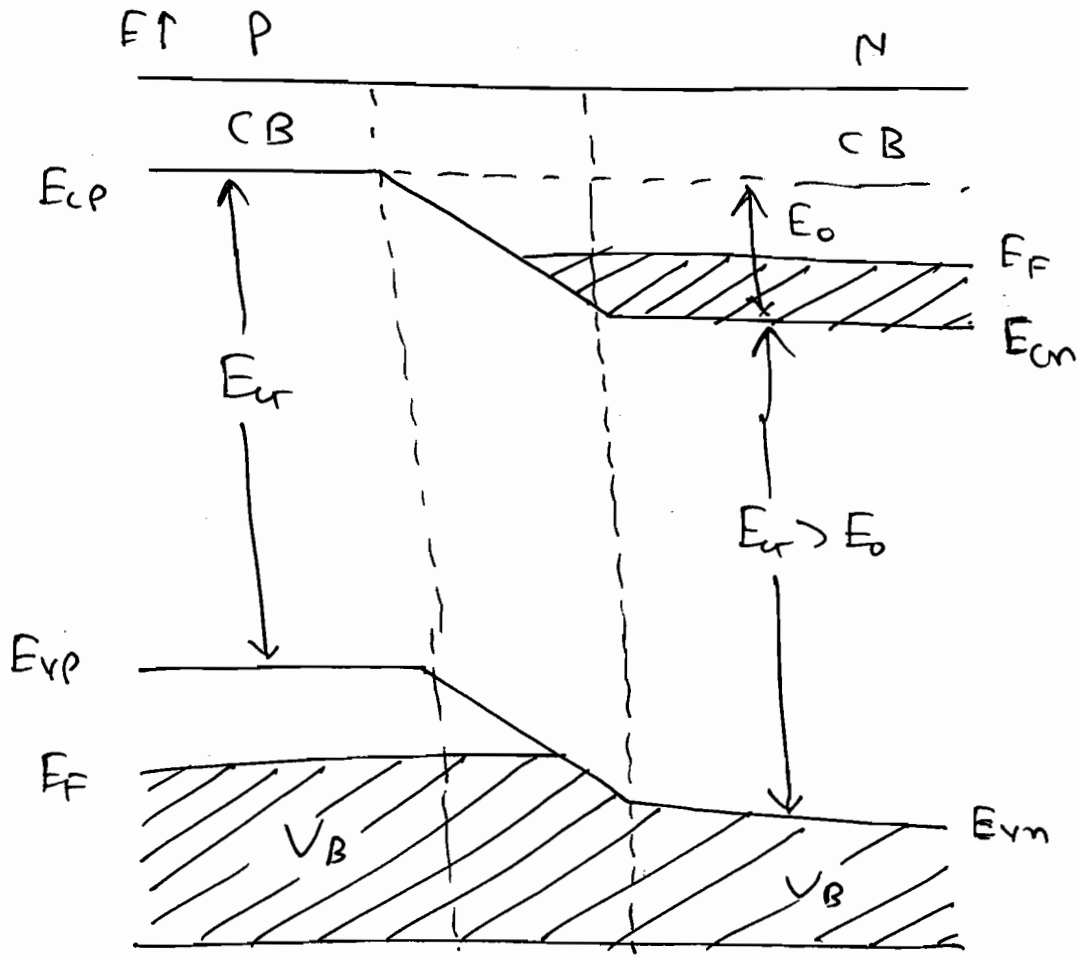
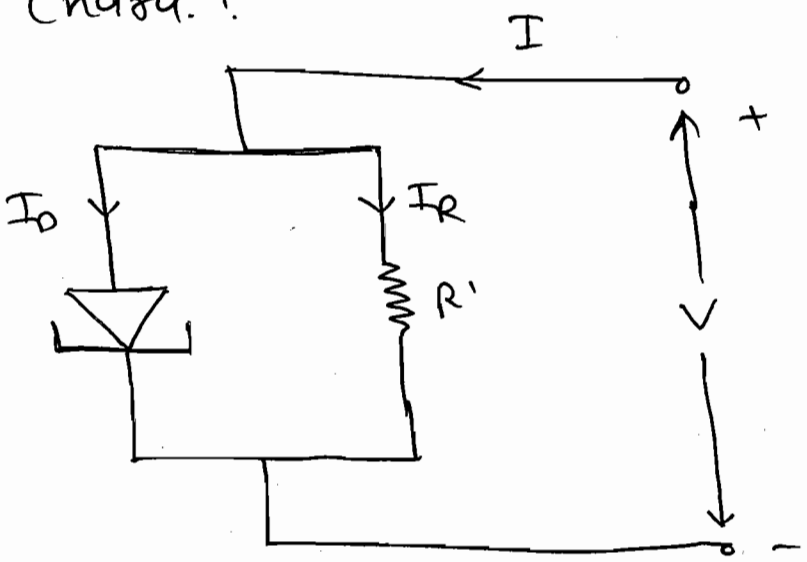


Fig- (E) - FB↑↑↑

→ Due to forward bias E_o decreases and $E_{cr} > E_o$ occurs (fig- (E)) which valid for a P-N diode hence from now onwards whatever current is possible in forward biased P-N diode will also be possible in forward biased tunnel diode hence forward char. of P-N diode (dash and dots) is superimpose onto forward char. of tunnel diode.

→ In FB tunnel diode I_{tunnel} flows from P→N. In FB P-N diode $I_{diffusion}$

istor R' is placed parrallel to a rent
nnel diode which has $\left|\frac{dI_D}{dV}\right|_{max} = \frac{1}{10}$ tarting
e value of R' such that the ncreases
tion doesn't exhibit -ve region in
-p) decreases
Charg.?



E.

reases

V_r and

ci ors current

I_{tunnel}

Zero.

e mes Zero

-ve region means as voltage
ncreases current decreases. -ve
egion should not be exibitted.

ence $\frac{dI}{dV} \geq 0$.

$I = I_D + I_R$.

$I = I_D + V/R'$.

$\therefore \frac{dI}{dV} = \frac{dI_D}{dV} + \frac{1}{R'}$.

$\frac{dI}{dV} \geq 0$.

ce, $\frac{1}{R'} \geq \left|\frac{dI_D}{dV}\right|_{max} \longrightarrow$ $R' \leq$ low

which

t which

increases,

sistance

Q Consider a tunnel diode under open circuit condition. Calculate width of depletion region given.

$$N_D = N_A = 4.41 \times 10^{19}\ cm^{-3}.$$

$$V_0 = 0.75\ V.$$

$$\epsilon = 141.6 \times 10^{-14}\ F/cm.$$

Soln:

$$W = \sqrt{\frac{2\epsilon V_0}{q}\left[\frac{1}{N_D} + \frac{1}{N_A}\right]}$$

$$= \sqrt{\frac{2 \times 141.6 \times 10^{-14} \times 0.75}{1.6 \times 10^{-19}} \times \frac{2}{4.41 \times 10^{19}}}$$

$$\boxed{W = 77.7\ A^\circ}$$

Note:

Eqn. given for P-N diode for W, X_{no}, X_{po}, V_0, E_0 etc can be used for any P-N jn of any electronic device.