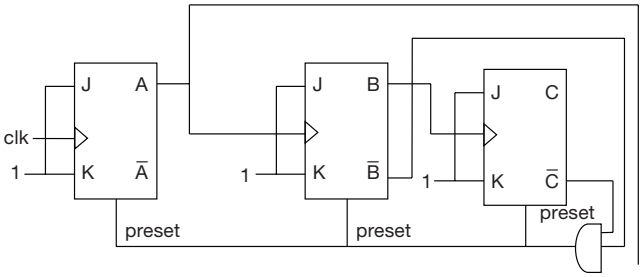
DIGITAL LOGIC TEST 2

Number of Questions: 25 **Section Marks: 30**

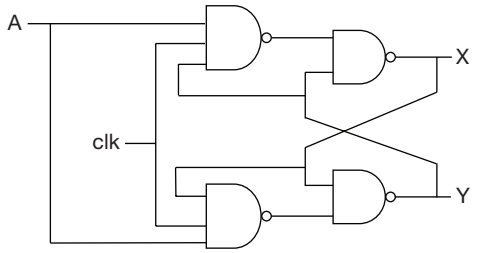
Directions for questions 1 to 25: Select the correct alternative from the given choices.

1. The ripple counter shown in figure works as a:



(A) Mod-6 up counter
(B) Mod-5 up counter
(C) Mod-5 down counter
(D) Mod-6 down counter

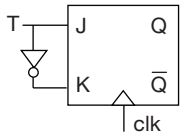
2. Consider the given circuit:

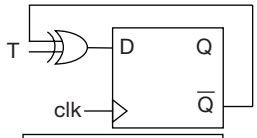


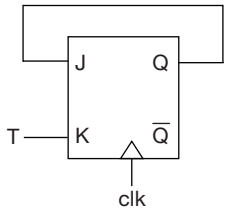
In this circuit, the race around condition
(A) does not occur
(B) occurs when clk = 0
(C) occurs when clk = 0, $A = 1$ and $X = Y = 1$
(D) occurs when clk = 1, $A = 1$

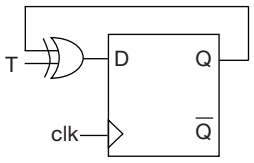
3. Three, modulo-4 counters are cascaded together then the resultant counter modulus is
(A) 3×4 (B) 3^4
(C) $4 \times 4 \times 4$ (D) $3 + 4$

4. Which of the following flip flop configuration works as *T* flip flop:

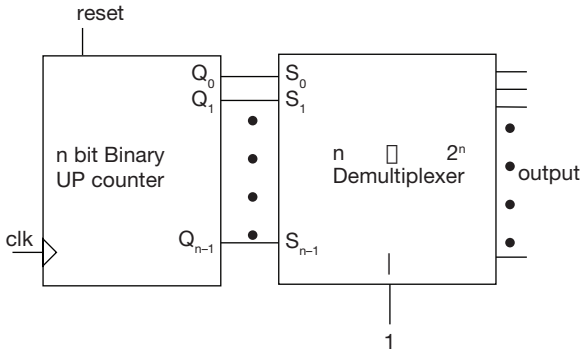
(A)


(B)


(C)


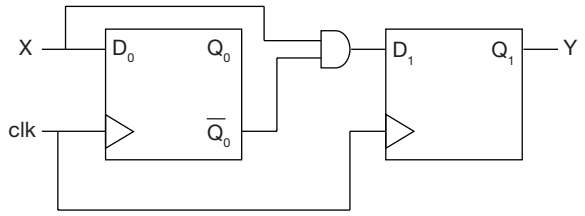
(D)


5.



'*n*' bit Binary UP counter is connected to $n \times 2^n$ Demultiplxer with input $I = 1$, as shown in the figure.
If the counter starts from reset, the above configuration works as
(A) Modulo – 2^n twisted ring counter
(B) Modulo – *n* ring counter
(C) Modulo – $2n$ Johnson counter
(D) Modulo – 2^n ring counter

6. Consider the following circuit with initial state $Q_0 = Q_1 = 0$. The *D* flip flops are positive edge triggered.



Consider the following timing diagrams of *X* and clk. Which one is the correct wave form of *Y*?

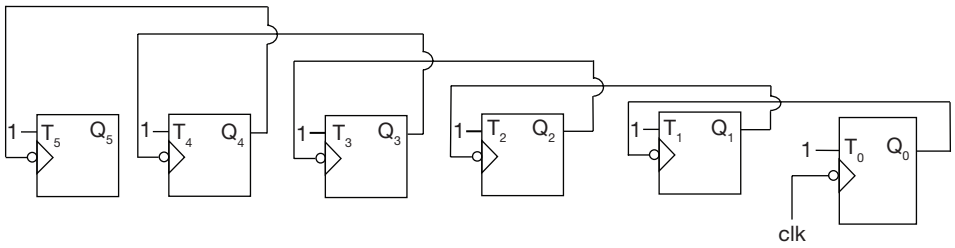
(A)


(B)


(C)


(D)

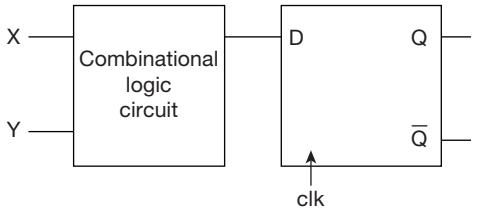

7. Six JK Flip flops are cascaded to form the circuit shown in figure. Clock pulses at a frequency of 128 kHz are applied as shown, The frequency (in kHz) of the wave form at Q_4 is _____.



(A) 32 kHz (B) 16 kHz
(C) 8 kHz (D) 4 kHz

8. The following truth table has to be realized with D flip flop.

XY	Q_{n+1}
0 0	Q_n
0 1	1
1 0	0
1 1	$\bar{Q}_n$

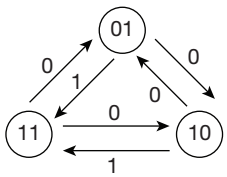


Then what is the equation of combinational logic circuit output in terms of X, Y and Q_n?

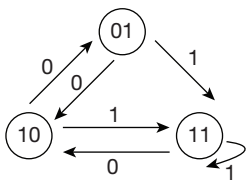
(A) $D = \bar{X}Q_n + Y\bar{Q}_n$ (B) $D = X\bar{Q}_n + \bar{Y}Q_n$
(C) $D = XY + Q_n$ (D) $D = (X + Y) + Q_n$

9. A clocked sequential circuit has 3 states A, B, C and 1 input X. As long as input $X = 0$, the circuit alternates between states A and B, if input $X = 1$ (either in state A or B), The circuit goes to state C and remain in state C as long as $X = 1$, from state C, circuit returns to state A when input $X = 0$, and then a repeats its behavior. Assume $A = 01$, $B = 10$, $C = 11$ the state diagram will be:

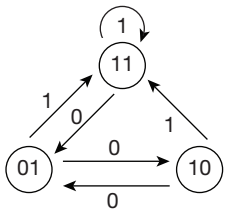
(A)



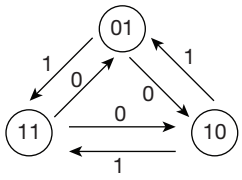
(B)



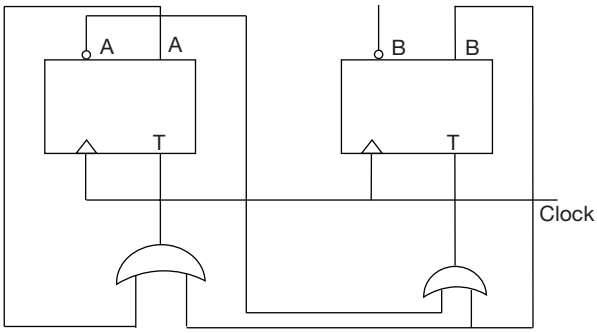
(C)



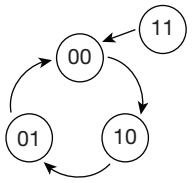
(D)



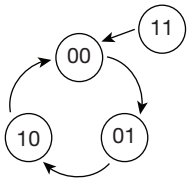
10. Find the state (AB) diagram for the following sequential circuit?



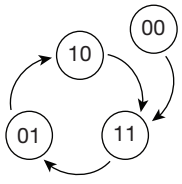
(A)



(B)

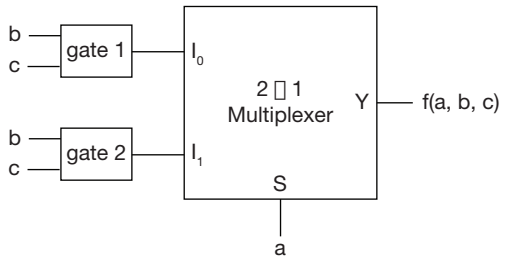


(C)



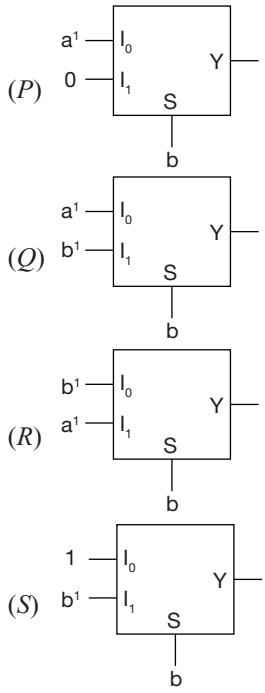
(D) None of these

11. The Boolean function $f(a, b, c) = a^1\, b + b^1\, c + ac^1$ has to be implemented by the following 2 × 1 multiplexer then the gate 1 and gate 2 are respectively?



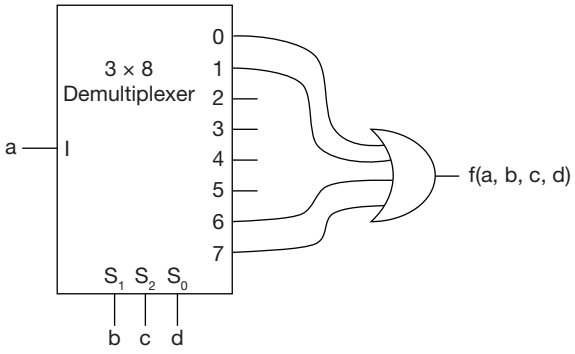
(A) OR, NAND
(B) AND, OR
(C) NOR, AND
(D) NAND, OR

12. Which of the following multiplexer implements 2 input NAND gate?



(A) Q, R
(B) P, R
(C) P, S
(D) R, S

13. The output of the following Demultiplexer circuit is:

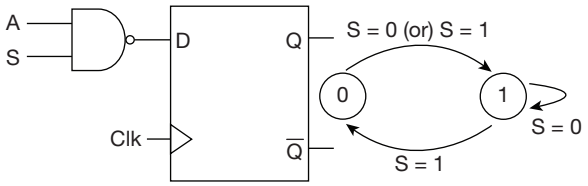


(A) $a(b \odot c)$
(B) $a(b \odot c)$
(C) $(a \odot b)c$
(D) $(a \odot b)c$

14. An 8 × 1 multiplexer has inputs A, B, C connected to the selection inputs S_2, S_1 and S_0 respectively. The data inputs I_0 through I_7 are as follows. $I_1 = I_2 = 0$; $I_3 = I_5 = I_7 = 1$; $I_0 = I_4 = D$; and $I_6 = D^1$ then the Boolean function that the multiplexer implements is?

(A) $AB + BC + A\bar{C}D + \bar{B}\bar{C}D$
(B) $AC + BD + A\bar{B}D + B\bar{C}\bar{D}$
(C) $\bar{B}\bar{C}D + AB\bar{D} + BC + AC$
(D) $A\bar{B}D + \bar{B}\bar{C}D + A\bar{C} + BC$

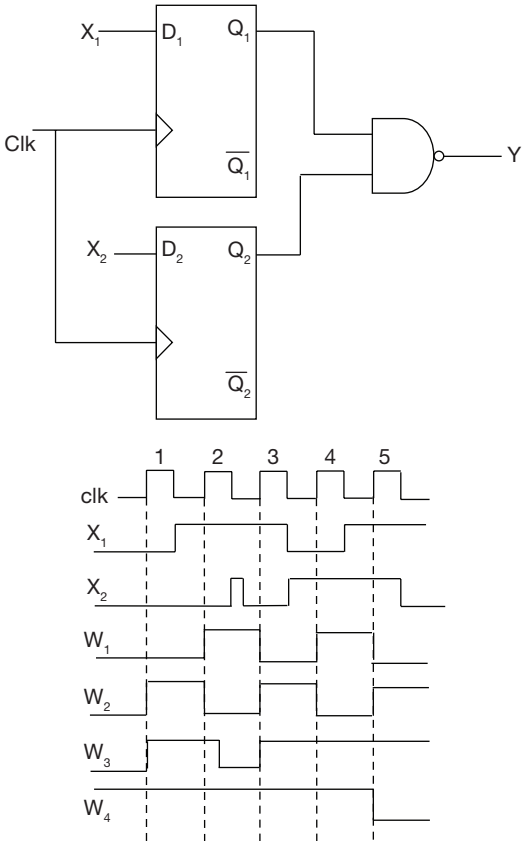
15. The digital circuit shown in the figure satisfies the given state diagram, when Q, is connected to input A of NAND gate



Suppose the NAND gate is replaced by an OR gate which are of the following options preserves the state diagram.

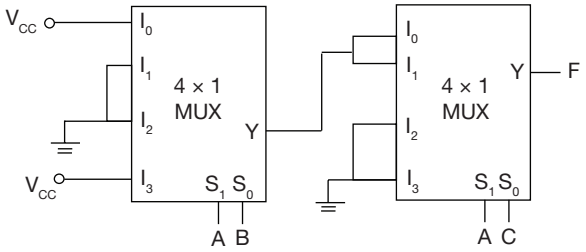
(A) input A is connected to $\bar{Q}$
(B) input A is connected to 1 and S is complemented
(C) input A is connected to S
(D) input A is connected to $\bar{Q}$ and S is complemented

16. In the circuit shown choose the correct timing diagram of output Y from the given wave forms W_1, W_2, W_3 and W_4



(A) W_1 (B) W_2
(C) W_3 (D) W_4

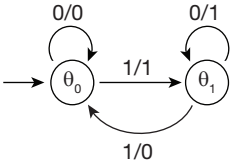
17. In the circuit shown the output F is given by:

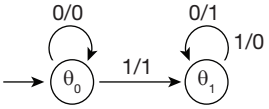


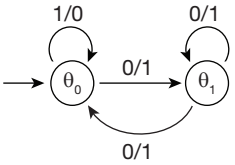
(A) $\bar{A} + \bar{B} + \bar{C}$ (B) ABC
(C) $\bar{A}B$ (D) $\overline{(A + B)}$

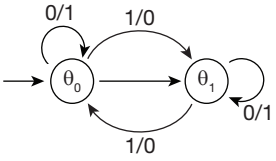
18. Suppose only one multiplexer and one inverter allowed to be used to implement any Boolean function of n variables. What is the minimum size of the multiplexer needed?
(A) 2^n line to 1 line (B) 2^{n-1} line to 1 line
(C) 2^{n-2} line to 1 line (D) 2^{n+1} line to 1 line

19. Which one of the following state diagram represents finite state machine, which takes as input a binary number from the least significant bit and computes 2's complement of the input number.

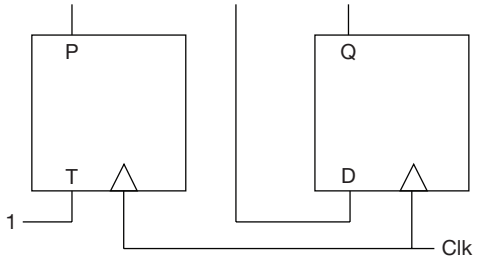
(A)


(B)


(C)


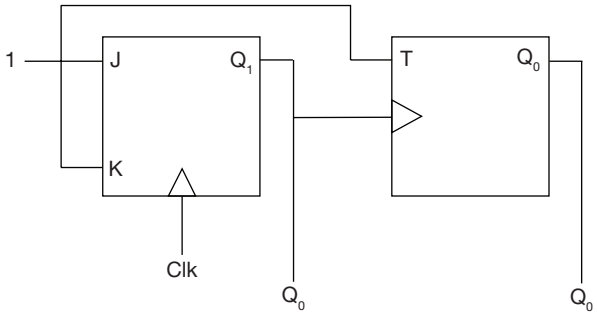
(D)


20. The following arrangement of Master-slave flip flips has the initial state of P, Q as 0, 1 respectively after the 3 clock pulses, the output states P, Q is:



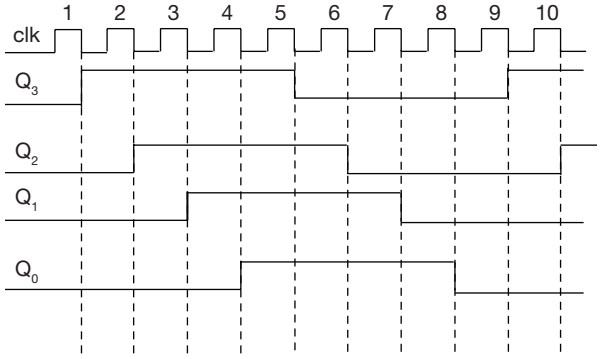
(A) 1, 0 (B) 0, 1
(C) 1, 1 (D) 0, 0

21. In the sequential circuit below, if the initial value of the output Q_1 Q_0 is 00, what are the next four values Q_1, Q_0?



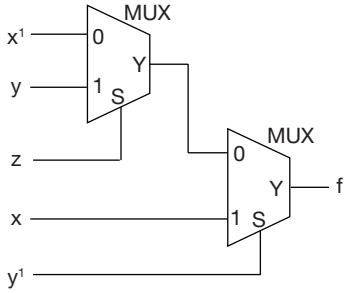
(A) 01, 10, 11, 00
(B) 11, 10, 01, 00
(C) 01, 11, 10, 00
(D) 10, 11, 01, 00

22. The waveforms of a counter are shown below, this is a



(A) synchronous *BCD* counter
(B) ripple counter
(C) ring counter
(D) twisted ring counter

23. Consider the circuit, here, which are the following options correctly represents $f(x, y, z)$



(A) $x^1y^1 + xy + xz$
(B) $xy^1 + x^1y + xz$
(C) $x^1y + xy^1 + y^1z$
(D) $xy + x^1y^1 + xyz$

24. The outputs Q and $\overline{Q}$ of a master slave SR flip flop are connected to its R and S inputs respectively. Its output Q when clock pulses are applied will be:

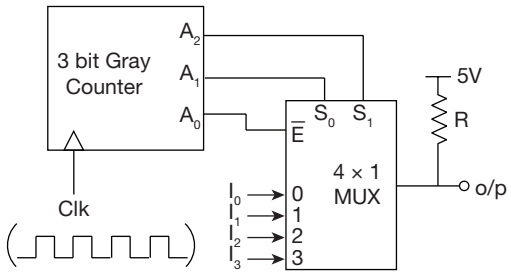
(A) permanently 0

(B) permanently 1

(C) fixed 0 or 1

(D) complementing with every clock pulse

25. A 3 bit gray counter is used to control the output of the multiplexer as shown in figure, the initial state of the counter is 000. The output is pulled high, the output of the circuit follows the sequence



(A) $1, I_0, I_1, 1, 1, I_3, I_2, 1, 1$

(B) $I_0, 1, 1, I_1, I_3, 1, 1, I_2, I_0$

(C) $I_0, 1, I_1, 1, I_2, 1, I_3, 1, I_0,$

(D) $1, I_0, 1, I_1, I_2, 1, I_3, 1, I$

Answer Keys

1. D	**2.** D	**3.** C	**4.** D	**5.** D	**6.** A	**7.** D	**8.** A	**9.** C	**10.** B
11. A	**12.** D	**13.** B	**14.** C	**15.** D	**16.** D	**17.** D	**18.** B	**19.** B	**20.** A
21. B	**22.** D	**23.** B	**24.** D	**25.** B					

Hints and Explanations

1. All flip flops have $J = K = 1$, so all are toggle switches
The output of flip flop is connected to rising edge clk input of next flip flop, so Down counter. clk input is given to flip flop A (LSB).
Preset is active high, so as preset = 1, all flip flops get 111, so AND gate $o/p = 1$, when $A = 1$, $B = 0$, $C = 0$ as $A, \overline{B}, \overline{C}$ are inputs, so the $CBA = 001$,
modulus = 111 – 001 = 6. Choice (D)

2. The given circuit is T latch, The input A is connected to first two NAND gates (J, K inputs connected together to make T latch)
So race around condition occurs when $A = 1$, clk = 1.
Choice (D)

3. When two counters are connected in cascade, the resultant modulus is the multiplication of the individual modulus.
So 3 counters are connected so resultant modulus
$= 4 \times 4 \times 4 = 64$. Choice (C)

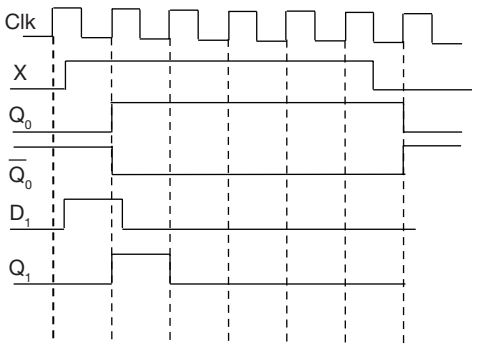
4. JK flip flop works as T flip flop if $J = K = T$
For D flip flop $Q_{n+1} = D$, $Q_{n+1} = T \oplus Q_n$ (T flip flop)
So by taking $D = T \oplus Q_n$ we get T flip flop.
Choice (D)

5. n bit binary UP counter counts in Binary sequence, so same binary sequence is applied to Demultiplexer, so input $I = 1$, will be at output in sequence, for 3 bit example.

$Q_2\ Q_1\ Q_0$	$S_2\ S_1\ S_0$	$Y_0\ Y_1\ Y_2$ ..... Y_7
0 0 0	0 0 0	1 0 0 0
0 0 1	0 0 1	0 1 0 0
0 1 0	0 1 0	0 0 1 0

It works like a module 2^n ring counter. Choice (D)

6. For D flip flop whatever input we apply, same output we get after clk pulse



Choice (A)

7. The frequency of $Q_1 = \dfrac{fclk}{2}$

$$\text{Frequency of } Q_1 = \frac{\frac{fclk}{2}}{2} = \frac{fclk}{4}$$

$$\text{Frequency of } Q_2 = \frac{\frac{fclk}{4}}{2} = \frac{fclk}{8}$$

$$\text{Frequency of } Q_3 = \frac{fclk}{16}$$

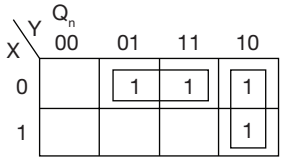
$$\text{Frequency of } Q_4 = \frac{fclk}{32} = \frac{128}{32} = 4 \text{ kHz}$$

$$\text{Frequency of } Q_5 = \frac{fclk}{64}$$

Choice (D)

8. The given XY flip flop truth table is

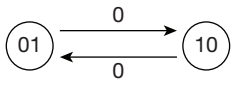
$X\ Y\ Q_n$	Q_{n+1}
0 0 0	0
0 0 1	1
0 1 0	1
0 1 1	1
1 0 0	0
1 0 1	0
1 1 0	1
1 1 1	0

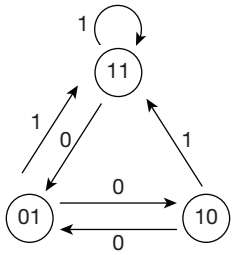


$Q_{n+1} = \bar{X}Q_n + Y\bar{Q}_n$

The characteristic equation of D flip flop is $Q_{n+1} = D$, This has to work like above XY flip flop. By equating $Q_{n+1} = D = \bar{X}Q_n + Y\bar{Q}_n$. Choice (A)

9. $A = 01$, $B = 10$, alternate states when $X = 0$
When $X = 1$, A, B go to state $C = 11$ as long as $X = 1$, C will remain in same state

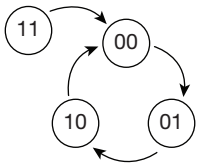




When $X = 0$, C will return to state $A = 01$ Choice (C)

10. Let us consider states as AB if initially state of the circuit is 00 (reset)

Clk	A B	T_A (A + B)	T_B (A^1 + B)	
0 1 2 3	0 0 0 1 1 0 0 0	0 1 1	1 1 0	If initially at 00 state, after 3 Clk pulses it comes back to same state 00.
0 1	1 1 0 0	1	1	If initial state is 11, it goes to 00 state after clock pulse



Choice (B)

11. Given $f(a, b, c) = a^1b + b^1c + ac^1$
$= a^1b + (a + a^1)b^1c + ac^1$
$= a^1b + a^1b^1c + ab^1c + ac^1$
$= a^1[b + b^1c] + a[b^1c + c^1]$
$= a^1[b + c] + a[b^1 + c^1]$
By comparing this equation with output of 2 × 1 multiplexer
$Y = I_0\ \bar{S} + l_1\ S = I_0\bar{a} + I_1a = [b + c]a^1 + [\overline{bc}]a$
Gate 1 is OR gate, gate 2 is NAND gate.
Choice (A)

12. For multiplexer P, $Y = I_0\ I_0\bar{S} + I_1S = a^1\ b^1 + 0 \cdot b$
For mux, Q $Y = a^1\ b^1 + b^1 \cdot b = a^1\ b^1$
For mux, R, $Y = b^1.b^1 + a^1 \cdot b = a^1 + b^1 = (ab)^1$
For mux, S, $Y = 1 \cdot a^1 + b^1 \cdot a = a^1 + b^1 = (ab)^1$
So, R, S implement NAND gate P, Q implements NOR gate. Choice (D)

13. The demultiplexer output $Y_0 = I\bar{S}_2\bar{S}_1\bar{S}_0$

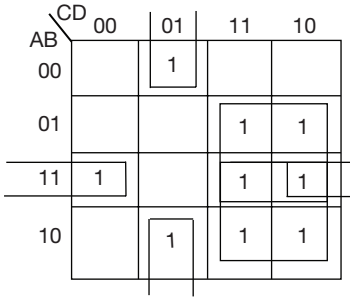
$Y_1 = I\bar{S}_2\bar{S}_1S_0$

$Y_2 = I\bar{S}_2S_1\bar{S}_0$

$Y_3 = IS_2\bar{S}_1\bar{S}_0$... ... etc

$f(a, b, c, d) = Y_0 + Y_1 + Y_6 + Y_7$
$= ab^1c^1d^1 + ab^1c^1d + abcd^1 + abcd$
$= ab^1c^1 + abc$
$= a[b \odot c]$ Choice (B)

14. For 8 × 1 multiplexer output
$Y = l_0\bar{S}_2\bar{S}_1\bar{S}_0 + I_1\bar{S}_2\bar{S}_1S_0 + I_2\bar{S}_2S_1\bar{S}_0 + I_3\bar{S}_2S_1S_0$
$+ I_4S_2\bar{S}_1\bar{S}_0 + I_5S_2\bar{S}_1S_0 + I_6S_2S_1\bar{S}_0 + I_7S_2S_1S_0$
$= \bar{A}\bar{B}\bar{C}D + 0 + 0 + \bar{A}BC + A\bar{B}\bar{C}D + A\bar{B}C$
$+ AB\bar{C}\bar{D} + ABC$
$= \sum m\,(1, 6, 7, 9, 10, 11, 12, 14, 15)$



$Y = \bar{B}\bar{C}D + AB\bar{D} + BC + AC$ Choice (C)

15. The input $D = \overline{A \cdot S} = \bar{A} + \bar{S}$
This NAND gate is replaced by OR gate
So A input should be complemented (to $\bar{Q}$) and S input should be complemented. Choice (D)

16. NAND gate output = 0
When two inputs are 1.
Only at last clk pulse $X_1 = X_2 = 1$
So $Y = 0$, remaining cases $Y = 1$, Choice (D)

17. Output of 1st multiplexer is
$Y = I_0\bar{A}\bar{B} + I_1\bar{A}B + I_2A\bar{B} + I_3AB$
$= \bar{A}\bar{B} + AB = A \odot B$
Output of 2nd multiplexer is
$Y = (A \odot B)\,\bar{A}\bar{C} + (A \odot B)\,\bar{A}\,C + 0 \cdot A\bar{C} + 0 \cdot AC$
$= (A \odot B)[\bar{A}\bar{C} + \bar{A}C] = (\bar{A}\bar{B} + AB)\bar{A}$
$= \bar{A}\bar{B} = (\overline{A + B})$ Choice (D)

18. Choice (B)

19. If two 2's complement has to be calculated we require two states.

(Inputs)	0	1
$Q_0(0)$	Q_0, 0	Q_1, 1
$Q_1(1)$	Q_1, 1	Q_1, 0

We can get 2's complement from LSB, by considering all zero's and the first 1 as it is, there after complementing 0's and 1's. Choice (B)

20.

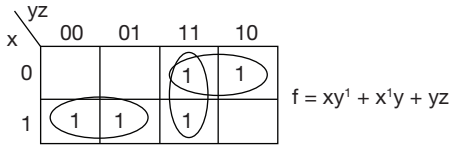
Clk	States	Input
	P Q	T D
0	0 1	1 0
1	1 0	1 1
2	0 1	1 0
3	1 0	1 1

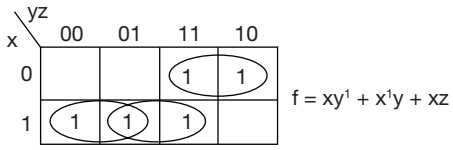
Choice (A)

21. The given circuit is an asynchronous counter (ripple counter) states will change in Binary sequence. Q is connected to rising edge clk pulse so down counter, so sequence is 00, 11, 10, 01, 00 ... Choice (B)

22. By observing sequence 0000 → 1000 → 1100 → 1110 → 1111 → 0111 → 0011 → 0001 → 0000
It is twisted ring counter. Choice (D)

23. Output of 1st multiplexer $Y = I_0\bar{S} + I_1S = x^1\,z^1 + yz$
Output of 2nd multiplexer $Y = I_0\bar{S} + I_1S$
$= (x^1\,z^1 + yz)\,(y^1)^1 + xy^1$
$= x^1yz^1 + yz + xy^1 = \sum m\,(2, 3, 4, 5, 7)$





Choice (B)

24. Q is connected to R, $\bar{Q}$ to S input
So $Q_{n+1} = S + \bar{R}Q_n = \bar{Q}_n + \bar{Q}_n \cdot Q_n$
So $Q_{n+1} = \bar{Q}_n$ so next state is complement of present state. Choice (D)

25.

$A_2\,A_1\,A_0$	E S_1 S_0	o/p
0 0 0	0 0 0	I_0
0 0 1	1 0 0	1
0 1 1	1 0 1	1
0 1 0	0 0 1	I_1
1 1 0	0 1 1	I_3
1 1 1	1 1 1	1
1 0 1	1 1 0	1
1 0 0	0 1 0	I_2
0 0 0	0 0 0	I_0

Enable is active low, when $E = 1$, the output is logic 1
When $E = 0$, output is from multiplexer. Choice (B)