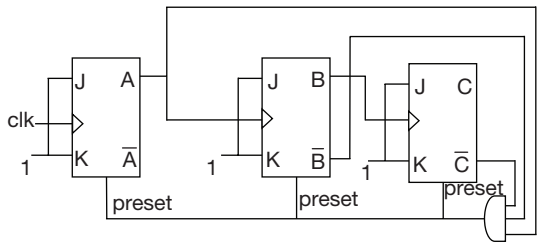
Analog and Digital Electronics Test 2

Number of Questions: 25 **Section Marks: 25**

Directions for questions 1 to 25: Select the correct alternative from the given choices.

1. The ripple counter shown in figure works as a



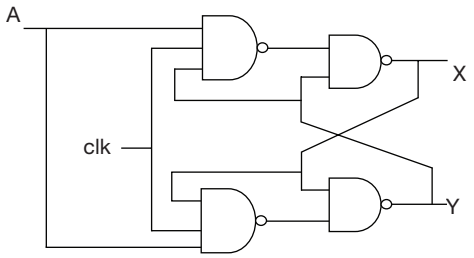
(A) Mod-6 up counter
(B) Mod-5 up counter
(C) Mod-5 Down counter
(D) Mod-6 Down counter

2. The minimized POS expression for k-map shown is

CD \ AB	00	01	11	10
00	0		0	X
01	X		X	X
11	0		0	0
10	0		0	0

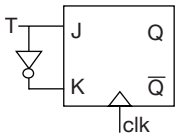
(A) $\overline{A}+B$
(B) $\overline{A}\,B$
(C) $(\overline{A}+\overline{B})(\overline{A}+B)(A+B)$
(D) $\overline{A}(A+B)$

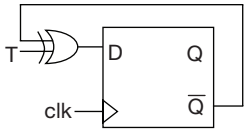
3. Consider the given circuit

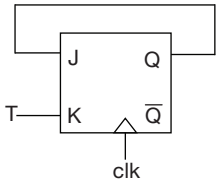


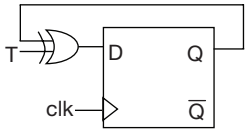
In this circuit, the race around condition
(A) does not occur
(B) occurs when clk = 0
(C) occurs when clk = 0, $A = 1$ and $X = Y = 1$
(D) occurs when clk = 1, $A = 1$

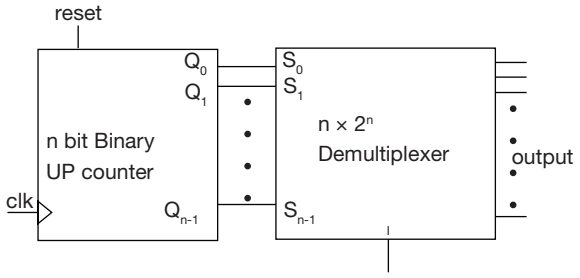
4. Which of the following flipflop configuration works as T flip flop:

(A)


(B)


(C)


(D)


5.


'n' bit Binary UP counter is connected to $n \times 2^n$ Demultiplxer with input $I = 1$, as shown in the figure. If the counter starts from reset, the above configuration works as
(A) Modulo – 2^n twisted ring counter
(B) Modulo – n ring counter
(C) Modulo – $2n$ Johnson counter
(D) Modulo – 2^n ring counter

6. $f(a, b, c) = ab + b_1c$ in the canonical POS form is represented as
(A) $(a + b + c)\,(a + b + c^1)\,(a + b^1 + c)\;\;(a^1 + b^1 + c)$
(B) $(a + b^1 + c)\,(a + b^1 + c^1)\,(a + b + c)\,(a^1 + b + c)$
(C) $(a + b + c)\,(a^1 + b^1 + c)\,(a + b^1 + c)$
(D) $(a^1 + b + c)\,(a^1 + b^1 + c)\,(a + b + c)\,(a + b^1 + c)$

7. The Essential prime Implicants of the function $f(A, B, C, D) = \overline{A}\,C + ABD + \overline{A}\,B + \overline{B}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}\,D$ are

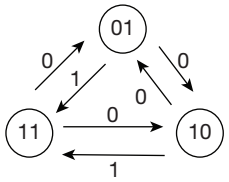
(A) $BD, \overline{B}\,\overline{D}, \overline{A}$ (B) $\overline{A}C, \overline{B}\,\overline{D}, B$
(C) $BD, \overline{A}C, \overline{B}$ (D) $\overline{A}\,\overline{B}, \overline{B}\,\overline{D}, C$

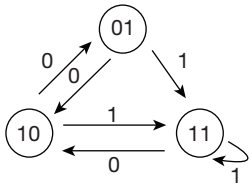
8. A combinational circuit has 3 inputs x, y, z and three outputs A, B, C. When the binary input is 4, 5, 6 and 7, the binary output is 2 less than the binary input. When

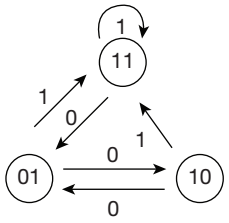
the binary input is 0, 1, 2 and 3, the output is 4 more than the binary input the Boolean expression for output A and C respectively are?

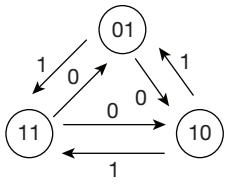
(A) $x^1 y, z$
(B) $x + y^1, z^1$
(C) x, z
(D) $x^1 + y, z$

9. A clocked sequential circuit has 3 states A, B, C and 1 input X. As long as input $X = 0$, the circuit alternates between states A and B, if input $X = 1$(either in state A or B), The circuit goes to state C and remain in state C as long as $X = 1$, from state C, circuit returns to state A when input $X = 0$, and then a repeats its behavior. Assume $A = 01$, $B = 10$, $C = 11$ the state diagram will be?

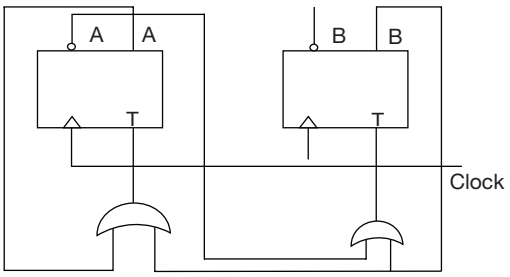
(A)


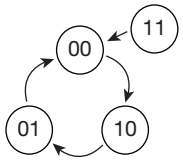
(B)


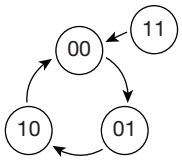
(C)


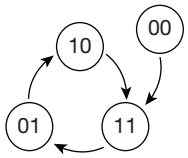
(D)


10. Find the state (AB) diagram for the following sequential circuit?



(A)


(B)


(C)


(D) None

11. The following program is intended to clear memory locations starting from memory address 0000H. How many memory locations will be cleared? ($A = 01$H)

```
        LXI   H, 0010H
        ORA   A
loop:   MVI   M,00H
        DCX   H
        JNZ   loop
        HLT
```

(A) 10
(B) 9
(C) 16
(D) a large memory block will be erased

12. The following program reads one data byte (X) at a time from input port1.

```
IN      PORT1
MVI     B, 20H
CMP     B
JC      REJECT
JM      REJECT
STA     3010H
JMP     ACCEPT
REJECT: JMP INVALID
```

Indentify the range of number is Decimal that will transfer the program to location INVALID.

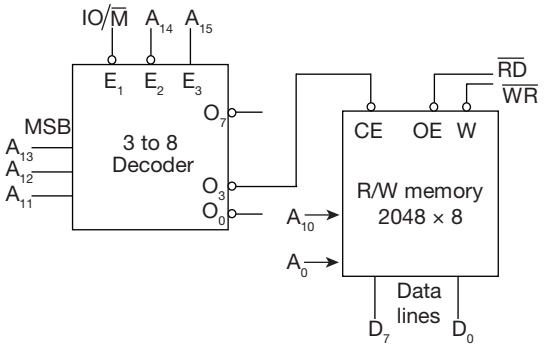
(A) $20H < X < A0H$
(B) $X < 20H$ and $X > A0H$
(C) $X < 32$ and $X > 160$
(D) $32 < X < 160$

13. At the end of the following program?

```
LXI     SP, 31AE H
MOV     C, 00H
PUSH    B
POP     PSW
RET
```

(A) The contents of Accumulator has been reset
(B) All the flags has been reset
(C) The contents of Accumulator and Register B has been swapped.
(D) Program status word is loaded on stack.

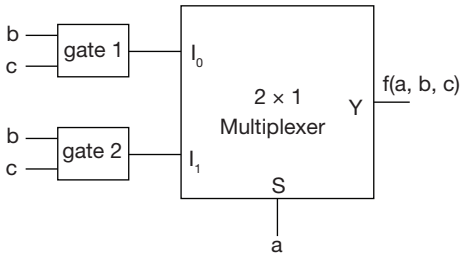
14.



A *R*/*W* memory is interfaced with 8085 microprocessor as shown. What is the range of memory map connected to O_3 line.

(A) 6800 – 6FFFH (B) 9000 – 98FFH
(C) 9800 – 9FFFH (D) 2300 – 2FFFH

15. The Boolean function $f(a, b, c) = a^1 b + b^1 c + ac^1$ has to be implemented by the following 2 × 1 multiplexer then the gate1 and gate 2 are respectively?



(A) OR, NAND (B) AND, OR
(C) NOR, AND (D) NAND, OR

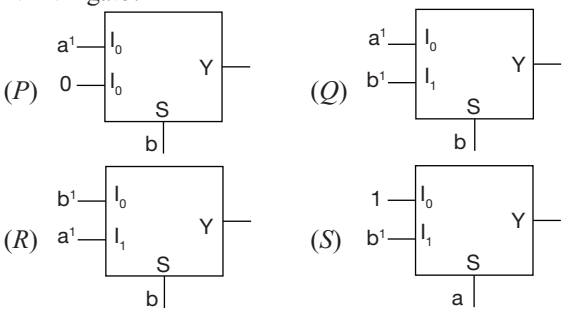
16. The resolution of a *D*/*A* converter is approximately 0.4 percent of its full scale range, It is

(A) an 8 bit converter (B) a 10 bit converter
(C) a 12 bit converter (D) a 16 bit converter

17. For a 12 bit *A*/*D* converter the range of input signal is 0 to +10V. The voltage corresponding to 1 LSB will be?

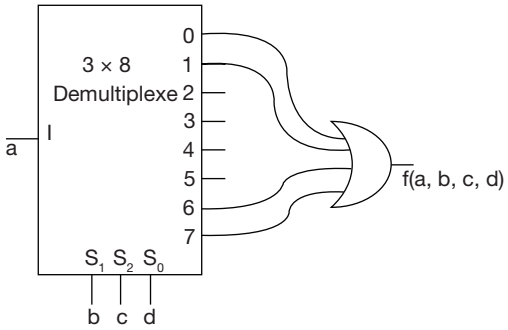
(A) 0 (B) 0.0012V
(C) 0.0024V (D) 0.833V

18. Which of the following multiplexer implements 2 input NAND gate?



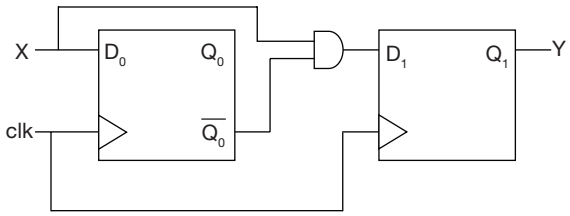
(A) *Q*, *R* (B) *P*, *R*
(C) *P*, *S* (D) *R*, *S*

19. The output of the following Demultiplexer circuit is

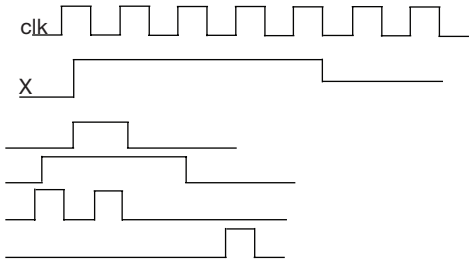


(A) $a(b \odot c)$ (B) $a(b \odot c)$
(C) $(a \odot b)c$ (D) $(a \odot b)c$

20. Consider the following circuit with initial state $Q_o = Q_1 = 0$. The *D* flipflops are positive edge triggered.



Consider the following timing diagrams of *X* and clk. Which one is the correct wave form of *Y*?



21. A *D*/*A* converter has 5V full scale output voltage and an accuracy of +0.2%, the maximum error for any output voltage will be

(A) 5mV (B) 10mV
(C) 20mV (D) 30mV

22. An 8 × 1 multiplexer has inputs *A*, *B*, *C* connected to the selection inputs S_2, S_1 and S_0 respectively. The data inputs I_0 through I_7 are as follows. $I_1 = I_2 = 0$; $I_3 = I_5 = I_7 = 1$; $I_0 = I_4 = D$; and $I_6 = D^1$ then the Boolean function that the multiplexer implements is?

(A) $AB + BC + A\overline{C}D + \overline{B}\,\overline{C}\,D$

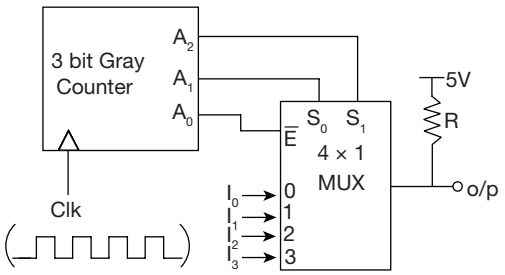
(B) $AC + BD + A\overline{B}\,D + B\overline{C}\,\overline{D}$

(C) $\overline{B}\overline{C}\,D + A\,B\,\overline{D} + BC + AC$

(D) $A\,\overline{B}\,D + \overline{B}\,\overline{C}\,D + A\overline{C} + BC$

23. A 3 bit gray counter is used to control the output of the multiplexer as shown in figure, the initial state of the

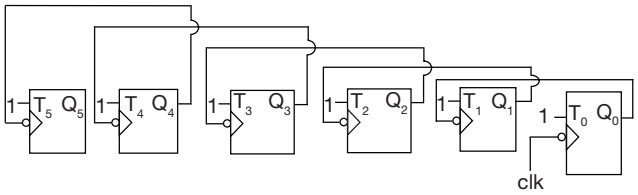
counter is 000. The output is pulled high, the output of the circuit follows the sequence



(A) $1, I_0, I_1, 1, 1, I_3, I_2, 1, 1$
(B) $I_0, 1, 1, I_1, I_3, 1, 1, I_2, I_0$
(C) $I_0, 1, I_1, 1, I_2, 1, I_3, 1, I_0,$
(D) $1, I_0, 1, I_1, I_2, 1, I_3, 1, I$

24. The waveforms of a counter are shown below, this is a
(A) synchronous BCD counter
(B) ripple counter
(C) ring counter
(D) twisted ring counter

25. Six *JK* Flip flops are cascaded to form the circuit shown in figure. Clock pulses at a frequency of 128 kHz are applied as shown, The frequency (in kHz) of the wave form at Q_4 is _____



(A) 32 kHz (B) 16 kHz
(C) 8 kHz (D) 4 kHz

Answer Keys

1. D	**2.** B	**3.** D	**4.** D	**5.** D	**6.** B	**7.** A	**8.** D	**9.** C	**10.** B
11. D	**12.** C	**13.** B	**14.** C	**15.** A	**16.** A	**17.** C	**18.** D	**19.** B	**20.** A
21. B	**22.** C	**23.** B	**24.** D	**25.** D					

Hints and Explanations

1. All flipflops have $J = K = 1$, so all are toggle switches
The output of flipflop is connected to rising edge clk input of next flip flop, so Down counter. clk input is given to flip flop A. (LSB).
Preset is active high, so as preset = 1, all flip flops get 111, so AND gate $o/p = 1$, when $A = 1$, $B = 0$, $C = 0$ as $A, \overline{B}, \overline{C}$ are inputs, so the $CBA = 001$,
modulus = 111 – 001 = 6. Choice (D)

2. Two octates present so minimized expression is $\overline{A}.B$

CD \ AB	00	01	11	10
00	0		X	X
01	X		X	X
11	0		0	0
10	0		0	0

Choice (B)

3. The given circuit is T latch, The input A is connected to first two NAND gates (J, K inputs connected together to make T latch)
So race around condition occurs when $A = 1$, clk = 1.
Choice (D)

4. *JK* flip flop works as T flip flop if $J = K = T$
For D flip flop $Q_{n+1} = D$, $Q_{n+1} = T \oplus Q_n$ (T flip flop)
So by taking $D = T \oplus Q_n$ we get T flip flop.
Choice (D)

5. n bit binary UP counter counts in Binary sequence, so same binary sequence is applied to Demultiplexer, so input $I = 1$, will be at output in sequence, for 3 bit example.

$Q_2\ Q_1\ Q_0$	$S_2\ S_1\ S_0$	$Y_0\ Y_1\ Y_2 \ldots . Y_7$
0 0 0	0 0 0	1 0 0 0
0 0 1	0 0 1	0 1 0 0
0 1 0	0 1 0	0 0 1 0

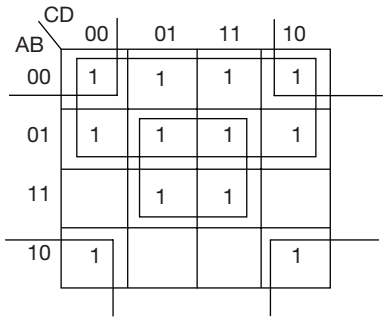
It works like a module 2^n ring counter. Choice (D)

6. $f(a, b, c) = ab + b^1.c$
$= (ab + b^1)(ab + c)$ $[x + yz = (x + y)(x + z)]$
$= (a + b^1)(a + c)(b + c)$
$= (a + b^1 + c.c^1)(a + b.b^1 + c)(a.a^1 + b + c)$
$= (a + b^1 + c)(a + b^1 + c^1)(a + b + c)(a + b^1 + c)(a + b + c)$
$(a^1 + b + c)$
$= (a + b^1 + c)(a + b^1 + c^1)(a + b + c)(a^1 + b + c)$
Choice (B)

7. $f(A, B, C, D) = \overline{A}\,C + ABD + \overline{A}\,B + \overline{B}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}\,D$

Product term	Equivalent	Min terms
$\overline{A}C$	0X1X	0010, 0011, 0110, 0111
ABD	11X1	1101, 1111
$\overline{A}B$	01XX	0100, 0101, 0110, 0111
$\overline{B}\,\overline{D}$	X0X0	0000, 0010, 1000, 1010
$\overline{A}\,\overline{B}\,\overline{C}D$	0001	0001

$f(A, B, C, D) = \sum m(0, 1, 2, 3, 4, 5, 6, 7, 8, 10, 13, 15)$

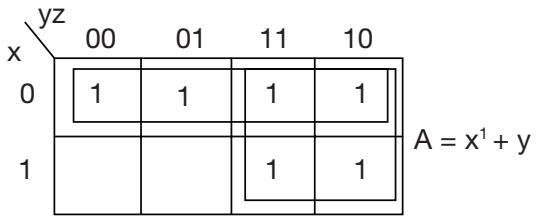


$f(A, B, C, D) = \overline{A} + BD + \overline{B}\,\overline{D}$

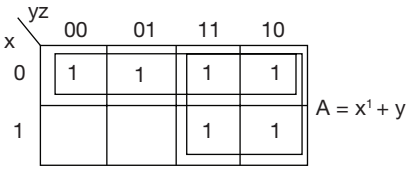
Essential prime implicants are $\overline{A}$, BD, $\overline{B}\,\overline{D}$

Choice (A)

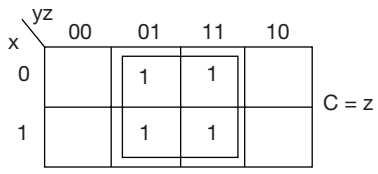
8. The truth table is



$A(x, y, z) = \sum m(0, 1, 2, 3, 6, 7)$
$B(x, y, z) = \sum m(2, 3, 4, 5)$
$C(x, y, z) = \sum m(1, 3, 5, 7)$
The k map for A

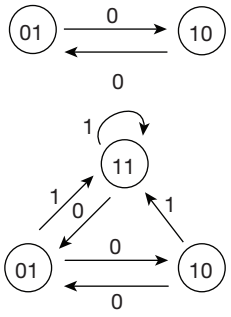


The k map for C



Choice (D)

9. $A = 01$, $B = 10$, alternate states when $X = 0$

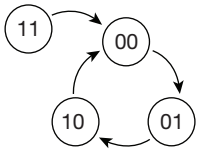


When $X = 1$, A, B go to state $C = 11$ as long as $X = 1$, C will remain in same state
When $X = 0$, C will return to state $A = 01$

Choice (C)

10. Let us consider states as AB if initially state of the circuit is 00 (reset)

Clk	A B	T_A (A + B)	T_B (A^1 + B)	
0 1 2 3	0 0 0 1 1 0 0 0	0 1 1	1 1 0	If initially at 00 state, after 3 Clk pulses it comes back to same state 00.
0 1	1 1 0 0	1	1	If initial state is 11, it goes to 00 state after clock pulse



Choice (B)

11. LXI H, 0010 H → Load HL = 0010
ORA A → OR Accumulator with itself
A = A + A → contents will be same but flags will change as per result So Z = 0, (A ≠ 00H)
MVI M, 00H → Copy 00H to memory location M address specified by HL register pair.
DCX H → Decrement HL register pair but this instruction will not effect the flags.
JNZ loop – If No zero flag go to loop, else Halt.
but zero flag = 1 because ORA A instruction and this will iterate infinitely and a large memory block will be erased. Choice (D)

12. IN Port 1 – take input from port 1 to Accumulator
MVI B, 20 H → Copy 20H to B = B = 20 H
CMP B → compare B with Accumulator
This will be performed by subtraction of (Accumulator – B) if input byte is X, then as per X – B the flags will be effected.
We will get a carry flag when X – 20H < 00H [CY = 1]
We will get a sign flag when X – 20 > 80H [S = 1]
JC REJECT – Jump on carry to REJECT location ($CY = 1$)

JM REJECT – Jump as Minus to REJECT location (S = 1)
So X < 20H = $(32)_D$
X > A0H = $(160)_D$ Choice (C)

13. LXI SP, 31AEH → load SP = 31AE, initialization of stack pointer
MOV C, 00H → The contents of C were reset C = 00H
PUSH B → The contents of BC register pair loaded on top of stack.
POP PSW → retrieve the top of stack (now BC) to program status word (Accumulator + Flag register)
So Accumulator = B, Flags = C = 00H
So contents of flag register were made reset.
Choice (B)

14. For the decoder to be enabled $E_2 = A_M = 0$, $E_3 = A_{15} = 1$, $E_1 = IO/\overline{M} = D$ for memory operation
Address range is to select O_3, $A_{13}\,A_{12}\,A_{11} - 011$

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7.....A_0
1	0	0	1	1	0	0	0	0.....0 → 9800H
1	0	0	1	1	1	1	1	1.....1 → 9FFFH

Choice (C)

15. Given $f(a, b, c) = a^1b + b^1c + ac^1$
$= a^1b + (a + a^1)b^1c + ac^1$
$= a^1b + a^1b^1c + ab^1c + ac^1$
$= a^1[b + b^1c] + a[b^1c + c^1]$
$= a^1[b + c] + a[b^1 + c^1]$
By comparing this equation with output of 2 × 1 multiplexer
$Y = I_0\,\overline{S} + I_1\,S = I_0\,\overline{a} + I_1\,a = [b + c]a^1 + \overline{[bc]}\,a$
Gate 1 is OR gate, gate 2 is NAND gate.
Choice (A)

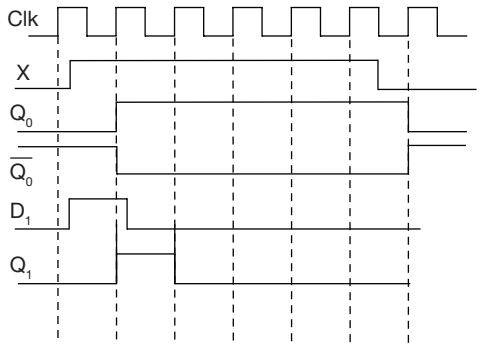
16. Resolution = 0.4% of full scale
$= \frac{0.4}{100} \times F.S.V$
$= \frac{FSV}{250}$
Resolution $= \frac{FSV}{2^n}$
So $2^n \approx 250$ approximately $n = 8$
Choice (A)

17. Resolution = 1 LSB $= \frac{FSV}{2^{12}} = \frac{10}{2^{12}} = \frac{10}{4096}$
$= 0.0024$V Choice (C)

18. For multiplexer P, $Y = I_0\,\overline{S} + I_1 S = a^1\,b^1 + 0.b$
For mux, Q $Y = a^1\,b^1 + b^1.b = a^1\,b^1$
For mux, R, $Y = b^1.b^1 + a^1.b = a^1 + b^1 = (ab)^1$
For mux, S, $Y = 1.a^1 + b^1.a = a^1 + b^1 = (ab)^1$
So, R, S implement NAND gate P, Q implements NOR gate. Choice (D)

19. The demultiplexer output $Y_0 = I\,\overline{S_2}\,\overline{S_1}\,\overline{S_0}$
$Y_1 = I\,\overline{S_2}\,\overline{S_1}\,S_0$
$Y_2 = I\,\overline{S_2}\,S_1\,\overline{S_0}$
$Y_3 = I\,S_2\,\overline{S_1}\,\overline{S_0}$ …. Etc
$f(a, b, c, d) = Y_0 + Y_1 + Y_6 + Y_7$
$= ab^1c^1d^1 + ab^1c^1d + abcd^1 + abcd$
$= ab^1c^1 + abc$
$= a[b \odot c]$ Choice (B)

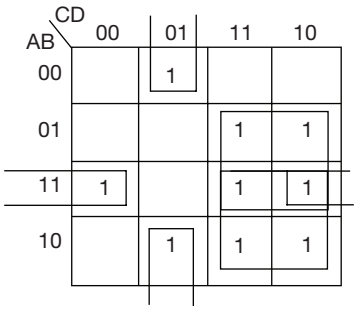
20. For D flip flop whatever input we apply, same output we get after clk pulse



Choice (A)

21. Error = Full scale output × Accuracy
$= 5\text{V} \times \frac{0.2}{100} = 10\text{mV}$ Choice (B)

22. For 8 × 1 multiplexer output
$Y = I_0\,\overline{S_2}\,\overline{S_1}\,\overline{S_0} + I_1\,\overline{S_2}\,\overline{S_1}\,S_0 + I_2\,\overline{S_2}\,S_1\,\overline{S_0} +$
$I_3\,\overline{S_2}\,S_1\,S_0 + I_4\,S_2\,\overline{S_1}\,\overline{S_0}$
$+ I_5\,S_2\,\overline{S_1}\,S_0 + I_6\,S_2\,S_1\,\overline{S_0} + I_7\,S_2\,S_1\,S_0$
$= \overline{A}\,\overline{B}\,\overline{C}\,D + 0 + 0 + \overline{A}\,BC + A\overline{B}\,\overline{C}\,D + A\,\overline{B}\,C +$
$AB\overline{C}\,\overline{D} + ABC$
$= \sum m(1, 6, 7, 9, 10, 11, 12, 14, 15)$



$Y = \overline{B}\,\overline{C}\,D + AB\overline{D} + BC + AC$ Choice (C)

23.

$A_2\ A_1\ A_0$	$E\ S_1\ S_0$	o/p
0 0 0	0 0 0	I_0
0 0 1	1 0 0	1
0 1 1	1 0 1	1
0 1 0	0 0 1	I_1
1 1 0	0 1 1	I_3
1 1 1	1 1 1	1
1 0 1	1 1 0	1
1 0 0	0 1 0	I_2
0 0 0	0 0 0	I_0

Enable is active low, when $E = 1$, the output is logic 1
When $E = 0$, output is from multiplexer. Choice (B)

24. By observing sequence
$0000 \rightarrow 1000 \rightarrow 1100 \rightarrow 1110 \rightarrow 1111 \rightarrow 0111 \rightarrow 0011 \rightarrow 0001 \rightarrow 0000$
It is twisted ring counter. Choice (D)

25. The frequency of $Q_o = \dfrac{fclk}{2}$

Frequency of $Q_1 = \dfrac{\frac{fclk}{2}}{2} = \dfrac{fclk}{4}$

Frequency of $Q_2 = \dfrac{\frac{fclk}{4}}{2} = \dfrac{fclk}{8}$

Frequency of $Q_3 = \dfrac{fclk}{16}$

Frequency of $Q_4 = \dfrac{fclk}{32} = \dfrac{128}{32} = 4\,\text{kHz}$

Frequency of $Q_5 = \dfrac{fclk}{64}$ Choice (D)