COMPUTER ORGANIZATION AND ARCHITECTURE TEST 1

Number of Questions: 25 **Section Marks: 30**

Directions for questions 1 to 25: Select the correct alternative from the given choices.

1. On which of the following factors does the CPU execution time of a program depends?
(i) CPU clock cycles required for a program.
(ii) Clock cycle time.
(A) (i) only (B) (ii) only
(C) Both (i) and (ii) (D) Neither (i) nor (iii)

2. Which of the following component(*s*) is not related to the performance of a computer?
(i) CPU execution time for a program
(ii) Instruction count
(iii) Clock cycles per instruction
(iv) Clock cycle time
(A) (ii) only (B) (iii) and (iv)
(C) (i), (iv) (D) None of these

3. Which of the following metrics will be affected by the Instruction set Architecture?
(A) Instruction count (B) Clock rate
(C) CPI (D) All of the above

4. Which of the following combination illustrates the basic design principles of the Hardware design of a computer?
(i) Simplicity favours regularity
(ii) Smaller is faster
(iii) Make the common case fast
(iv) Good design demands good compromises
(A) (i), (iii) (B) (ii), (iv)
(C) (i), (ii), (iv) (D) (i), (ii), (iii), (iv)

5. To convert a 16 - bit number to a 32 - bit equivalent, take the MSB of the number and replicate it to fill the new bits of the 32 - bit number. The old bits are copied into the right portion of the new word. This is known as
(A) Sign expansion
(B) Sign extension
(C) Size casting
(D) Conversion from 16 bit number to 32 bit number is not possible

6. A number in scientific notation that has no leading zeros is called a ——— number.
(A) Floating point (B) Normalized
(C) Overflow (D) De-normalized

7. Consider a 5 - stage pipeline :
1. Instruction fetch 2. Register Read
3. ALU operation 4. Data Access
5. Register write

The time taken for memory access is 200 ns, CPU operation is 200 ns, register read or write is 100 ns. Consider a program with the following kind of instructions:
I_1: Load word
I_2: Store word
I_3: ALU operation
I_4: BEQ (Branch if equal)
If each instruction takes exactly one clock cycle, under ideal conditions, what is the time between I_1 and I_4 with out pipelining?
(A) 800 ns (B) 2100 ns
(C) 2400 ns (D) 600 ns

8. For the previous problem, what is the time between I_1 and I_4 using pipelining?
(A) 2100 ns (B) 2400 ns
(C) 800 ns (D) 600 ns

9. The speed up of pipelined processor compared to non pipelined processor is
——— the number of pipeline stages.
(A) always equal to (B) always less than
(C) less than (D) greater than

10. Pipelining improves the performance by
(A) increasing instruction throughput.
(B) decreasing the execution time of an individual instruction.
(C) Both (A) and (B)
(D) replacing complex instructions with simple instructions.

11. Assume that an enhancement is made to a computer that improves some mode of execution by a factor of 10. This new fast mode is used 50% of the time, measured as a percentage of the execution time when the fast mode is in use. What is the over all speed up we can achieve?
(A) 5.5 (B) 5.2
(C) 4.8 (D) 5.0

12. A bus protocol requires 20 ns for devices to make requests, 10 ns for arbitration and 30 ns to complete each operation. How many operations can be completed per second?
(A) $10 * 10^6$ (B) $17 * 10^6$
(C) $20 * 10^6$ (D) $33 * 10^6$

13. A process has five interrupt lines, numbered 0 – 4 and a policy that low numbered interrupts have priority over higher numbered ones. The processor starts with no interrupts pending and the following sequence of interrupts occurs: 4, 3, 0, 1, 2, 3
Assume that handling any interrupt takes enough time that two more interrupts arrive while the first interrupt is being handled, until all of the interrupts have arrived and that interrupts cannot interrupt each other.
In what order the interrupts are handled ?
(A) 0, 1,2, 3, 3, 4 (B) 4, 3, 0, 1, 2, 3
(C) 4, 0, 1, 3, 2, 3 (D) 4, 0, 1, 2, 3, 3

14. Which of the following mapping technique will provide simpler hardware, simple instruction set and provides all addressing modes?
(i) Memory mapped I/O
(ii) Isolated I/O
(A) (i) only (B) (ii) only
(C) Both (i) and (ii) (D) Neither (i) nor (ii)

15. Which of the following factors limits the maximum transfer rate of DMA?
(A) Speed of I/O devices
(B) Erroneous transfer of block
(C) Speed of bus
(D) All the above

16. An address field in an instruction contains decimal value 10. Where is the corresponding operand located for direct addressing?
(A) In the location '10'.
(B) '10' is the operand itself.
(C) '*PC*+ 10' location.
(D) Data insufficient

17. Suppose we had a block transfer from an I/O device to memory. The block consists of 1024 words and one word can be transferred to/from memory at a time. The number of interrupts needed to transfer a block using DMA is _____.
(A) 0 (B) 1
(C) 1024 (D) Unpredictable

18. For the above problem, what is the number of interrupts needed to transfer a block using interrupt driven I/O?
(A) 0 (B) 1
(C) 1024 (D) Unpredictable

19. For the Q.no :17, what is the number of interrupts needed to transfer a block using 'programmed I/O'?
(A) 0 (B) 1
(C) 1024 (D) Unpredictable

20. The number of times does the processor need to refer to memory when it fetches and executes an indirect address mode instruction (if the instruction is not a branch instruction) is:
(A) 0 (B) 1
(C) 2 (D) 3

21. Which of the following is a valid difference between a program branch instruction and a subroutine call?
(i) A branch instruction changes the contents of PC.
(ii) A branch instruction do not save the contents of PC before changing, Where as a subroutine will save PC.
(A) (i) only (B) (ii) only
(C) Both (i) and (ii) (D) Neither (i) nor (ii)

22. If there are no push and pop operations in an instruction set, then which of the following is TRUE?
(A) CPU can't able to use the stack.
(B) CPU can use the stack to perform its internal functions.
(C) The programmer can use the stack explicitly.
(D) None of the above

23. Match the following:

Addressing mode		Basic advantage	
1.	Immediate	a.	No memory reference
2.	Direct	b.	Simple
3.	Indirect	c.	Large address space
4.	Register	d.	Flexibility

(A) 1 – b, 2 – a, 3 – c, 4 – a
(B) 1 – a, 2 – a, 3 – d, 4 – b
(C) 1 – a, 2 – b, 3 – c, 4 – a
(D) 1 – a, 2 – b, 3 – d, 4 – c

24. What is the 8 - bit biased notation representation for –45?
(A) 01010010 (B) 10101101
(C) 11010011 (D) 11010010

25. Which of the following are the disadvantages of device polling?
(i) Polling consumes execution resources even when there are no I/O requests to handle.
(ii) There is a need to schedule the polling frequency.
(A) (i) only (B) (ii) only
(C) Both (i) and (ii) (D) Neither (i) nor (ii)

Answer Keys

1. C	**2.** D	**3.** D	**4.** D	**5.** B	**6.** B	**7.** C	**8.** D	**9.** C	**10.** A
11. A	**12.** B	**13.** D	**14.** A	**15.** D	**16.** A	**17.** B	**18.** C	**19.** A	**20.** D
21. C	**22.** B	**23.** C	**24.** A	**25.** C					

Hints and Explanations

1. CPU execution time for a program = CPU clock cycles for a program * clock cycle time. Choice (C)

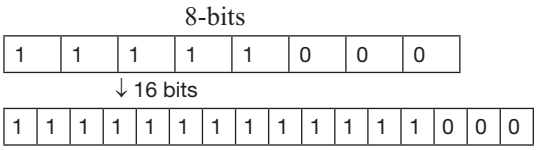
2. All the four are the basic measurements at different levels in the computer. Choice (D)

3. The instruction set architecture affects all the three aspects of CPU performance; it affects the instructions needed for a function, the cost in cycles of each instruction and the overall clock rate of the processor.
Choice (D)

4. The design principles of Hardware of a computer are
1. Simplicity
2. Smaller number of registers
3. Commonly occurring things needs to be constant.
4. Some compromises required for good design

Choice (D)

5.



Choice (B)

7. Without using pipelining the time taken for a single instruction is the sum of the times required by all the stages of the pipeline.
i.e., $IF + RR + ALU + DA + RW$
= 200 + 100 + 200 + 200 + 100 = 800ns
Each instruction requires one clock cycle.
Time between I_4 and I_1 is 800 ns * 3(instructions)
= 2400 ns. Choice (C)

8. Using pipelining I_2 will start IF after completion of I_1's IF.
So the maximum stage delay 200 ns is considered as time between I_1 and I_2.
(i.e., any two instructions)
Time between I_1 and I_4 is 3 × 200 ns = 600 ns.
Choice (D)

9. The speed up of pipelined processor is equal to number of pipeline stages under ideal conditions. But in general, it will be less than the number of stages.
Choice (C)

10. Pipelining improves performance by increasing instruction throughout rather than decreasing the execution time of an individual instruction. Choice (A)

11. Speed of after enhancement
= 0.5 * 10 + (1 – 0.5)
= 5 + 0.5 = 5.5. Choice (A)

12. Time taken for an operation= 20 ns + 10 ns + 30 ns = 60 ns. Number of operations completed per second

$$= \frac{1}{60\times10^{-9}}$$

$= 17 * 10^6$ operations/sec Choice (B)

13. Lower numbered interrupts have high priority.
Let initially 4 is handled, mean while, 3 and 0 will occur. Give priority to 0.
While 0 is handled, 1 and 2 will occur with 3 also in pending Queue. Next handle 1, 2, 3, 3.
∴ Order is 4, 0, 1, 2, 3, 3. Choice (D)

14. Memory mapped I/O provides
- Simple hardware
- Simple instruction set
- All address modes available. Choice (A)

15. DMA does not use CPU but its transfer rate is limited because of
1. low speed of I/O devices
2. low speed of bus
3. less internal buffering
4. erroneous Disk. Choice (D)

16. In direct addressing mode, the address of operand is directly present in the instruction itself. So location 10 contains the data. Choice (A)

17. DMA will generate an interrupt after completion of block transfer.
∴ One interrupt will be generated. Choice (B)

18. In interrupt driven technique, interrupt will be generated after transfer of every word.
∴ 1024 interrupts. Choice (C)

19. In programmed I/O, no interrupt will be generated.
The CPU will check the status bits.
∴ Zero interrupts. Choice (A)

20 '3' memory references required.
one for fetching instruction and '2' for fetching operand. Choice (D)

21. A branch instruction do not save PC before changing PC, where as a subroutine saves for restoring them later. Choice (C)

22. CPU can use stack even if there are no PUSH and POP instructions. PUSH and POP are used by the programmer. Choice (B)

23. Immediate, Register – No memory reference
Direct – simple.
Indirect – large address space. Choice (C)

24. The bias using 8-bits is 127.
Biased value of –45 is
–45 + 127 = 82 = 01010010. Choice (A)

25. Polling wastes the resources and the frequency of polling also need to be scheduled. Choice (C)