Chapter 12

Microprocessor 8085

LEARNING OBJECTIVES

After reading this chapter, you will be able to understand:

- Organization of microprocessor based system
- Microprocessor 8085
- Instructions classifications
- Instruction word size
- Operations in micro-processor
- 8085 signals
- Peripheral – mapped I/O
- Memory mapped I/O
- Additional instructions
- Stack
- Subroutine
- Restart (RST) instructions

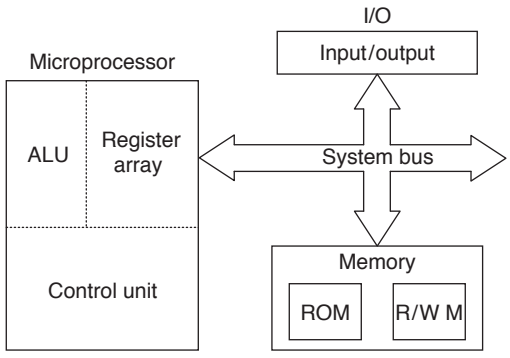
Introduction

The microprocessor is a programmable integrated device that has computing and decision-making capability similar to that of the central processing unit (CPU) of computer.

The microprocessor communicates and operates in the binary numbers 0 and 1 called bits.

Each microprocessor has a fixed set of instruction in the form of binary patterns called machine language to make it easier to understand the binary instructions that are given abbreviated names, called mnemonics, which form the assembly language for a given microprocessor.

Organization of Microprocessor-Based System



Microprocessor-based systems include three components: microprocessor, input/output (I/O) and memory

These components are organized around a common communication path called bus.

Microprocessor

The microprocessor is a clock driven semiconductor device consisting of electric logic circuits manufactured by using either LSI, or VLSI technique.

Arithmetic Logic Unit

The ALU unit performs arithmetic operations as addition, subtraction, and logic operations like AND, OR, exclusive OR.

Register Array

Microprocessor consists of various registers identified by *B*, *C*, *D*, *E*, *H* and *L*. These registers are primarily used to store data temporarily during the execution of a program.

Control Unit

The control unit provides the necessary timing and control signals to all the operations in the microcomputer.

Microprocessor 8085

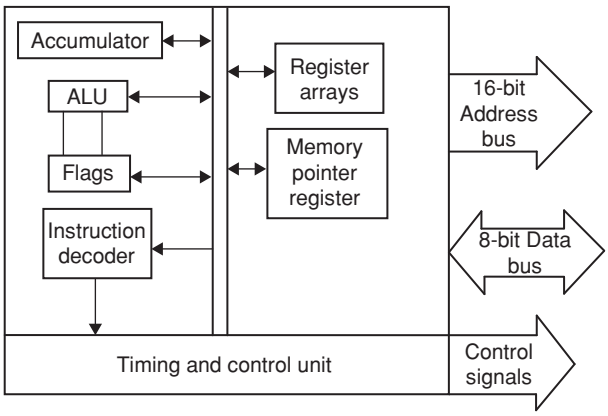


Figure 1 8085 Hardware model

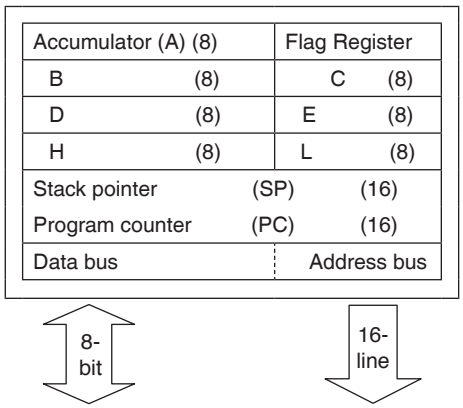


Figure 2 8085 Programming model

Table 1 *Flag register*

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	*Z*		*AC*		*P*		*CY*

Registers

The 8085 has six general purpose registers to store 8-bit data. These are identified as *B*, *C*, *D*, *E*, *H* and *L*, They can be combined as register pairs *BC*, *DE*, and *HL* to perform some 16-bit operations.

Accumulator

It is an 8-bit register, part of ALU. The result of an operation is stored in the accumulator. It is also identified as register *A*.

Flags

The ALU includes five flip-flops these flags are set or reset after the execution of an arithmetic or logic operation.

Z—Zero flag is set to 1 when result is zero, otherwise it is reset

CY—Carry flag—if an arithmetic operation results in carry or borrow, the carry flag is set, otherwise reset

S—Sign flag is set if bit D_7 (MSB) of the result = 1, otherwise reset

P—Parity flag is set, if result has an even number of 1's, for odd number of 1's the flag is reset

AC—Auxiliary carry flag is set, when (in arithmetic operation) a carry is generated by digit D_3 and passed to D_4 (carry transition from lower nibble to higher nibble). This flag is used internally for BCD operations.

Program Counter (PC) and Stack Pointer (SP)

These are two 16-bit registers used to hold memory addresses.

The function of program counter is to point to memory address from which the next byte is to be fetched and executed

When a byte (machine code) is being fetched, the program counter is incremented by one to point to the next memory location

Stack pointer points to a memory location in R/W memory, called stack. The beginning of the stack is defined by loading a 16-bit adder in the stack pointer.

Instructions Classifications

An instruction is a binary pattern designed inside a microprocessor to perform a specific function. The entire group of instructions, called instructions set, determines what functions the microprocessor can perform.

Data Transfer (Copy) Operations

These instructions perform the following six operations

Load an 8-number in a register

Load 16-bit number in a register pair

Copy from register to register

Copy between register and memory

Copy between I/O and Accumulator

Copy between registers and stack memory

Mnemonics	Operations
MVI reg., 8-bit	Load 8-bit data in a register
MOV Rd, Rs	Copy data from source (Rs) to destination (Rd) register
LXI Rp, 16-bit	Load 16-bit Num in a register pair(Rp)
OUT 8-bit (port addr)	Send data byte from accumulator
IN 8-bit (port Addr)	Accept data byte from input device into accumulator
LDA 16-bit	Load accumulator with data from 16-bit memory address
STA 16-bit	Store contents of A in 16-bit memory address
LDAX Rp	Load 'A' with data from memory address specified by (Rp) register pair
STAX Rp	Store data in A into the memory location specified by (Rp)
MOV R, M	Copy the data byte into register (R) from the memory specified by the address by HL pair
MOV M, R	Copy data byte into memory specified by HL pair from the register (R)

Arithmetic Instructions

The frequently used arithmetic operations are add, subtract, increment, decrement, the result will be stored in accumulator.

Mnemonics	Operation
ADD R	Add contents of reg. to contents of A
ADI 8-bit	Add 8-bit data to contents of A
ADD M	Add the contents of memory (in HL reg.) to A
SUB R	Subtract the contents of reg. from contents of A
SUI 8-bit	Subtract 8-bit data from contents of A
SUB M	Subtract the contents of memory HL from A
INR R/M	Increment reg./contents in memory (specified in HL) by 1
DCR R/M	Decrement reg./contents in memory (specified in HL) by 1
INX Rp	Increment the contents of register pair by 1
DCX Rp	Decrement the contents of register pair by 1

Logic and Bit Manipulation Instructions

These instructions include the following operations AND, OR, EX-OR, compare rotate bits, result will be stored in accumulator.

Mnemonic	Operations
ANA R/M	Logically AND the contents of reg./memory with contents of A
ANI 8-bit	Logically AND 8-bit data with A
ORA R/M	Logically OR the contents of reg./memory with contents of A
ORI 8-bit	Logically OR 8-bit data with A
XRA R/M	Ex-OR, the contents of a register/memory with A
XRI 8-bit	Ex-OR the contents of 8-bit data with A
CMP R	Compare the contents of R with A
CPI 8-bit	Compare 8-bit data with A
CMA	Complement accumulator

Branch Instructions

The following instructions change the program sequence

Mnemonics	Operation
JMP 16-bit address	Unconditional change the program sequence to specified address
JZ 16-bit address	Change the program sequence to specific address if zero flag is set
JNZ 16-bit address	If zero flag is reset change program sequence
JC 16-bit address	If carry flag is set change the program sequence
JNC 16-bit address	Change program sequence if carry flag is reset
CALL 16-bit address	Change the program sequence to the location of a subroutine specified
RET	Return to the called program after subroutine sequence

Machine Control Instructions

These instructions affect the operation of the processer

HLT—Stop processing and wait

NOP—Do not perform any operation

In data transfer, the contents of the source are not destroyed. Only the contents of the destination are changed. The data copy instructions do not affect the flags.

Arithmetic and logical operations are performed with the contents of accumulator and results are stored in the accumulator

Instruction word size

1-byte instructions These include OP code and operand in the same byte, each instructions, requires 1-byte memory space

Example: MOV C, A; ADD B; CMA
Mnemonic followed by letters representing register or memory.

2-byte instructions The first byte specifies the operation code and the second byte specifies operand. A mnemonic followed by 8-bit

Example: MVI A, 32H; MVI B, F2H;
These instructions would require two memory locations

3-byte instructions These instructions would require three memory locations, each to store the binary codes. The first byte specifies the op code, and the following two bytes specify the 16-bit address, the second byte is the low order address and third byte is the higher order address

These instructions have mnemonic followed by 16-bit
Example:

LDA 2050 H	3A first byte (op code) 50 second byte 20 third byte
JMP 2085 H	C3 first byte (op code) 85 second byte 20 third byte

An instructions has two parts, OP code (operation to be performed) and operand (data to be operated on)

The operand can be data (8 or 16-bit), address or register or it can be implicit.

The method of specifying an operand (directly or indirectly etc) is called the addressing mode.

Operations in Micro-processor

The microprocessor (MPU) primarily performs four operations

1. memory read
2. memory write
3. I/O read
4. I/O write

For each operations, it generates the appropriate control signals. To communicate with a peripheral (and memory) the MPU identifies the location by its address, transfers data, and provides timing signals.

The 8085 microprocessor has 16 address lines, 8-data lines, and control bus to provide timing of various operations. The 8085 can respond to four externally initiated operations: reset, interrupt, ready and hold.

Memory is a group of registers arranged in a sequence to store bits: The 8085 MPU requires an 8-bit wide memory word and uses 16-bit address to select a memory location. The memory addressing assigned to a memory chip in a system is called the memory mapping.

The assignment of memory address is done through the chip select logic.

Memory can be classified into two groups.

1. Read/write memory is volatile and can be used to read and write information this is also called user memory
2. The ROM is a non volatile memory and the information written into this memory is permanent

Input/output devices or peripherals can be interfaced with 8085 in two days. Peripheral I/O and memory mapped I/O.

In peripheral I/O, the MPU uses an 8-bit address to identify an I/O, and IN and OUT instructions for data transfer. In memory mapped I/O, the MPU uses a 16-bit address to identify an I/O, and memory related instructions for data transfer.

To execute an instruction, the MPU places the 16-bit address on the address bus, sends the control signal to enable the memory chip and fetches the instruction. The instruction is then decoded and executed.

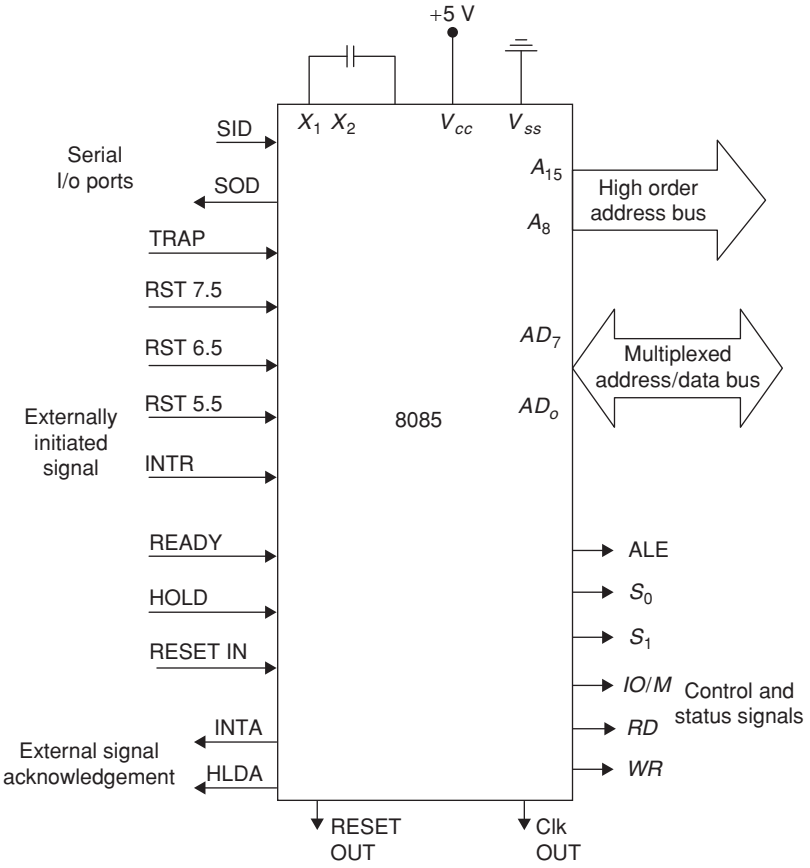


Figure 3 The 8085 microprocessor signals

8085 Signals

8085 is an 8-bit general purpose microprocessor.

Addressing capacity: 64 k bytes

It is an integrated circuit with 40 pins and uses a +5 V power supply, operates at 3 MHz single phase clock. (8085 A-2 version can operate at the maximum frequency of 5 MHz)

The signals of 8085 microprocessor are classified into 6 groups.

1. Address bus: The 8085 has 16 lines ($A_{15} - A_8$) and ($AD_7 - AD_0$) as address bus. Higher order address lines are unidirectional, lower order address lines ($AD_7 - AD_0$) are used for data and lower order address bus.
2. Data bus: The signal lines ($AD_7 - AD_o$) are bi-directional. In executing an instruction, during earlier part of the cycle, these lines are used as the lower address bus. During later part of the cycle, these lines are used as data bus.
3. Control and status signals:
   ALE: Address latch enable: It is active high signal generated every time the 8085 begin an operation.

(Machine Cycle): It indicates the bits $AD_7 - AD_0$ are address bits.

$\overline{RD}$ -Read: This active low signal indicates the selected IO/memory device to be read, and data are available on data bus.

$\overline{WR}$ -write: This active low signal indicates the data available on data bus are to be written into a selected memory or I/O.

$IO/\overline{M}$ This signal used to indicate IO(1) or memory(0) operation.

S_1 and S_0: These status signals can identify various operations as per the table below.

Machine Cycle	$IO/\overline{M}$	S_1	S_0	Control Signals
op code fetch	0	1	1	$\overline{RD} = 0$
Memory read	0	1	0	$\overline{RD} = 0$
Memory write	0	0	1	$\overline{WR} = 0$
I/O read	1	1	0	$\overline{RD} = 0$
I/O Write	1	0	1	$\overline{WR} = 0$
Interrupt acknowledge	1	1	1	$\overline{\text{INTA}} = 0$
Halt	Z	0	0	$\overline{RD}, \overline{WR} = z, \overline{\text{INTA}} = 1$
Hold	Z	X	X	$\overline{RD}, \overline{WR} = Z$
Reset	Z	X	X	$\overline{\text{INTA}} = 1$

4. Power supply and clk frequency
   V_{CC}: +5 V power supply, V_{SS}: Ground X_1, X_2: A crystal (RL or RC) is connected between these two pins; the frequency is internally divided by two.
   Clk (out): This is system clock for other devices.
5. Externally initiated signals:
   INTR (input): general purpose interrupt request.
   $\overline{\text{INTA}}$ (output): Interrupt Acknowledgement
   RST 7.5: } Restart interrupts, vectored interrupts,
   RST 6.5: } That transfer the program control to
   RST 5.5: } Specific memory location (8x)
   TRAP (input): non maskable interrupt with highest priority.
   HOLD (input): This signal indicates that a peripheral such as DMA is requesting the use of address/data bus.
   HLDA (output): Hold request acknowledgement.
   READY (input): When this signal goes low, microprocessor waits for an integral number of clock cycles until it goes high.
   $\overline{\text{RESETN}}$: When the signals goes low, PC is set to zero, the buses are tri-stated and microprocessor is reset.
   RESET OUT: This signal indicates, MPU is being rest and used to rest other devices.
6. Serial IO ports:
   SID—serial input data,
   SOD—serial output data.

The 8085 microprocessor has a multiplexed bus $AD_7 - AD_0$ used as lower order address bus and the data bus.

The bus $AD_7 - AD_0$ can be demultiplexed by using a latch and the ALE signal

The 8085 has a status signal $IO/\overline{M}$ and two control signals $\overline{RD}, \overline{WR}$, by ANDing these signals, four control signals can be generated $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{IOR}}$, $\overline{\text{IOW}}$,

To execute an instruction the MPU

- Places the memory address of instruction on address bus
- Indicates the operation status on the status lines
- Sends $\overline{\text{MEMR}}$ control signal to enable the memory, fetches the instruction byte, and places it in the instruction decoder.
- Executes the instruction.
- Each instruction of 8085 microprocessor can be divided into a few basic operations called machine cycles, and each machine cycle can be divided into T-states.

The frequently used machine cycles are Opcode fetch, memory read and write, and I/O read and write.

When 8085 performs any of the operations, it asserts the appropriate control signal and status signal.

The opcode fetch and the memory read are operationally similar, the 8085 reads from memory in both machine cycles. However, the 8085 reads opcode during the opcode fetch cycle, and it reads 8-bit data during the memory read cycle. In the memory write cycle, the processer writes data into memory.

The 8085 performs there basic steps in any of these machine cycles, it places the address on address bus. Sends appropriate control signals, and transfers data via data bus.

8085 Machine Cycles and Bus Timings

1. Instruction cycle: It is the time required to complete the execution of an instruction, one instruction cycle consists of 1 to 6 machine cycles.
2. Machine cycle: It is the time required to complete one operation like accessing memory or IO or acknowledging external request. This cycle may consist of 3 to 6 T-states.
3. T-states: It is the part of the operation performed in one clock period. Each T-state is exactly equal to one clock period.

In each instruction cycle, the first operation is always opcode fetch, this cycle can be of four to six T-states duration.

Memory read is similar to opcode fetch but requires 3 T-states, and these two differentiated by the status signals.

Memory write cycle consists of 3 – T-states.

I/O read or I/O write consists of 3 – T-states.

Interrupt acknowledgement machine cycle consists of 6 T-states.

Consider instruction STA 2016 H, → store accumulator contents in memory location 2016 H.

This instruction includes → opcode fetch and memory read machine cycles to read address 2016 H, and then memory write machine cycle. Total of 4 machine cycles, and it is a 3-byte instruction.

Total T-states are = opcode fetch + memory read + memory read + memory write = 4 + 3 + 3 + 3 = 13 T-states.

Consider another instruct OUT 20 H, → transfer the data from accumulator to output device at 20 H.

This instruction consists of op code fetch, +memory read (reading 20 H) + I/O write.

Total T-states are = 4 + 3 + 3 = 10 T-states

Consider CALL 2006 H instruction, This instruction is a 3 byte instruction, which takes the program control to the address specified 2006 H and it stores the address of next instruction on the top of stack, so that RET instruction can take execution to previous program.

So call instruction consists of 5 machine cycles. Opcode fetch + memory read + memory read + memory write + memory write (storing program counter) = 4 + 3 + 3 + 3 + 3 = 18 T-states

To interface a memory chip with 8085, the necessary low order address lines of the 8085 address bus are connected to the address lines of the memory chip.

The high order address lines are decoded to generate $\overline{CS}$ signals to enable the chip.

In the absolute decoding technique, all the address lines that are not used for the memory chip to identify a memory register must be decoded, thus the chip select can be asserted by only one address. In the particular decoding technique, same address lines are left don't care. This technique reduces hardware, but generates multiple address resulting in fold back memory space.

Peripheral-mapped I/O

A latch is commonly used to interface output devices. A tri-state buffer is commonly used to interface input devices. To interface an output or an input device, the low order address bus $A_7 - A_0$ (or high order bus) needs to be coded to generate the device address plus, which must be combined with the control signal $\overline{IOR}$ or $\overline{IOW}$ to select the device.

Memory Mapped I/O

Memory related instructions are used to transfer data, to interface I/O device, the entire bus must be decoded to generate the device address pulse, which must be combined with the control signal $\overline{MEMR}$ or $\overline{MEMW}$ to generate the I/O select pulse. This pulse is used to enable the I/O device and transfer the data.

Memory interfacing

The primary function of memory interfacing is that the microprocessor should able to read and write into a given register of a memory element. To perform read/write operation with memory, the microprocessor should.

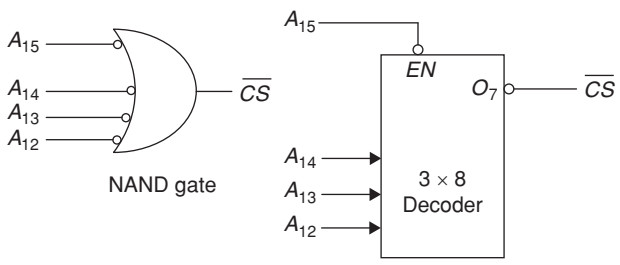
1. be able to select the chip (through $\overline{CS}$)
2. identify the register (using address bus)
3. enable read/write operation (using $\overline{RD}$ or $\overline{WR}$ signals)

Address decoding and memory addresses The process of address decoding should result in identifying a register for a given address. We should able to generate a unique pulse for a given address.

Let us consider 4k × 8 R/W memory has to interface with 8085 microprocessor.

Microprocessor uses 16-bit address, but $4k \times 8 = 2^{12} \times 8$ memory uses 12-bit address ($A_{11} - A_0$).

To interface with microprocessor, lower order address $A_{11} - A_0$ are connected to memory chip and remaining four address lines ($A_{15} - A_{12}$) of 8085 microprocessor must be decoded, this can be done by a gate/decoder/demultiplexer.

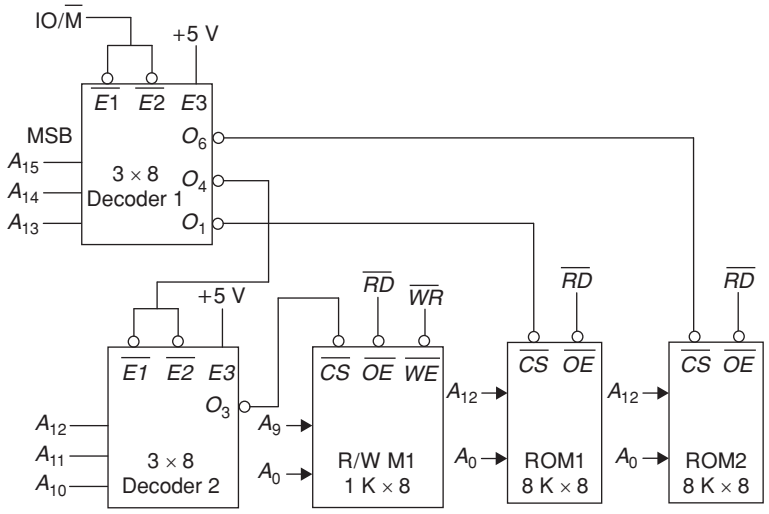


We can obtain the address range of this memory chip 4k × 8 by analyzing the possible logic levels on the 16 address lines.

As per the NAND gate, (or) decoder shown to select $\overline{CS}$, the address inputs $A_{15} - A_{12}$ should be 1111, and the address lines $A_{11} - A_0$ can assume any combinations from all 0 to all 1s. So memory address of this chip ranges from F000 H to FFFF H.

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	= F000H
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	= FFFFH
Chip select				Register select												

Example: Identify the address range of the memory chips ROM1, ROM2 and R/WM1? For the memory interfacing circuit with 8085 microprocessor shown in the next page.



Solution: ROM1, ROM2 are read only memories $\overline{OE}$ —output enable is connected to $\overline{RD}$ signal of microprocessor. The chip select of ROM1, ROM2 are given from 3 × 8 decoder 1 outputs O_2 and O_6.

The enable inputs $\overline{E1}, \overline{E2}$ are connected $IO/\overline{M}$ so only memory operations will enable the decoder 1.

The range of address for ROM1 (ROM1 is selected with O_1 of decoder, so $A_{15}\,A_{14}\,A_{13} = 001$)

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	= 2000 H
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	= 3FFFH

$A_{15} - A_{13}$ – used for chip select

$A_{12} - A_0$ – address inputs for ROM for all zero to all one

8k × 8 ROM = $2^{13} \times 8 \rightarrow$ 13 address lines $(A_{12} - A_0)$

ROM2 is selected with O_6 of decoder 1

So $A_{15}\,A_{14}\,A_{13} = 110$

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
																= C000H
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	= DFFFH

Read or write memory 1 of size 1 k × 8 = $2^{10} \times 8$ has 10 address lines $A_9 - A_0$, its chip select is connected from O_3 of decoder 2 with inputs $A_{12}\,A_{11}\,A_{10}$ (= 011)

Decoder 2 is enabled by decoder 1, O_4 output, so $A_{15}\,A_{14}\,A_{13} = 100$.

Output enable $(\overline{OE})$, write enable $(\overline{WE})$ are connected to microprocessor $\overline{RD}, \overline{WR}$ signals. So the range of address for the R/w memory is

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	
																= 800H
1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	= 8FFFH
Decoder 1			Decoder 2			Address llines of 1 k × 8										

Range of address for ROM1 = 2000H – 3FFFH

Range of address for ROM2 = C000H – DFFFH

Range of address for R/w M1 = 8C00H – 8FFFH

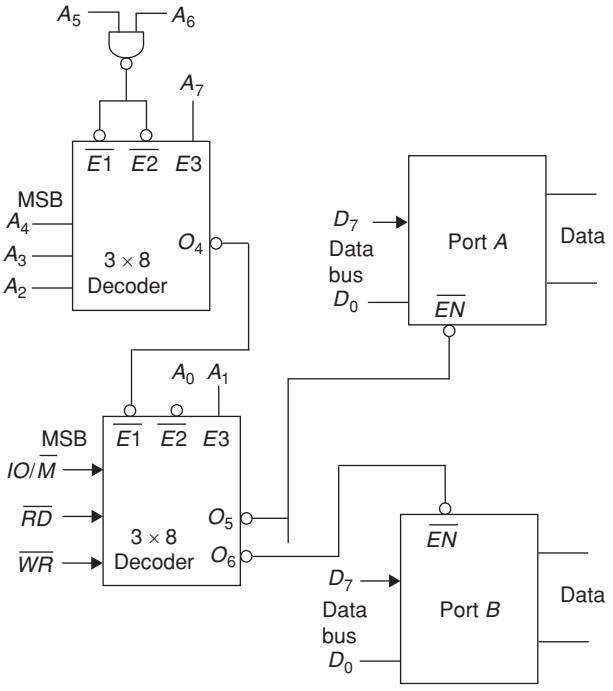
Peripheral I/O instructions The I/O devices such as key boards, and displays can be interfaced with 8085 microprocessor with 8-bit addresses in peripheral mapped I/O. In memory mapped I/O, 16-bit address will be used and memory related instructions for peripheral mapped I/O 8-bit address will be used.

- IN 8-bit port adder → This is 2-byte instruction, which transfers the data from input port to accumulator.
- OUT 8-bit port adder → This is a 2-byte instruction which transfers the data from accumulator to output port.

When an I/O instruction is executed, the 8085 microprocessor places the device address (port number) on the demultiplexed lower order as well as higher order address bus.

Address can be decoded to generate the pulse corresponding to the device address on the bus, and it will be added with appropriate signal IOR or IOW, and when both signals asserted, the I/O port is selected.

Example: In the following I/O interfacing circuit identify ports A and B as input or output ports and addresses of the ports? And find the instruction to be used?



Solutions: Two ports port A, and port B are connected in the above figure with two decoders.

First decoder O_4 is used to enable $(\overline{E1})$ of second decoder, so $A_4 A_3 A_2 = 100$.

First decoder will be enabled if $\overline{E1}\overline{E2}E3 = 001$, so $A_5 A_6$ = 11 (NAND output = 0), $A_7 = 1$

Second decoder will be enabled $\overline{E2}\,E3 = 01$

So $A_1 = 1, A_0 = 0$

The address of the port is

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	1	1	1	0	0	1	0	= F2H

So both port A, and port B will have same address F2H,

But if we select IO Read operation

$IO/\overline{M} = 1, \overline{RD} = 0, \overline{WR} = 1$, inputs for second decoder. So O_5 will be selected, port A is used for IO read operation IN F2 H is the instruction for port A. (input)

For IO write operation

$IO/\overline{M} = 1, \overline{RD} = 1, \overline{WR} = 0$, 110 input for decoder will select O_6 output, so port B will be enabled for write operation.

OUT F2 H is the instruction for output port B.

Table 2 *Comparison between Memory Mapped I/O and Peripheral I/O*

	Memory Mapped I/O		Peripheral I/O
1	device address is 16-bit.	1	device address is 8-bit.
2	$\overline{\text{MEMR}}/\overline{\text{MEMR}}$ control signals for input/output.	2	$\overline{\text{IOR}}/\overline{\text{IOW}}$ control singles for input/output.
3	The memory map (64 k) is shared between IOs and system memory.	3	I/O map is independent of the memory map, 256 input devices and 256 output devices can be connected.
4	More hardware needed to decode 16-bit memory address but arithmetic/logical operations can be performed.	4	Less hardware needed to decode 8-bit address, Arithmetic and logical operations not available.

Additional Instructions

Table 3 *Additional Jump Instructions*

JP 16-bit	Jump on Plus (if $D_7 = 0$ and $S = 0$)
JM 16-bit	jump on minus (if $D_7 = 1$ and $S = 1$)
JPE 16-bit	jump on even party ($p = 1$)
JPO 16-bit	jump on odd party ($p = 0$)

Table 4 *Additional Data Transfer and 16-bit Arithmetic Instructions*

LXI, Rp, 16-bit	load reg. pair immediate
LDAX B/D	load accumulator indirect
LDA 16-bit	load accumulator direct
STAX B/D	store accumulator indirect
STA 16-bit	store accumulator direct
INX Rp,	increment register pair
DCX RP,	decrement register pair.

Table 5 *Logic Operation: Rotate*

RLC	Rotate accumulator left
RAL	Rotate accumulator left through carry
RRC	Rotate accumulator right
RAR	Rotate accumulator right through carry

Logic operations: Compare

CMP R/M: Compare register/memory with accumulator
CPI 8-bit: Compare immediate with accumulator

If $A <$ R/M $CY = 1, Z = 0$
If $A >$ R/M $CY = 0, Z = 0$
If $A =$ R/M $CY = 0, Z = 1$

Remaining flags effected according to the result of subtraction.

Table 6 16-*bit data transfer and data exchange instructions*

LHLD 16-bit	Load HL registers direct
SHLD 16-bit	Store HL registers direct
XCHG 16-bit	Exchange the contents of HL with DE
XTHL	Exchange the top of the stack with HL
SPHL	Copy HL reg. pair into stack pointer
PCHL	Copy HL reg. pair into the program counter
ADC R/M	Add reg./memory contents with carry to accumulator
SBB R/M	Subtract reg./memory contents with barrow from accumulator
DAA	Decimal adjust accumulator, it adjusts the 8-bit number in accumulator to form 2BCD numbers. It works with addition when BCD numbers are used
ACI 8-bit	Add immediate to accumulator with carry
CMC	Complement carry
DAD RP	Add register pair to HL registers
DI	Disable interrupts
EI	Enable interrupts
POP RP	POP off stack to reg. pair
PUSH Rp	Push reg. pair on to stack
SBI 8-bit	Subtract immediate with barrow
STC	Set carry
RIM	Read interrupt mask
SIM	Set interrupt mark
RST	Restart

Stack

Memory locations in R/W memory can be employed as temporary storage for information by initializing 16-bit address in the stack pointer (SP) register, these memory locations are called stack.

The stack space grows upward in the numerically decreasing order of memory address.

The contents of the stack pointer can be interpreted as the address of the memory location that is already used for storage. The retrieval of bytes begins at the address in the stack pointer; however the storage begins at the next memory location (in the decreasing order)

The storage and retrieval of data bytes on the stack should follow the LIFO (last in first out sequence) information in stack location is not destroyed until new information is stored in those location

PUSH Rp: Store register pair on stack: In copies the contents of the specified register pair on the stack. The stack pointer register is decremented and the contents of high order register (e.g., register B, D/H) are copied in the location shown by stack pointer register. The stack pointer register again decremented and the contents of the low order register (ex-register C/E/L) are copied in that location.

Operand PSW represents program status word, meaning the contents of the accumulator and the flags.

POP Rp: Retrieve register pair from stock: It copies the contents of the top two memory locations of stack into specified register pair.

First the contents of the memory location indicated by the stack pointer register are copied into the low order register (ex: register C/E/L) and then the stack pointer register incremented by 1. The contents of the next memory location are copied into the high order register (e.g., register H/B/D) and the stack pointer register is again incremented by 1.

Subroutine

It's a group of instructions written separately from the main program to perform a function that occurs repeatedly in the main program.

8085 has two instructions to implement subroutines. CALL 16-bit: call subroutine unconditionally. It transfer the program sequence to a subroutine address specified in instruction. First it saves the contents of the program counter (the address of next instruction) on the stack. Decrements the stack pointer by two, jumps unconditionally to the memory location specified by the second and third bytes in instruction. This instruction is accompanied by a return instruction in the subroutine.

RET: return from subroutine unconditionally. It inserts the two bytes from the top of the stack into the program counter and increments stack pointer by two. Unconditionally returns from a subroutine.

Conditional Call and Return Instructions

The conditional call and return instructions are based on four data conditions (flags) carry, zero, sign, parity.

If the call instruction in the main program is conditional the return instruction in the subroutine can be conditional or unconditional.

CC 16-bit: call subroutine if carry flag is set ($CY = 1$)

CNC 16-bit: call subroutine if carry flag is reset ($CY = 0$)

CZ 16-bit: call subroutine if zero flag is set ($z = 1$)

CNZ 16-bit: call subroutine if zero flag is reset ($z = 0$)

CM 16-bit: call subroutine if sign flag is set ($S = 1$ negative number)

CP 16-bit: call subroutine if sign flag is reset ($S = 0$ positive number)

CPE 16-bit: call subroutine if parity flag is set ($p = 1$ even parity)

CPO 16-bit: call subroutine if parity flag is reset ($p = 0$, odd parity)

Conditional RETURN

RC – return if $CY = 1$
RNC – return if $CY = 0$
RZ – return if $Z = 1$,
RNZ – return if $Z = 0$,
RM – return if S = 1
RP – return if $S = 0$
RPE – return if $P = 1$
RPO – return if $P = 0$

The programming technique of a subroutine calling another subroutine is called nesting; this process is limited only by the number of available stack locations. When a subroutine calls another subroutine, all return addresses are stored on the stack. One call can have multiple return instructions.

Restart (RST) Instructions

RST instructions are 1-byte call instructions that transfer the program execution to a specific location, on page 00 H.

RST 0 – call 0000 H
RST 1 – call 0008 H
RST 2 – call 0010 H
RST 3 – call 0018 H
RST 4 – call 0020 H
RST 5 – call 0028 H
RST 6 – call 0030 H
RST 7 – call 0038 H

The interrupt is an asynchronous process of communication with the microprocessor, initiated by an external peripheral.

The 8085 has a maskable interrupt that can be enabled or disabled using the instructions EI and DI.

The 8085 has four additional interrupt inputs, one non-maskable and three maskable, these three interrupts are implemented without any external hardware and are known as RST 7.5, 6.5, and 5.5.

The instruction SIM is necessary to implement the interrupt 7.5, 6.5, 5.5.

The instruction RIM can be used to check whether any interrupt requests are pending.

The direct memory access (DMA) is a process of high-speed data transfer under the control of external devices such as a DMA controller.

Table 7 *Summary of Interrupts in 8085 in the Order of Their Priority*

Interrupts	Type	Trigger
TRAP	Non-maskable – vectored (0024 H)	Level and edge sensitive
RST 7.5	Maskable vectored (003C H)	Edge-sensitive
RST 6.5	Maskable vectored (00034 H)	Level sensitive
RST 5.5	Maskable vectored (0002 CH)	Level sensitive
INTR	Maskable non-vectored (RST code from external hardware (0000-0038 H)	Level sensitive

Solved Examples

Example 1: Consider the following set of instructions:

LXI B, 7E45 H
STC
MOV A, B
ORA A
RAL
MOV B, A
This set of instructions

(A) Doubles the number in register B.
(B) Divides the number in register by 2.
(C) OR contents of B and A.
(D) Adds A and B register contents.

Solution: (A)

LXI B, 7E45 H—move 7E45 H to BC register pair, i.e., $B = 7EH$, $C = 45$ H.
STC—set carry, $CY = 1$
MOV A, B—Move contents of B to A.
ORA A—OR content of A with A itself, this makes $CY = 0$, and other flags will be effected as per result in A, and contents of A will not be altered as A OR $A = A$ only.
RAL—rotate accumulator left arithmetically, i.e., include carry bit in rotation, this instructions moves the contents of accumulator to shift left by 1-bit, and carry bit = (0) will be added at LSB side. This rotation is equal to multiplication by 2. Left shift by n-bit = multiplication by 2^n.
MOV B, A—move contents of A to B, i.e., store result in B again. Now the contents of B are doubled.

Common Data for Questions 2–4: Consider the following program of 8085 microprocessor and a subroutine at memory location 1010 H.

2020: LXI H, 2020 H
2023: SPHL
2024: MOV A, C
2025: XRA C
2026: RAL
2027: CZ 1010 H
202A: NOP

1010: PUSH B
1011: PUSH D
1012: POP B
1013: POP D
1014: XTHL
1015: RET

Example 2: What is the operation of subroutine at 1010 H?

(A) Interchanges contents of B and D registers
(B) Swaps the contents of SP and HL register pair

(C) Interchanges the contents of *B* and *D* register pairs.
(D) Copies the top of the stack to HL register pair.

Example 3: What are the contents of SP when the microprocessor is executing instruction at 1014 H?
(A) 201E H (B) 2020 H
(C) 1015 H (D) 202A H

Example 4: For how many number of times the instruction at 202AH will execute?
(A) Infinite times (B) 2
(C) 1 (D) Never executes

Solutions for questions 2 to 4:

2. (C) **3.** (A) **4**. (D)

2020: LXI H, 2020 H: Load HL register path with 2020 H, HL = 2020 H

2023: SPHL—Move HL register pair to SP stack pointer, SP = 2020 H

2024: MOV A, C—Move contents of register C to accumulator

2025: XRA C: XOR accumulator with C, now A = 00 H CY = 0, Z = 1.

2026: RAL—Rotate accumulator left through carry now CY = 0, A = 00 H

2027: CZ 1010 H-jump to 1010 if zero flag = 1, as Z = 1 now control execution go to 1010 H

But to come back to main program, CALL instruction stores the present PC = 202 AH on top of the stack, so now contents of top of stack are 202A, SP = 201E H and PC will be charged to 1010 H

1010: PUSH B—move contents of *BC* register pair on top of stack

1011: PUSH D—move contents of *DE* register pair on top of stack

1012: POP B—retrieve the top of stack contents to *BC* register pair i.e., *BC* = *DE*

1013: POP D—retrieve the top of stack contents to *DE* register pair i.e., *DE* = *BC*

These 4 instructions will interchange *B*, *D* register pairs, as stack works with last in first out principle, after these 4 instructions top of stack will have 202 AH and SP = 201E H

1014: XTHL—Exchange top of stack with HL register pair contents,

Now HL = 202AH, top of stack = 2020 H

1015:RET Return instruction returns to main program by taking the stored address of next instruction of CALL instruction on top of the stack i.e., by retrieving top of the stack to *PC*.

Now PC—2020 H. So the execution starts from 2020 H abs *CZ* will be always 1 and CALL(*CZ*) will be executed infinite number of times.

Example 5: Consider the following program for an 8085 microprocessor

```
    MVI A, 8-bit data
    ANA A
    JP SUB1
    XRA A
SUB1: OUT 8-bit port address
      HLT
```

At output port
(A) Only numbers with even number of 1's will appear
(B) Only numbers with odd number of 1's will appear
(C) No negative numbers will appear
(D) Only negative numbers will appear

Solution: (C)
MVI A, 8-bit data—Move 8-bit data to accumulator
ANA A—AND accumulator with accumulator itself.
JP SUB1—if sign flag is 0, i.e., for positive number, jump to SUB1, or else go to next instruction.
XRA A—XOR A with A i.e., contents of A − 00 H
SUB1: OUT 8-bit port address—output the accumulator contents to the 8-bit port address.

HLT—stop execution.

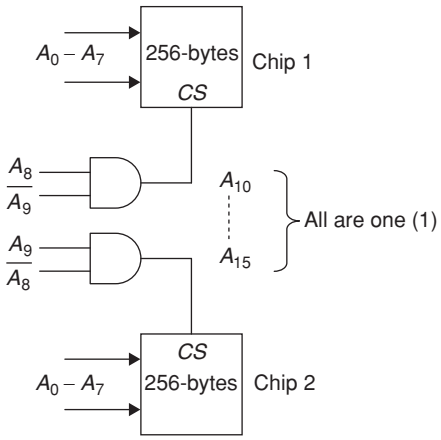
The program outputs only positive numbers. If the jump on positive condition fails then contents of accumulator will be reset, and 00 H will be the output at output port.

EXERCISES

Practice Problems I

Directions for questions 1 to 16: Select the correct alternative from the given choices.

1. Given two memories what is the memory address range represented by chip 1 or chip 2. (CS – chip select, $A_0 - A_{15}$ are address lines)



(A) 0100 – 02FF (B) F500 – F6FF
(C) F900 – FAFF (D) FD00 – FEFF

2. If we have an 8085 program as shown such that the program starts at location 0100 H, the content of accumulator when PC reaches 010C H is _____

LXI SP, 00 EF
LXI H, 0700
MOV A, M
XRA M
MOV M, A
MVI A, 30H
SUB M

(A) 30 H (B) 02 H
(C) 00 H (D) FF H

3. From the given program, what will be the content of SP on completion of RET execution?

LXI SP, EFFFH
CALL 2000 H
2000 H LXI H, 3CF4 H
PUSH PSW
SPHL
POP PSW
RET

(A) EFFD (B) EFFF
(C) 3CF6 (D) 3CF8

4. Given a 8085 program. Indicate the status of *CY* and *Z* flags after the execution of line 7 in the program.

Line 1: MVI A, B5 H
2: MVI B, 0EH
3: XRI 69 H
4: ADD B
5: ANI FBH
6: CPI 9F H
7: STA 3010 H
8: HLT

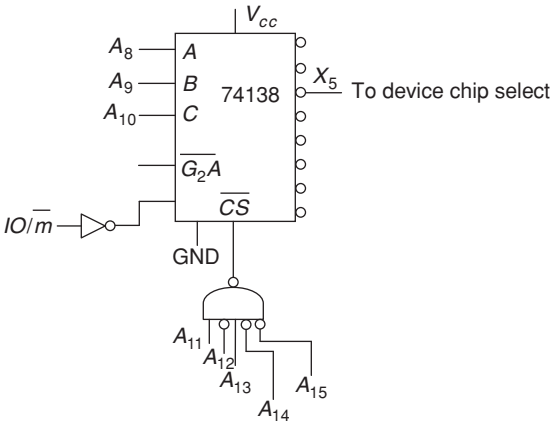
(A) $CY = 0, z = 0$ (B) $CY = 0, z = 1$
(C) $CY = 1, z = 0$ (D) $CY = 1, z = 1$

5. Predict the content of PC and HL after the execution of part of program.

2710 LXI H, 30A2H
2713 DAD H
2714 PCHL

(A) PC = 2715 H HL = 30 A2 H
(B) PC = 30 A2 H HL = 2715 H
(C) PC = 6144 H HL = 6144 H
(D) PC = 6144 H, HL = 2715 H

6. Determine the address range for the device connected to X_5.



(A) 2D00 – 2DFF (B) 2E00 – 2EFF
(C) FD00 – FDFF (D) 2F00 – 2FFF

7. For the program, find the content of accumulator after its complete execution

MVI A, 40 H
MOV B, A
STC
CMC
RAR
XRA B

(A) 60 H (B) 67 H
(C) 20 H (D) 40 H

8. Serial input data of 8085 can be loaded into bit-7 of accumulator by
(A) executing a RIM instruction
(B) using TRAP
(C) executing a RST 1
(D) None of these

9. Consider the program

```
    LXI D, 0009 H
    XRA A
LOOP: DCX D
    JNZ LOOP
```

The loop will be executed
(A) 9 times (B) 8 times
(C) 1 time (D) None of these

10. If we have an I/O port having address of 01 H what will be the content of flag register after the execution of instructions? (Assume data is 75 H)

```
IN  01 H
ANI 81 H
```

(A) 1 0 * 1 * 1 * 0
(B) 0 1 * 1 * 0 * 0
(C) 0 1 * 0 * 0 * 0
(D) 0 1 * 0 * 1 * 0

11. The content of SP and HL after the execution of instruction.

```
1000 LXI SP, 27FE
1003 CALL 1006
1006 POP H
```

(A) SP = 27FE, HL = 1003
(B) SP = 27FD, HL = 1003
(C) SP = 27FE, HL = 1006
(D) SP = 27FC, HL = 1006

12. In order to design a memory system of size 16 k bytes using chips with 11 address lines and 4 data lines each, how many chips are required
(A) 8 (B) 2
(C) 16 (D) 4

13. If the A contain 39 BCD, B contain 12 BCD then what will be the output of instructions?

```
ADD B
DAA
```

(A) 4 BH (B) 51 H
(C) B1H (D) 18 H

14. What are events followed by the instruction POP PSW in 8085 microprocessor?
(A) flag register ← [SP]
SP ← SP + 1
A ← [SP]
SP ← SP + 1
(B) SP ← SP + 1
flag register ← [SP]
SP ← SP + 1
A ← [SP]
(C) SP ← SP – 1
flag register ← [SP]
SP ← SP – 1
A ← [SP]
(D) flag register ← [SP]
SP ← SP – 1
SP ← SP – 1
[SP] ← A

Common Data for Questions 15 and 16: An 8085 assembly language program is given below.

```
Line 1:  MVI A, B5 H
     2:  MVI B, 0EH
     3:  XRA  A
     4:  ADD B
     5:  ANI 8CH
     6:  CPI 8DH
     7:  STA 3010 H
     8:  HLT
```

15. The contents of the accumulator just after execution of the ADD instruction in line 4 will be
(A) 00 H (B) C3 H
(C) 0CH (D) 0EH

16. After execution of line 7 of the program, the status of the *CY* and *Z* flags are
(A) $CY = 0, Z = 0$ (B) $CY = 0, Z = 1$
(C) $CY = 1, Z = 0$ (D) $CY = 1, Z = 1$

Practice Problems 2

Directions for questions 1 to 15: Select the correct alternative from the given choices.

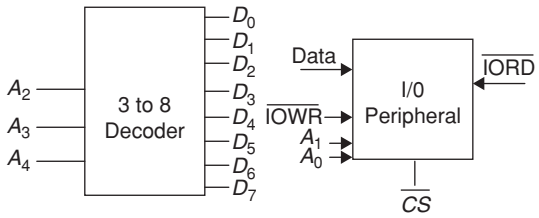
1. In an 8085 microprocessor, if we execute the instruction CMP B with content of B less than that of accumulator. As a result
(A) both carry flag and zero flag are set
(B) carry flag is set and zero flag is reset
(C) both carry flag and zero flag are reset
(D) carry flag is reset and zero flag is set

2. Match the number of machine cycles required to execute the instructions.

(i)	LHLD 2050 H	(1)	5
(ii)	LDA 2050 H	(2)	4
(iii)	LXI H, 2050 H	(3)	2
(iv)	XCHG	(4)	3
		(5)	1

(A) i – 1, ii – 2, iii – 4, iv – 5
(B) i – 1, ii – 2, iii – 4, iv – 3
(C) i – 1, ii – 5, iii – 1, iv – 3
(D) i – 2, ii – 1, iii – 1, iv – 5

3. An input/output peripheral is to be interfaced to an 8085 microprocessor. To select the input/output device in address range *E*1 to E3H, its $\overline{CS}$ should be connected to which of the decoder output pins?



(A) D_0 (B) D_7
(C) D_1 (D) D_3

4. An instruction that can be used so as to select only the higher 4-bits of accumulator in 8085 programming language
(A) ANI FOH (B) ANI OFH
(C) XRI OFH (D) XRI FOH

5. It is desired to multiply 0AH by 0BH and store the result in accumulator. The numbers are available in *C* and *D*. The steps required are
(A) MVI A, 00 H
LOOP: ADD C
DCR D
JNZ LOOP
HLT
(B) MVI A, 00 H
LOOP: JNZ LOOP
ADD C
DCR D
HLT
(C) MVI A, 00
LOOP: ADD C
JNZ LOOP
DCR D
HLT
(D) None of these

6. The content of accumulator after the execution of instruction
MVI A A7 H
ORA A
RLC
(A) CFH (B) 4FH
(C) 4EH (D) CEH

7. In the given program the number of times the first and second JNZ instruction causes the control to be transferred to LOOP are
MVI H, 02 H
MVI L, 05 H
LOOP: DCR L
FIRST: JNZ LOOP
DCR H
SECOND: JNZ LOOP
HLT
(A) 5 and 2 (B) 4 and 1
(C) 259 and 1 (D) 260 and 2

8. If the accumulator content is 27 H and if carry flag is already set, the instruction ACI 16 H will result in
(A) 3F H, $CY = 1$ (B) 39 H, $CY = 0$
(C) 3E H, $CY = 0$ (D) 3E H, $CY = 1$

9. Match the vectored interrupts with the address

A.	TRAP	(1) 002CH
B.	RST 7.5	(2) 003CH
C.	RST 6.5	(3) 0024 H
D.	RST 5.5	(4) 0034 H

(A) A – 2, B – 3, C – A, D – 1
(B) A – 3, B – 1, C – 2, D – 4
(C) A – 4, B – 2, C – 1, D – 3
(D) A – 3, B – 2, C – 4, D – 1

10. For the given program of 8085 µP what is the time interval between two MEMW signals.
START: MOV A, B
OUT 55
DCR B
STA FFF8 H
JMP START
(A) 5.8 µs (B) 6.2 µs
(C) 7.8 µs (D) 5.2 µs

11. Consider the following microprocessor programming code
L X I H, 5050 H
MOV A, M

MOV B , 05 H
ADD A, B
CMA
MOV M,A
HLT

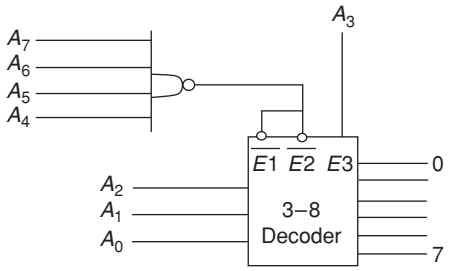
Memory location 5050 H is loaded with $(0A)_H$. The status of zero flag and carry flag after execution of CMA is

(A) $Z = 1, C = 1$ (B) $Z = 0, C = 1$
(C) $Z = 1, C = 0$ (D) $Z = 0, C = 0$

12. The last address location of a 1 KB memory chip is given as F080. The starting address will be

(A) EC 80 H (B) EC 81 H
(C) F000 H (D) EC00 H

13. A 3 – 8 decoder is used to decode the addresses and interface it to the microprocessor. Address lines are connected to the decoder as shown in the figure. The range of address possible to be selected by the given schematic is



(A) 88 H – 8 FH (B) F 0 H – F8 H
(C) F8 H – FFH (D) 00 H – FFH

14. Consider the following assembly language program.

MVI A, B3 H
MVI B, 10 H
XRI 69 H
ADD B
STA 3000 H
HLT

The content of accumulator after executing ADD instruction will be

(A) 69 H (B) DAH
(C) EAH (D) CIH

15. The status of control buses of an 8085 program is given below.

$IO/\overline{M}$ – HIGH

$\overline{RD}$ – LOW

$\overline{WR}$ – HIGH

The data in memory location 2500 H is 08 H. The output port is 25 H and input port is 20 H. The assembly language instruction being executed is

(A) IN 08 H (B) OUT 25 H
(C) OUT 08 H (D) IN 20 H

Previous Years' Questions

1. If the following program is executed in a microprocessor, the number of instruction cycles it will take from START TO HALT is **[2004]**

```
START MV1A, 14H  :  Move 14 H to register A
SHIFT RLC        :  Rotate left without carry
JNZ SHIFT        :  Jump on non-zero to SHIFT
HALT
```

(A) 4 (B) 8
(C) 13 (D) 16

2. The 8085 assembly language instruction that stores the contents of H and L registers into the memory locations 2050_H and 2051_H, respectively is: **[2005]**

(A) SPHL2050_H (B) SPHL 2051_H
(C) SHLD 2050_H (D) STAX 2050_H

3. A software delay subroutine is written as given below: **[2006]**

```
DELAY:  MVI  H,   255 D
        MVI  L,   255 D
LOOP:   DCR  L
        JNZ  LOOP
        DCR  H
        JNZ  LOOP
```

How many times DCR L instruction will be executed?

(A) 255 (B) 510
(C) 65025 (D) 65279

4. In an 8085, A microprocessor based system, it is desired to increment the contents of memory location whose address is available in (D.E) register pair and store the result in same location. The sequence of instructions is **[2006]**

(A) XCHG
INR M
(B) XCHG
INX H
(C) INX D
XCHG
(D) INR M
XCHG

5. Which one of the following statements regarding the INT (interrupt) and the BRQ (but request) pins in a CPU is true? **[2007]**

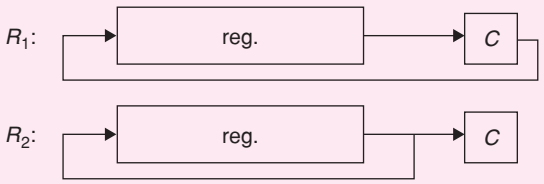
(A) The BRQ pin is sampled after every instruction cycle, but the INT is sampled after every machine cycle

(B) Both INT and BRQ are sampled after every machine cycle

(C) The INT pin is sampled after every instruction cycle, but the BRQ is sampled after every machine cycle

(D) Both INT and BRQ are sampled after every instruction cycle

Common Data for Questions 6 and 7: The associated figure shows the two types of rotate right instructions R_1, R_2 available in a microprocessor where reg. is a 8-bit register and C is the carry bit. The rotate left instruction L_1 and L_2 are similar except that C now links the most significant bit of reg. instead of the least significant one.



6. Suppose reg. contains the 2's complement number 11010110. If this number is divided by 2 the answer should be **[2007]**

(A) 01101011 (B) 10010101
(C) 11101001 (D) 11101011

7. Such a division can be correctly performed by the following set of operations **[2007]**

(A) L_2, R_2, R_1 (B) L_2, R_1, R_2
(C) R_2, L_1, R_1 (D) R_1, L_2, R_2

8. An input device is interfaced with Intel 8085A microprocessor as memory mapped I/O. The address of the device is 2500 H. In order to input data from the device to accumulator, the sequence of instruction will be **[2008]**

(A) LXI H, 2500 H
MOV A, M

(B) LXI H, 2500 H
MOV M, A

(C) LHLD 2500 H
MOV A,M

(D) LHLD 2500 H
MOV M,A

9. The contents (in Hexadecimal) of some of the memory locations in an 8085A based system are given below **[2008]**

Address	Contents
..	..
26FE	00
26FF	01
2700	02
2701	03
2702	04
..	..

The contents of stack pointer (SP), program counter (PC) and (H, L) are 2700 H, 2100 H and 0000 H respectively. When the following sequence of instructions are executed,

2100 H: DAD SP
2101 H: PCHL

the contents of (SP) and (PC) at the end of execution will be

(A) (PC) = 2102 H, (SP) = 2700 H
(B) (PC) = 2700 H, (SP) = 2700 H
(C) (PC) = 2800 H, (SP) = 26 FEH
(D) (PC) = 2A02 H, (SP) = 2702 H

10. The increasing order of speed of data access for the following devices is **[2009]**

(i) Cache memory
(ii) CDROM
(iii) Dynamic RAM
(iv) Processor registers
(v) Magnetic tape

(A) (v), (ii), (iii), (iv), (i)
(B) (v), (ii), (iii), (i), (iv)
(C) (ii), (i), (iii), (iv), (v)
(D) (v), (ii), (i), (iii), (iv)

11. In an 8085 microprocessor, the contents of the accumulator, after the following instructions are executed will become **[2009]**

XRA A
MVIB F0 H
SUB B

(A) 01 H (B) 0F H
(C) F0 H (D) 10 H

12. When a "CALL Addr" instruction is executed, the CPU carries out the following sequential operations internally where, **[2010]**

(R) means content of register R
((R)) means content of memory location pointed to by R
PC means Program Counter
SP means Stack Pointer

(A) (SP) incremented
(PC) ← Addr
((SP)) ← (PC)

(B) (PC) ← Addr
((SP)) ← (PC)
(SP) incremented

(C) (PC) ← Addr
(SP) incremented
((SP)) ← (PC)

(D) ((SP)) ← (PC)
(SP) incremented
(PC) ← Addr

13. A portion of the main program to call a subroutine SUB in an 8085 environment is given below. **[2011]**

```
        :
        :
    LXI D, DISP
LP: CALL SUB
        :
        :
```

It is desired that control be returned to LP + DISP + 3 when the RET instruction is executed in the subroutine. The set of instructions that precede the RET instruction in the subroutine are.

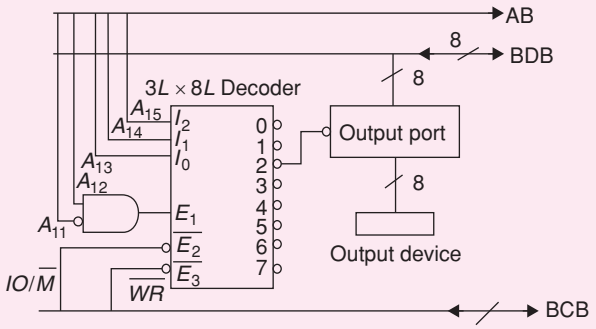
(A)
```
POP  D
DAD  H
PUSH D
```

(B)
```
POP  H
DAD  D
INX  H
INX  H
INX  H
PUSH H
```

(C)
```
POP  H
DAD  D
PUSH H
```

(D)
```
XTHL
INX  D
INX  D
INX  D
XTHL
```

14. An output device is interfaced with 8-bit microprocessor 8085A. The interfacing circuit is shown in figure **[2014]**



The interfacing circuit makes use of 3 line to 8 line decoder having 3 enable lines $E_1, \overline{E}_2, \overline{E}_3$. The address of the device is

(A) 50_H (B) 5000_H
(C) $A0_H$ (D) $A000_H$

15. In an 8085 microprocessor, the following program is executed **[2014]**

Address Location	Instruction
2000 H	XRA A
2001 H	MVI B, 04 H
2003 H	MVI A, 03 H
2005 H	RAR
2006 H	DCR B
2007 H	JNZ 2005
200A H	HLT

At the end of program, register A contains

(A) 60 H (B) 30 H
(C) 06 H (D) 03 H

Answer Keys

Exercises

Practice Problems 1

1. D	**2.** A	**3.** D	**4.** A	**5.** C	**6.** A	**7.** A	**8.** A	**9.** C	**10.** B
11. C	**12.** C	**13.** B	**14.** A	**15.** D	**16.** C				

Practice Problems 2

1. C	**2.** A	**3.** A	**4.** A	**5.** A	**6.** B	**7.** C	**8.** C	**9.** D	**10.** C
11. D	**12.** B	**13.** C	**14.** C	**15.** D					

Previous Years' Questions

1. A	**2.** C	**3.** D	**4.** A	**5.** A	**6.** D	**7.** A	**8.** A	**9.** B	**10.** B
11. D	**12.** D	**13.** B	**14.** B	**15.** A					

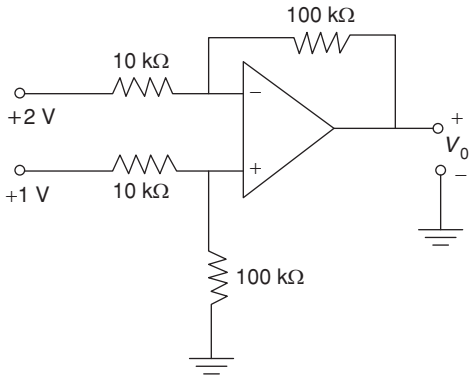
TEST
ANALOG AND DIGITAL ELECTRONICS

Time: 60 min.

Directions for questions 1 to 25: Select the correct alternative from the given choices.

1. Consider the following OP-Amp circuit:

What is the output voltage V_0 in the OP-Amp circuit?



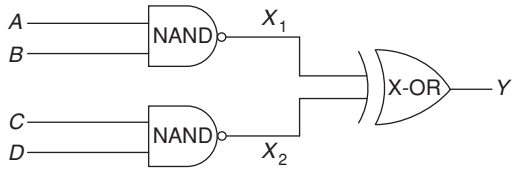
(A) +10 V
(B) –10 V
(C) +11 V
(D) –11 V

2. A 555 a stable oscillator with $R_1 = 40$ kΩ, $R_2 = 120$ kΩ and $C = 4{\cdot}0$ μF will oscillate at
(A) 1.288 Hz
(B) 443.5 Hz
(C) 443.5 kHz
(D) 1.288 kHz

3. The simplified SOP form for the Boolean expression $Y(A, B, C, D) = \Sigma\,(0, 1, 2, 3, 4, 5, 7)$ is

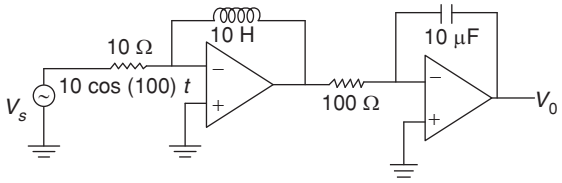
(A) $\overline{A}\,\overline{B} + \overline{A}\,\overline{C} + \overline{A}D$
(B) $\overline{A}\,\overline{B} + \overline{A}\,\overline{C} + \overline{A}B + CD$
(C) $\overline{A}\,\overline{C} + \overline{A}D + \overline{A}\,\overline{B} + C\overline{D}$
(D) $\overline{A}\,\overline{C} + \overline{A}D$

4. Which one of the following statements regarding the figure below is correct? A, B, C, D are input bits and Y is the output bit



(A) Output is zero when $A = B = C = D$
(B) $\overline{\overline{AB} + \overline{CD}} = Y$
(C) Y is always zero
(D) All are correct

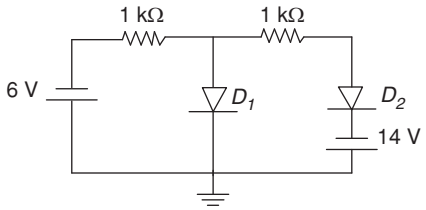
5.



In the figure, assume the OP-Amps to be ideal. The output V_0 of the circuit (in m V) is

(A) $10\cos(100\,t)$
(B) $10\int_0^t \cos(100\tau)d\tau$
(C) $10^{-4}\int_0^t \cos(100\tau)d\tau$
(D) $10^{-4}\dfrac{d}{dt}\cos(100t)$

6. The current through diode D_1 is [assume the diodes are ideal]

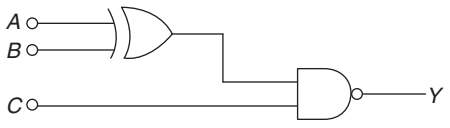


(A) 4 mA
(B) 6 mA
(C) 0 mA
(D) –2 mA

7. An amplifier circuit has an overall current gain of 100 and an input resistance of 20 kΩ with a load resistance of 2 kΩ. The overall voltage gain of the amplifier is _____.
(A) 2 dB
(B) 10 dB
(C) 20 dB
(D) 40 dB

8. The resolution of a 4-bit counting ADC is 0.5. For an analog input of 5.8 V, the digital output of the ADC will be _____.
(A) 1011
(B) 1100
(C) 1101
(D) 1110

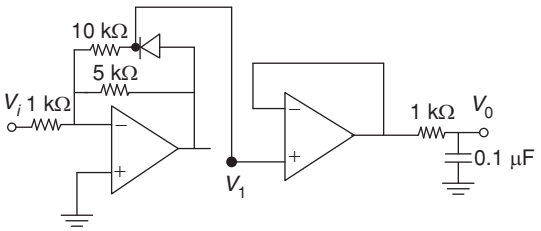
9. The Boolean expression for the output of the logic circuit shown in the following figure is



(A) $Y = \overline{A}\,\overline{B} + AB + \overline{C}$
(B) $Y = \overline{AB} + AB + \overline{C}$
(C) $Y = \overline{A}B + A\overline{B} + C$
(D) $Y = \overline{A}B + \overline{AB} + \overline{C}$

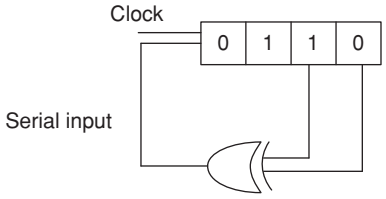
10. The number of memory chips of size 1 k × 4-bits required to build a memory bank of size 16 k × 8-bits is
(A) 64
(B) 32
(C) 16
(D) 8

11. The input voltage V_i in the circuit is a 2 kHz sine wave of 1 V amplitude. Assuming ideal operational amplifiers with ±15 V DC supply the average value of output voltage V_0 is (assume ideal diode)



(A) 3.33 V (B) 1.06 V
(C) 2.35 V (D) 4.71 V

12.



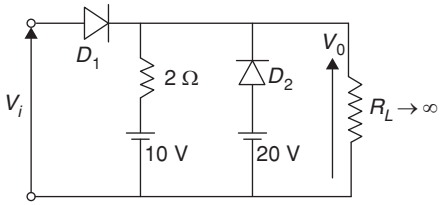
Initial contents of the 4-bit serial-in-parallel out right shift, shift register as shown in figure are 0110. After three clock pulses, the contents of the shift register will be
(A) 0000 (B) 0101
(C) 1010 (D) 1110

13. In an 8085 microprocessor, the contents of the accumulator, after following instructions are executed, will become

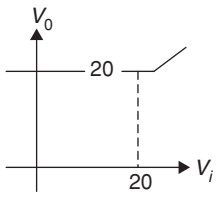
XRA	A
MVI	B, F0 H
SUB	B

(A) 01 H (B) 0F H
(C) F0 H (D) 10 H

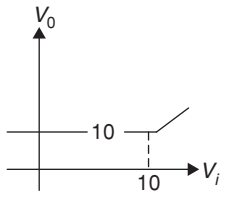
14. Assuming diodes D_1 and D_2 of the circuit shown in figure to be ideal ones, the transfer characteristics of the circuit will be



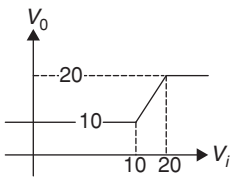
(A)



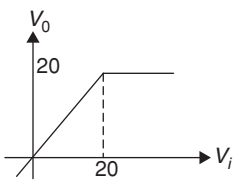
(B)



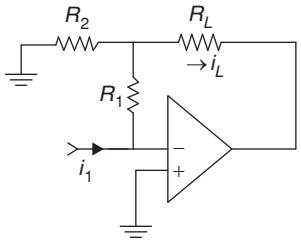
(C)



(D)



15. The below circuit shows a current controlled current source. The expression for $\frac{i_L}{i_1}$ is



(A) $\left(1+\frac{R_1}{R_2}\right)$

(B) $\left(1+\frac{R_L}{R_2}\right)$

(C) $\left(1+\frac{R_1+R_2}{R_L}\right)$

(D) $\frac{R_1}{R_2}$

16. The following program is written for an 8085 microprocessor to add two bytes, located at memory addresses 1 FFE and 1 FFF

```
LXI  H, 1FFE
MOV B, M
INR L
MOV A, M
ADD B
INR L
MOV M, A
XOR A
```

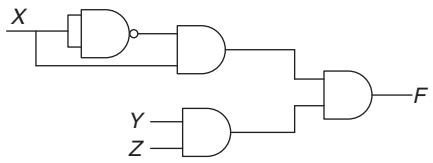
On completion of the execution of the program, the result of addition is found.
(A) in the register *A*
(B) at the memory address 1000
(C) at the memory address 1F00
(D) at the memory address 2000

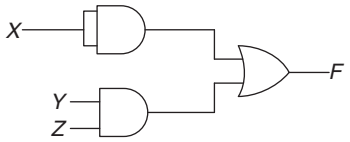
17. The following Karnaugh map represents a function *F*.

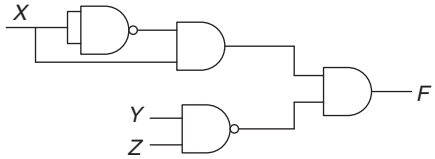
F

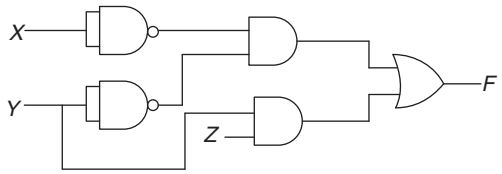
YZ / X	00	01	11	10
0	1	1	1	0
1	0	0	1	0

Which of the following circuits is a realization of the above function F?

(A)


(B)


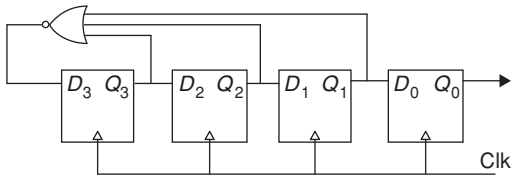
(C)


(D)


18. If $X = 1$ in the logic equation
$[X + Z\{\overline{Y} + (\overline{Z} + X\overline{Y})\}]\{\overline{X} + \overline{Z}(X + Y)\} = 1$, then,

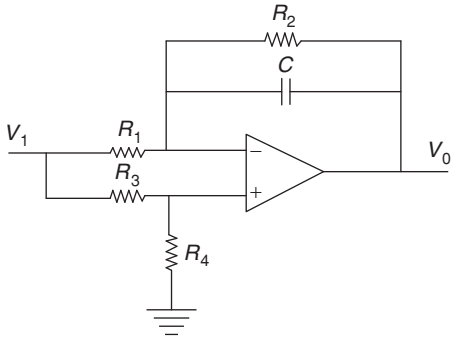
(A) $Y = Z$ (B) $Y = \overline{Z}$
(C) $Z = 1$ (D) $Z = 0$

19. For the ring counter in the figure, the initial state of the counter is 1110 (i.e., Q_3, Q_2, Q_1, $Q_0 = 1110$). The MOD number of the counter is



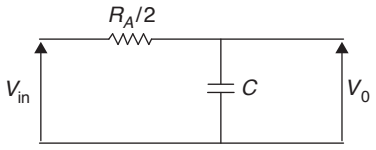
(A) 2 (B) 4
(C) 7 (D) 8

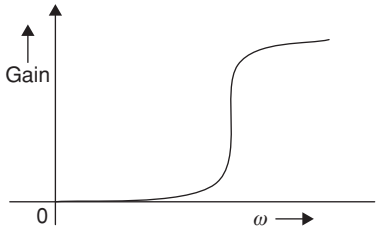
Common Data for Questions 20 and 21: A general filter circuit is shown in the following figure:

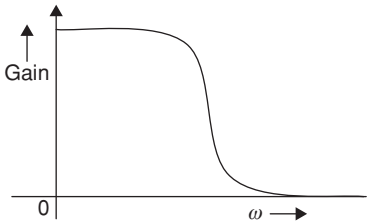


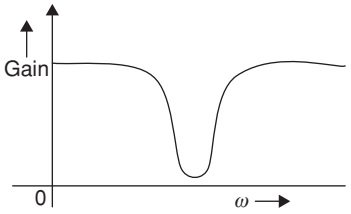
20. If $R_1 = R_2 = R_A$ and $R_3 = R_4 = R_B$, the circuit acts as
(A) all pass filter (B) band pass filter
(C) high pass filter (D) low pass filter

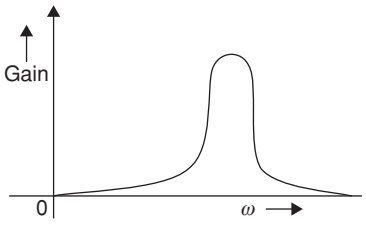
21. If the output of the above filter is given to the circuit shown below, the gain *Vs* frequency characteristic of the output V_0 will be

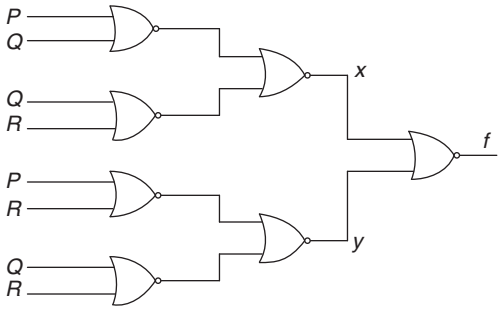


(A)


(B)


(C)


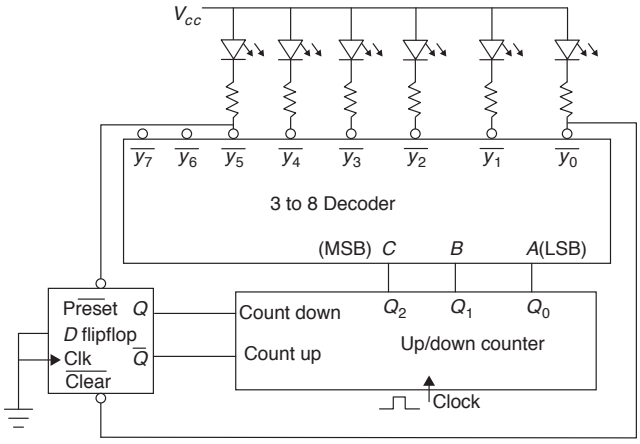
(D)


22.


What is the Boolean expression for the output f of the combinational logic circuit of NOR gates given above?

(A) $\overline{Q + R}$ (B) $\overline{P + Q}$
(C) $\overline{P + R}$ (D) $\overline{P + Q + R}$

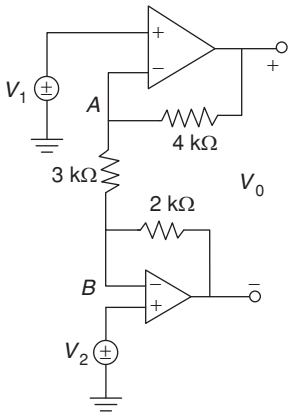
23. The circuit below shows an up/down counter working with a decoder and a flip flop. Preset and clear of the flip flop are asynchronous active low inputs.



Assume that initial values of counter output $(Q_2Q_1Q_0)$ as zeros. The counter output in decimal for next 12 clock cycles are

(A) 0, 1, 2, 3, 4, 4, 3, 2, 1, 1, 2, 3, 4
(B) 0, 1, 2, 3, 4, 5, 0, 1, 2, 3, 4, 5, 0
(C) 0, 1, 2, 3, 4, 5, 5, 4, 3, 2, 1, 0, 0
(D) 0, 1, 2, 3, 4, 5, 4, 3, 2, 1, 0, 1, 2

24. The gain of the amplifier $A_V = \dfrac{V_0}{(V_1 - V_2)}$ is?



(A) –9 (B) +9
(C) –6 (D) +3

25. A BJT is specified to have a maximum power dissipation P_{D0} of 5 W at an ambient temperature of 25°C and a maximum junction temperature of 150°C. Then how much power can be safely dissipated at an ambient temperature of 50°C.

(A) 6 W (B) 5 W
(C) 4 W (D) 3 W

Answer Keys

1. B	**2.** A	**3.** A	**4.** A	**5.** A	**6.** C	**7.** C	**8.** B	**9.** A	**10.** B
11. B	**12.** C	**13.** D	**14.** C	**15.** A	**16.** C	**17.** D	**18.** D	**19.** B	**20.** C
21. D	**22.** A	**23.** D	**24.** D	**25.** C					