Chapter 5

Operational Amplifiers

CHAPTER HIGHLIGHTS

- *Operational Amplifiers*
- *CMRR (Common Mode Rejection Ratio)*
- *Current – Mirror Circuit*
- *Electrical Parameters of op-Amp*
- *Open Loop op-Amp Configurations*
- *Closed Loop op-Amp Configurations*
- *Log and Antilog Amplifier*
- *Filters (Wide Band Pass and Wide Band Reject Filters)*
- *Oscillators*
- *RC–phase Oscillator and Twin-T Oscillator*
- *The Colpitts Oscillator and Armstrong Oscillator*
- *Hartley Oscillator, Clapp Oscillator and Crystal oscillator*
- *Waveform Generators and Wave Shaping Circuits.*
- *IC Voltage Regulators*

Operational Amplifiers

An operational amplifier is a direct coupled high gain, amplifier consisting of one or more differential amplifiers, usually followed by a level translator and an output stage. The output stage is generally a push–pull or push–pull complementary–symmetry pair

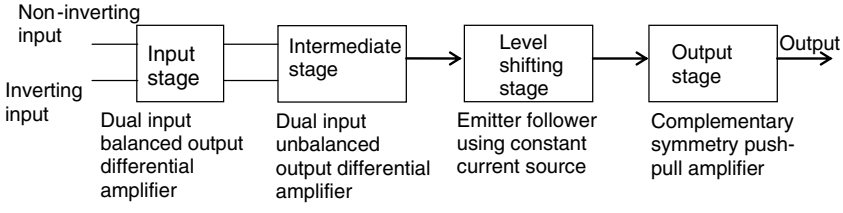
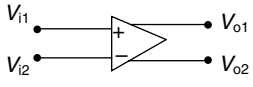


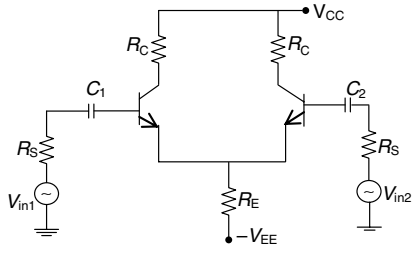
Figure 1 Block diagram of a typical op-amp

Differential Amplifier

Symbol



Circuit Diagram



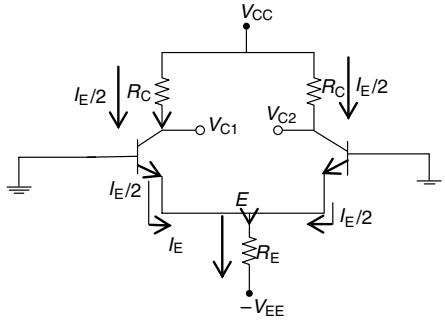
Modes of Operation

1. Single ended: Either of the input is grounded.
2. Double ended: Opposite polarity signals are applied at two inputs.
3. Common mode: Two similar input signals are applied at both inputs.

DC Analysis

(a) Make the AC sources ground.
(b) Replace the coupling capacitors open.

Equivalent Circuit



KVL at input side gives

$$0 - V_{BE} - V_E = 0$$

$$V_E = -0.7 \text{volts}$$

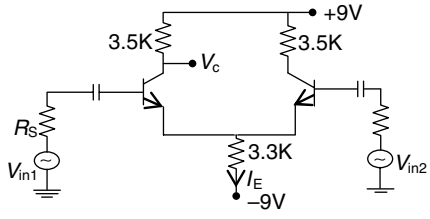
$$V_E - I_E R_E + V_{EE} = 0$$

$$I_E = \frac{V_{EE} - 0.7}{R_E}$$

Solved Examples

Example 1

Determine I_E and V_C for the given circuit.



(A) 4.1 volts, 5 mA (B) 5 volts, 2.5 mA
(C) 5 volts, 5 mA (D) 4.6 volts, 2.5 mA

Solution

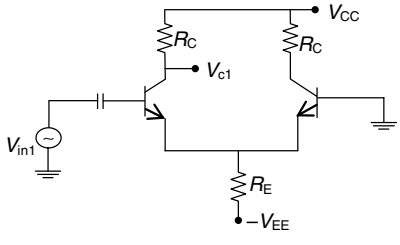
$$I_E = \frac{V_{EE} - 0.7}{R_E}$$

$$I_E = \frac{9 - 0.7}{3.3K} = 2.5 \text{ mA}$$

$$V_C = V_{CC} - \frac{I_E}{2} R_C$$

$$V_C = 4.6 \text{ votls.}$$

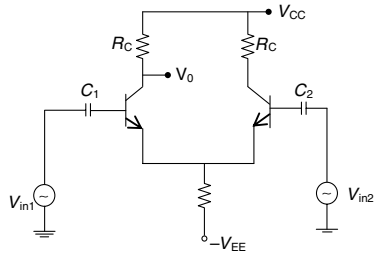
Single-ended operation



$$\text{Voltage gain } A_V = \frac{R_C}{2r_e} = \frac{VC1}{V_{in_1}}$$

$$\text{Input impedance } Z_i = 2\beta r_e$$

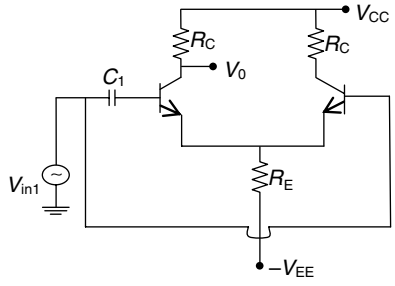
Double-ended operation



$$V_d = V_{in1} - V_{in2}$$

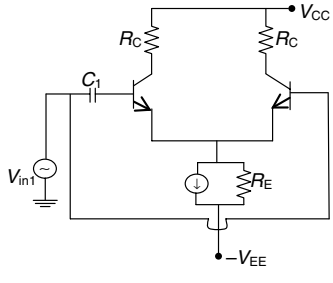
$$A_V = \frac{V_0}{V_d} = \frac{R_C}{2r_e}$$

Common-mode operation



$$A_C = \frac{V_0}{V_{in}} = \frac{\beta R_C}{\beta r_e + 2(\beta + 1)R_E}$$

In all IC design application, 'A_c' (common-mode gain) must be as small as possible. Hence, R_E has to be so large. Therefore, R_E is replaced by a constant current source to achieve smaller 'A_c'.



CMRR (Common-mode rejection ratio)

$$\text{CMRR} = \frac{A_d}{A_c}$$

$$\text{CMRR in dB} = 20 \log \left(\frac{A_d}{A_c} \right)$$

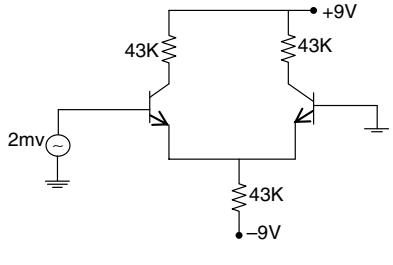
Where A_d = Differential gain

A_c = common mode gain

In all practical applications, CMRR should be as high as possible. Ideal value of CMRR = ∞

Example 2

Calculate the single-ended voltage gain for the given circuit?



(A) 100 (B) 91.2 (C) 87.4 (D) 83

Solution

$$A_v = \frac{R_C}{2r_e}$$

$$r_e = \frac{26\text{mV}}{I_{E_1}} = \frac{26\text{mV}}{I_{C_1}}$$

$$I_E = \frac{V_{EE} - 0.7\text{V}}{R_E} = 193\ \mu\text{A}$$

$$I_{C1} = \frac{I_E}{2} = 96.5\text{mA}$$

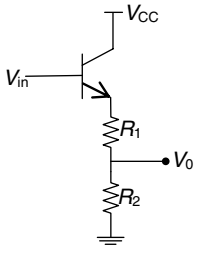
$$\therefore r_e = \frac{26\text{mv}}{96.5\mu\text{A}} = 269\ \Omega$$

$$A_v = \frac{R_C}{2r_e} = 87.4$$

Level Shifter

The purpose of the coupling capacitor in any amplifier is to block DC and allows AC. In the absence of a capacitor, level shifter circuit is used to block DC.

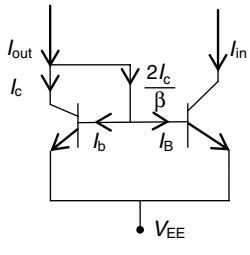
Simple Level Shifter



$$V_0 = V_{in}\frac{R_2}{R_1 + R_2}$$

Resistor R_2 not only level shifts DC by an amount $\frac{R_2}{R_1 + R_2}$ but also attenuates the AC signal. Remedy is to replace R_2 with current mirror circuit.

Current Mirror Circuit



If both transistors are assumed to be symmetrical,

$$I_{out} = I_C + \frac{2Ic}{\beta}$$

$$= I_C[1 + 2/\beta]$$

If 'β' is designed to be so large, then

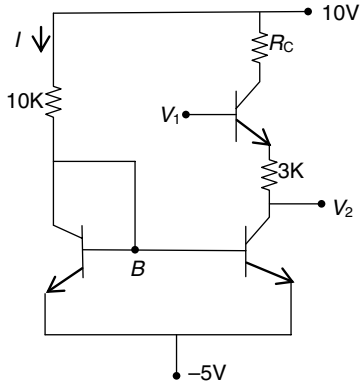
$$I_{out} \approx I_C \approx I_{in}$$

Advantage

1. I_C depends only on base current but not on the collector–emitter voltage.

Example 3

Find $V_1 - V_2$ level shift in the given circuit, if $V_{BE} = 0.7$volts and β is assumed to be so large?



(A) 4.52 (B) 5.23 (C) 4.99 (D) 6.25

Solution

$$V_B - 0.7 + 5 = 0$$

$$V_B = -4.3 \text{ volts}$$

$$I = \frac{10 - V_B}{10\text{K}} = 1.43 \text{ mA}$$

$\therefore$ Current through 3 kΩ resistor is 1.43 mA.

$$V_1 - V_2 = 0.7 + \text{I}(3\ \text{k}\Omega)$$

$$V_1 - V_2 = 4.99$$

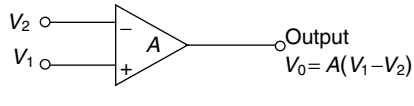
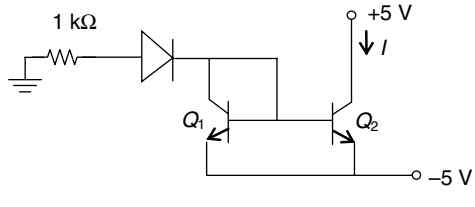


Figure 2 Schematic symbol for op-amp

Example 4

Two perfectly matched silicon transistors are connected as shown in the figure. Assuming β of the transistors to be very high and forward voltage drop in diode will be 0.7 V, then the value of current I is



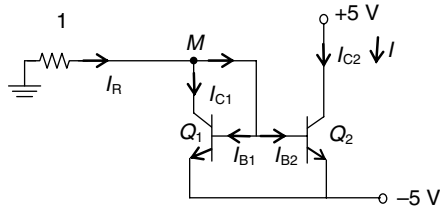
(A) 0 mA (B) 3.6 mA (C) 4.3 mA (D) 5.7 mA

Solution

Since both are perfectly matched

$$V_{BE1} = V_{BE2}$$

$$\frac{I_{C_1}}{I_{C_2}} = \exp\left[\frac{V_{BE1} - V_{BE2}}{V_t}\right] = e^0 = 1$$



Since β is the same for both transistors, $I_{B1} = I_{B2} = I_B$

By KVL in loop at Q_1 $I_R = \dfrac{0 - 0.7 - 0.7(-5)}{1\ \text{k}\Omega} = 3.6\ \text{mA}$

KCL at point, M

$$I_R = I_{C1} + 2I_B = I_{C1} + 2\frac{I_{C1}}{\beta}$$

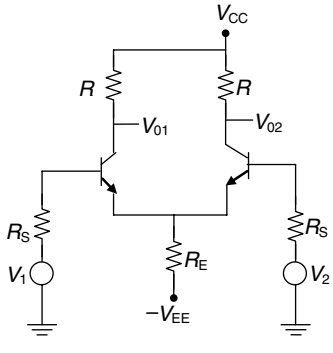
$$I_{C_1} = \frac{\beta}{\beta + 2} \cdot I_R$$

For large β

$$I_{C1} \approx I_R = 3.6\ \text{mA}$$

Direction for questions 5 to 7:

The differential amplifier as shown in figure has element values $R_C = 50\ \text{k}\Omega$, $r_\pi = 1\ \text{m}\Omega$, $R_s = 2\ \text{k}\Omega$, $R_E = 200\ \text{k}\Omega$, $\beta_0 = 2 \times 10^3$



Example 5

Differential mode voltage gain is

(A) –300 (B) –200 (C) –100 (D) 50

Solution

$$h_{fe} = \beta = 2 \times 10^3,\ r_\pi = 1\ \text{m}\Omega$$

$$R_C = R_L = 50\ \text{k}\Omega,\ R_E = 200\ \text{k}\Omega,\ R_S = 2\ \text{k}\Omega$$

$$A_{DM} = -\frac{h_{fe}R_L}{r_\pi} = -\frac{2\times10^3 \times 50 \times 10^3}{1\times10^6} = -100$$

Example 6

Common-mode voltage gain is

(A) –0.5 (B) –0.25 (C) –0.125 (D) 0

Solution

$$A_{CM} = -\frac{R_L}{2R_E} \text{ when } r_\pi > R_S$$

$$= -\frac{50k\Omega}{2\times200k\Omega} = -\frac{1}{8} = -0.125$$

Example 7

The value of CMRR in dBis

(A) 800 (B) 60 (C) 58 (D) ∞

Solution

$$\text{CMRR} = \frac{A_{DM}}{A_{CM}} = \frac{100}{0.125} = 800$$

$$\text{CMRR in dB} = 20 \log (800) = 58\ \text{dB}$$

Electrical Parameters of Op-Amp

Input offset voltage is the voltage that must be applied between the two input terminals of an op-amp to null the output.

The algebraic difference between the currents into the inverting and non-inverting terminals is referred to as input offset current $I_{io} = |I_{B1} - I_{B2}|$

Input bias current, I_B, is the average of the currents that flow into the inverting and non-inverting terminals of op-amp.

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

Common-mode rejection ratio is the ratio of differential voltage gain A_d to the common-mode voltage gain A_{CM}.

$$\text{CMRR} = \frac{A_d}{A_{CM}}$$

The higher the value of CMRR, the better is the matching between the input terminals.

The change in an op-amp input offset voltage V_{io} caused by variations in supply voltages is called the supply voltage rejection ratio (SVRR), PSRR.

Slew rate is defined as the maximum rate of change of output voltage per unit of time and is expressed in volt per microseconds.

$$\text{SR} = \left.\frac{dV_0}{dt}\right|_{\text{maximum}} \text{V/ms}$$

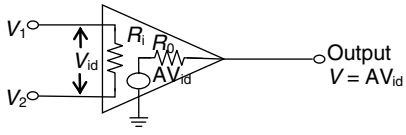
Slew rate indicates how rapidly the output of an op-amp can change in response to the changes in the input frequency, slew rate changes with change in voltage gain, and is normally specified at (+1) unity gain

The characteristics of ideal op-amp are as follows:

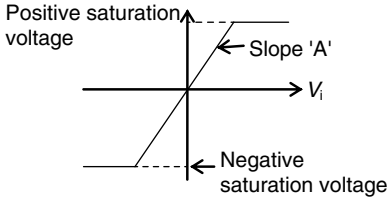
1. Infinite voltage gain (A).
2. Infinite input resistance (R_i).
3. Zero output resistance (R_0).
4. Zero output voltage when input voltage is zero.

5. Infinite bandwidth.
6. Infinite CMRR.
7. Infinite slew rate.

Equivalent Circuit of an Op-Amp

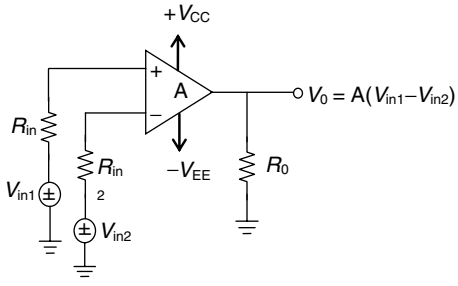


$$V_0 = AV_{id} = A(V_1 - V_2)$$

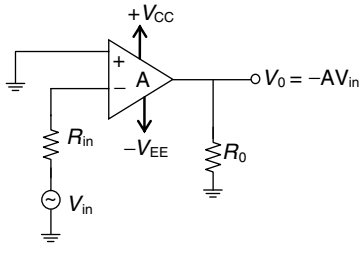


Open Loop Op-Amp

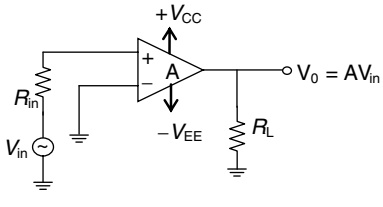
Differential Amplifier



The Inverting Amplifier



Non-inverting Amplifier

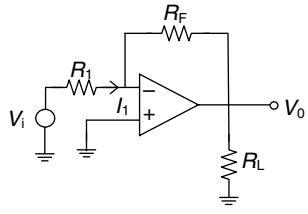


Very small values of input voltages can drive the open op-amp into saturation, as gain is very high, and this prevents the use of open loop configurations of op-amps in linear applications.

Very high gain of open loop op-amp as well as its variation with temperature, power supply, and production yield makes the open loop op-amp configuration, unsuitable for linear applications

Closed Loop Op-Amp Configurations

Inverting Amplifier

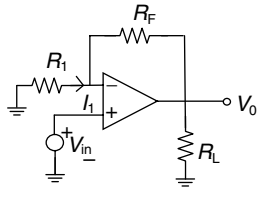


$$I_1 = \frac{V_i}{R_i},\ V_0 = -I_1 R_f = \frac{-R_f}{R_1} V_i$$

$$A_v = \frac{-R_f}{R_i}$$

This is voltage shunt feedback circuit

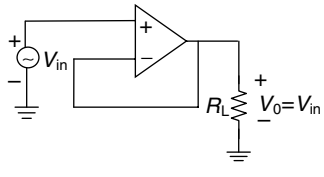
Non-Inverting Amplifier



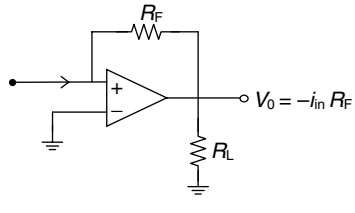
$$A_v = 1 + \frac{R_f}{R_i}$$

This is voltage series negative feedback configuration.

Voltage follower



Current to Voltage Converter



The introduction of negative feedback stabilizes the gain; however, it is also smaller than the open loop gain. On the other hand, positive feedback is necessary in oscillator circuits.

The use of negative feedback in a non-inverting amplifier increases the input impedance, and bandwidth, and decreases output resistance, total output offset voltage.

The input resistance of the inverting amplifier is relatively smaller because it depends on the resistance connected in series with the input signal source.

A special case of non-inverting amplifier is voltage follower, while the current to voltage converter is the special case of inverting amplifier. The voltage converter produces output voltage proportional to input current.

Differential Amplifiers

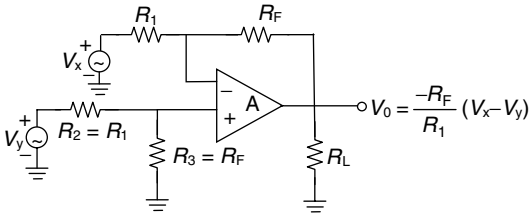


Figure 3 Differential amplifier with one op-amp

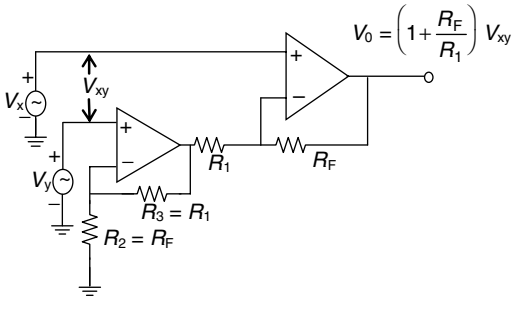
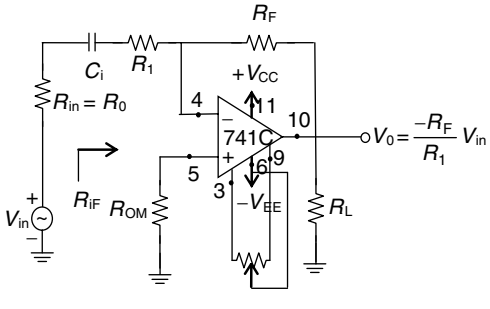


Figure 4 Differential amplifier with two op–amps

Negative feedback is also used in differential amplifier. The differential amplifier with one op-amp has the same characteristics as inverting amplifier, while the amplifier with two op-amps has the same characteristics as the non-inverting amplifier.

AC Amplifier – Inverting Amplifier



The coupling capacitor not only blocks the DC voltage but also sets the low-frequency cut-off limit.

$$f_L = \frac{1}{2\pi C_i (R_{iF} + R_o)}$$

The high-frequency cut-off f_H or high end of the bandwidth depends on the closed loop gain of the amplifier.

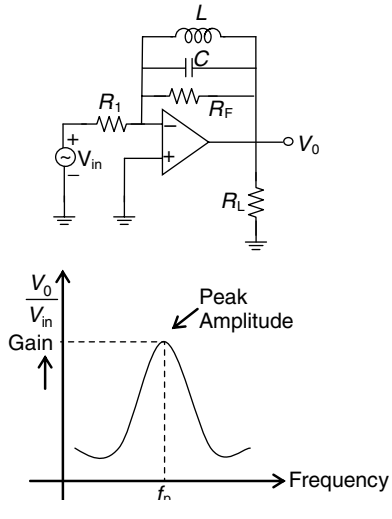
$$f_F = \frac{\text{(unity gain bandwidth)}}{A_F} \times k$$

$$\text{and } k = \frac{R_F}{R_1 + R_F},$$

$$A_F = \frac{-R_F}{R_i} \text{ (inverting amplifier)}$$

$$= 1 + \frac{R_F}{R_i} \text{ (non-inverting amplifier)}$$

The Peaking Amplifier



The peaking response, that is, the frequency response that peaks at a certain frequency, can be obtained by using a parallel LC network with the op-amp.

$$f_P = \frac{1}{2\pi\sqrt{LC}}, \text{ if } Q_{coil} \geq 10$$

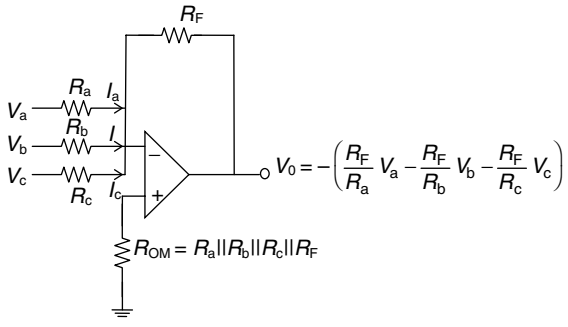
The gain of amplifier at resonance is maximum and is given by $A_F = \dfrac{-R_F \parallel R_P}{R1}$

R_P = equivalent resistance of the tank current = $Q^2_{coil}\, R$,

R = internal resistance of the coil

$$\text{BW} = \frac{f_p}{Q_p}, \; Q_p = R_F \parallel \frac{R_p}{X_L}$$

Weighted Amplifier



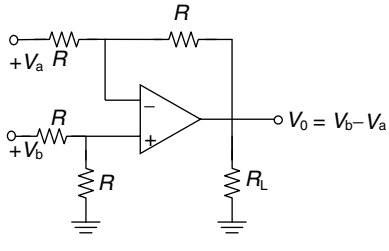
Summing Amplifier

$$R_a = R_b = R_c = R, \text{ then } V_0 = \frac{-R_F}{R}(V_a + V_b + V_c)$$

Averaging Amplifier

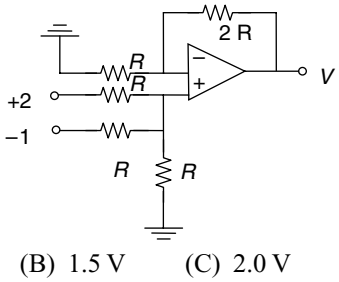
If $\frac{R_F}{R} = \frac{1}{n}$ for n inputs, then output is average of input voltages.

Subtractor



Example 8

The output voltage of the circuit



(A) 1.0 V (B) 1.5 V (C) 2.0 V (D) 3 V

Solution

$$V_o = \left(1 + \frac{2R}{R}\right)\left[\frac{R}{R+R} \times 2 + \frac{R}{R+R} \times (-1)\right]$$

$$= 3\left[\frac{1}{2} \times 2 - \frac{1}{2}\right] = 1.5\,V$$

Example 9

An op-amp has a differential gain of 10^3 and a CMRR of 100, the ouptut voltage of the op-amp with inputs 120 µV and 80 µV will be

(A) 26 mV (B) 41 mV (C) 100 mV (D) 200

Solution

$$CMRR = \left(\frac{A_d}{A_c}\right) = 100 \Rightarrow A_c = \frac{A_d}{100} = 10$$

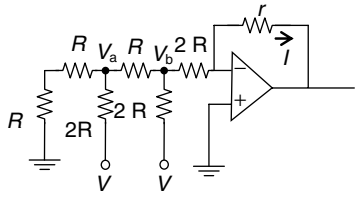
$$V_d = V_1 - V_2 = 40\ \mu V$$

$$V_c = \frac{V_1 + V_2}{2} = 100\ \mu V$$

$$V_o = A_d V_d + A_c . V_c = 10^3 \times 40 \times 10^{-6} + 10 \times 100 \times 10^{-6} = 41\ mV$$

Example 10

The current I through resistance r in the circuit is



(A) $\frac{-V}{4R}$ (B) $\frac{V}{6R}$ (C) $\frac{V}{12R}$ (D) $\frac{V}{3R}$

Solution

$$\frac{-V_a}{2R} = \frac{V_a - V}{2R} + \frac{V_a - V_b}{R}$$

$$4V_a = 2V_b + V \qquad (1)$$

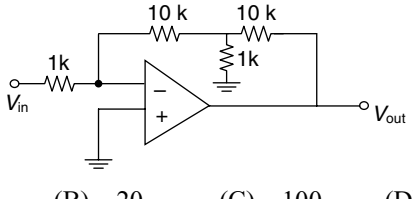
$$\frac{V_b - V_a}{R} + \frac{V_b - V}{2R} + \frac{V_b}{2R} = 0 \qquad (2)$$

So we get $-V_a = V_b = \frac{V}{6}$

$$I = \frac{V}{12R}.$$

Example 11

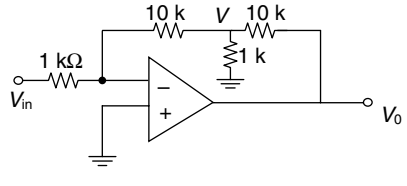
Assuming the op-amp to be ideal, the gain V_{out}/V_{in} for the circuit shown is?



(A) −1 (B) −20 (C) −100 (D) −120

Solution

Nodal equation at 'V'



$$\frac{V-0}{10}+\frac{V}{1}+\frac{V-V_{out}}{10}=0$$

$$12V=V_{out}$$

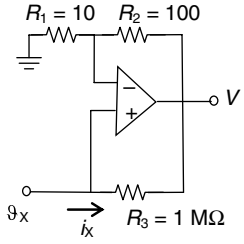
Nodal equation at inverting node, we get

$$\frac{V_{in}-0}{1}=\frac{0-V}{10}\Rightarrow V_{in}=\frac{-V}{10}$$

$$\frac{V_{out}}{V_{in}}=\frac{12}{-1/10}=-120$$

Example 12

Input resistance $R_{in}=(\vartheta_x/i_x)$ of the circuit is



(A) +100 kΩ (B) −100 kΩ
(C) + 1 mΩ (D) −1 mΩ

Solution

Using KCL at inverting terminal, we have

$$\frac{v_x-V}{R_2}+\frac{V_x-0}{R_1}=0$$

$$\frac{v_x}{V}=\frac{R_1}{R_1+R_2}$$

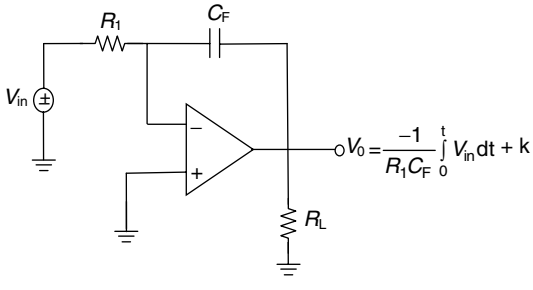
Using same at non-inverting terminal

$$i_x=\frac{v_x-V}{R_3}=\frac{v_x-v_x\left(\frac{R_1+R_2}{R_1}\right)}{R_3}$$

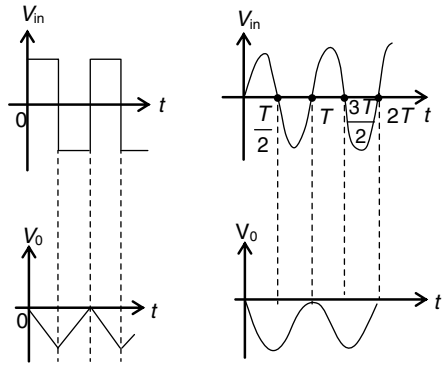
$$i_x=\frac{-v_x\ R_2}{R_1\ R_3}$$

$$R_{in}=\frac{v_x}{i_x}=\frac{-R_1\ R_3}{R_2}=-100\ k\Omega.$$

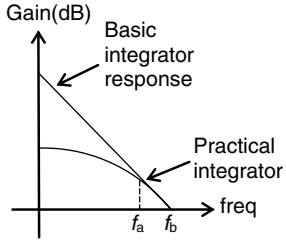
The Integrator



1. Basic Integrator

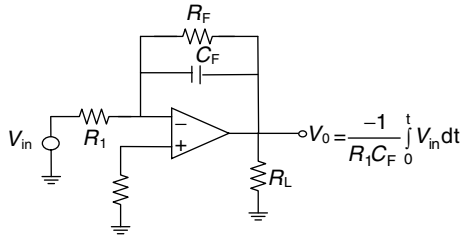


2. Input–output Wave Forms



$$f_b=\frac{1}{2\pi R_1C_F}$$

The stability and low-frequency roll off problem can be corrected by the addition of a resistor R_F as shown in the practical integrator.



The gain-limiting frequency $f_a=\dfrac{1}{2\pi R_FC_F}$

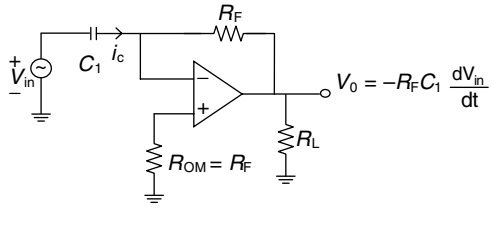
R_FC_F and R_1C_F values should be selected such that $f_a<f_b$

The input signal will be integrated properly if the time period 'T' of the signal is larger than or equal to R_FC_F

$$T\geq R_FC_F$$

where $R_FC_F=\dfrac{1}{2\pi f_a}$

The Differentiator



The output V_0 is equal to $R_F C_1$ times the negative instantaneous rate of change of input voltage V_{in} with time.

Differentiator performs the reverse of the integrator's function, a cosine wave input will produce a sine wave output, or a triangular input will produce a square wave output.

The frequency at which gain is zero is

$$f_a = \frac{1}{2\pi R_F C_1}$$

The gain $\frac{R_F}{X_{C1}}$ of the circuit increases with increase in frequency at a rate of 20 dB/decade. This makes the circuit unstable, also the input impedance X_{C1} decreases with increases in frequencies.

Both the stability and the high-frequency noise problems can be corrected by the addition of two components R_1 and C_F.

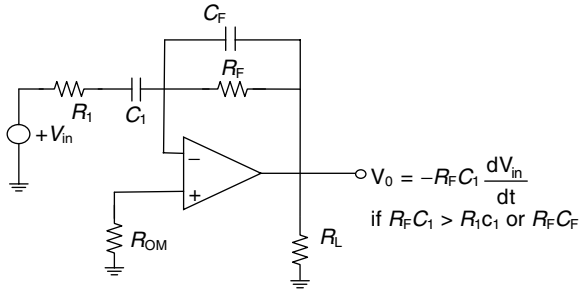
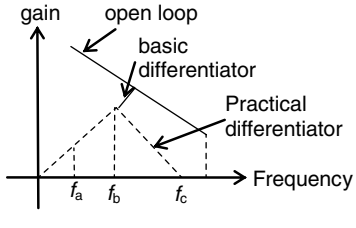


Figure 5 Practical differentiator



Frequency response

The gain-limiting frequency f_b is given by

$$f_b = \frac{1}{2\pi R_1 C_1}$$

Generally the values of f_a, f_b, f_c are

$$f_a = \frac{1}{2\pi R_F C_1}, f_b = \frac{1}{2\pi R_1 C_1}, f_c$$

$$f_c = \frac{1}{2\pi R_F C_F}$$

f_c = unity gain bandwidth

The input signal will be differentiated properly if time period (T) of input signal $T \geq R_F C_1$

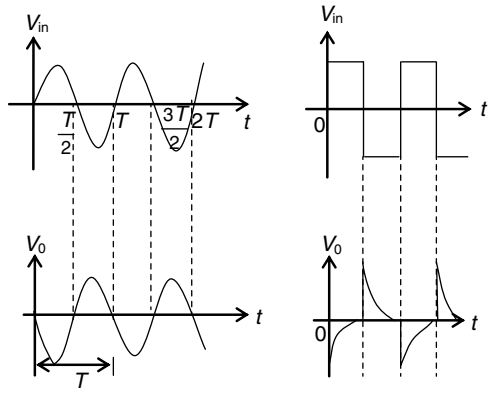
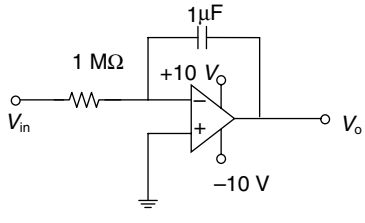


Figure 6 Input–output wave forms

Example 13

A unit positive step is applied at the input of the circuit shown in figure. After 20 sec, the output V_o will be



(A) +20 V (B) +10 V (C) −10 V (D) −20 V

Solution

$$V_0 = \frac{-1}{sCR} V_i = \frac{-1}{sCR} \cdot \frac{1}{s} (V_i \text{ is unit step})$$

$$= \left[\frac{-1}{s^2 RC}\right]$$

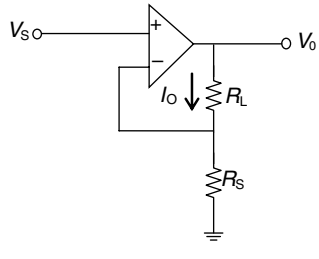
$$V_0 = \frac{-1}{RC} t \text{ after 20 seconds}$$

$$V_0 = \frac{-1}{1 \times 1} \times 20 = -20\text{V}$$

But $\pm V_{sat} = \pm 10$ V so output is −10 V.

Example 14

The current I_o is

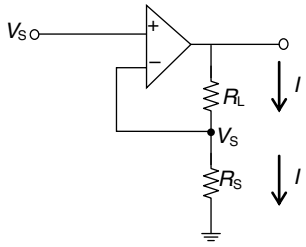


(A) $V_S \cdot \frac{R_L}{R_S (R_L + R_S)}$ (B) $\frac{V_S}{R_S}$

(C) $\frac{V_S}{R_L}$ (D) $V_S \left(\frac{1}{R_S} + \frac{1}{R_L}\right)$

Solution

No current flows into input $I_o = \dfrac{V(s)}{R(s)}$.



Example 15

The open loop voltage gain of an operational amplifier is 240. The noise level in the output without feed back is 100 mV, if negative feedback with $\beta = \dfrac{1}{60}$ is used, the noise level in the output will be

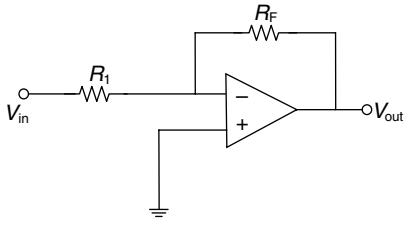
(A) 1.66 mV (B) 2.4 mV (C) 4.0 mV (D) 20 mV

Solution

$$N_f = \frac{N}{1+\beta A} = \frac{100}{1+\frac{1}{60}\times 240} = \frac{100\text{mV}}{5} = 20\text{mV}$$

Example 16

For the operational amplifier circuit shown in the figure, what is the maximum possible value of R_1 if the voltage gain required is between −10 and −25? Upper limit of $R_F = 1$ mΩ.



(A) ∞ (B) 1 mΩ (C) 100 kΩ (D) 40 kΩ

Solution

$$A_v = \frac{V_o}{V_{in}} = \frac{-R_F}{R_1}$$

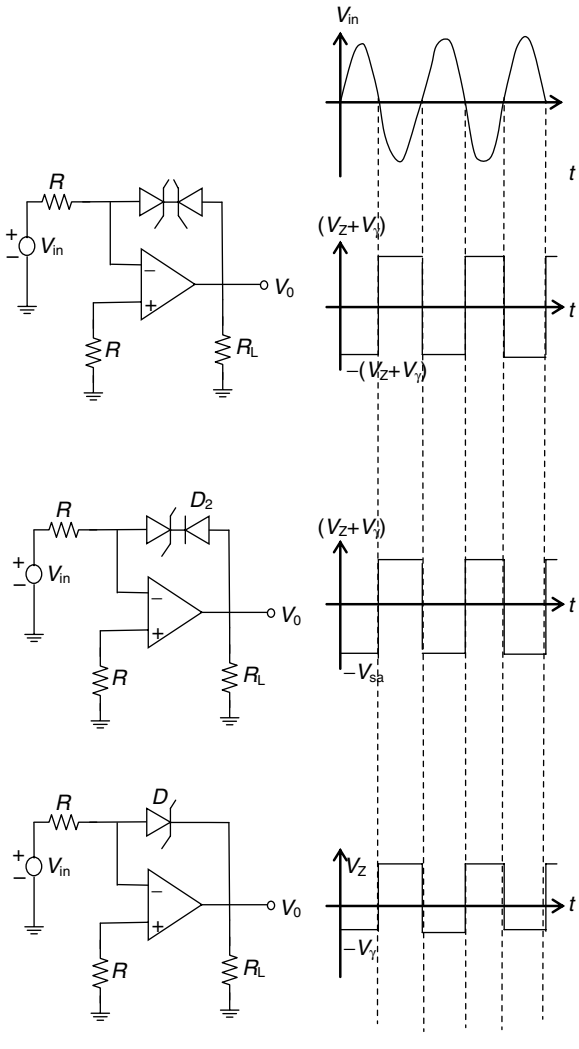
For $A_v = -10 = \dfrac{-R_F}{R_1} \Rightarrow R_1 = 100\ \text{k}\Omega$

For $A_v = -25 = \dfrac{-R_F}{R_1} \Rightarrow R_1 = 40\ \text{k}\Omega$

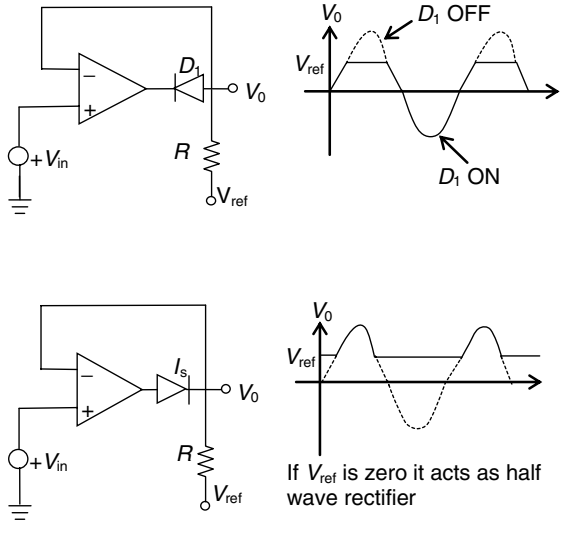
The maximum possible value of

$$R_1 = 100\ \text{k}\Omega$$

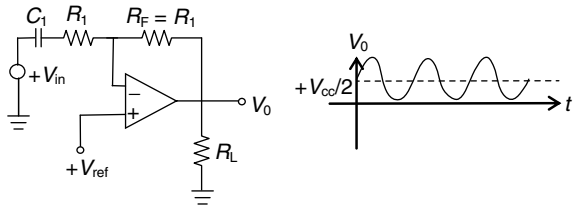
Voltage Limiters



Clippers

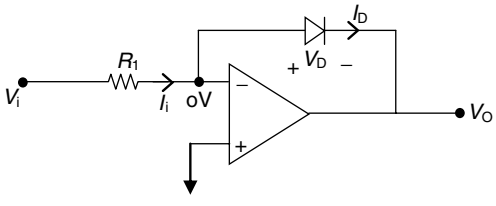


Clamper



Log and Antilog Amplifier

In logarithmic amplifier, output signal is logarithm of the input signal which can be obtain by using non-liner devices such as diode, transistor, etc.



If we apply KVL, then $V_o = -V_D$

As we know $I_D = I_S\, e^{\frac{V_0}{\eta V_f}}$

$$\Rightarrow V_D = \eta V_f \ln\left(\frac{I_D}{I_S}\right) = -V_D$$

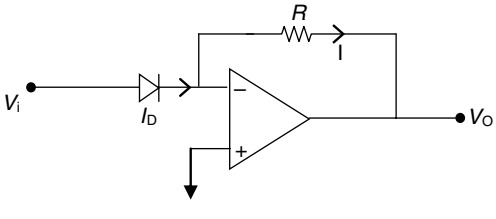
$$\Rightarrow V_D = \eta V_T \ln\left(\frac{I_S}{I_D}\right)$$

Where $I_D = \frac{V_L}{R_1} = I_i$

$$\Rightarrow V_D = \eta V_T \left[In\, I_s - In\frac{V_i}{R_1}\right]$$

Antilog amplifier

In this configuration, output voltage is an antilogarithm of input voltage.



From KCL

$$I_D = I = I_S\, e^{\frac{V_i}{\eta V_T}}$$

From KVL, $V_o = -V_R$

$$= -RI$$

$$= -R\left(I_S e^{\frac{V_i}{\eta V_T}}\right)$$

$$= -RI_S In^{-1}\left(\frac{V_i}{\eta V_T}\right)$$

Filters

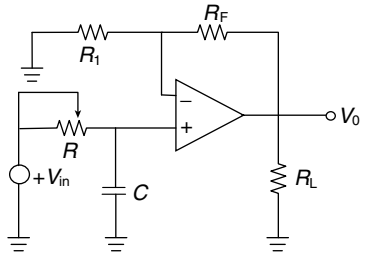
An electric filter is a frequency-selective circuit that passes a specified band of frequencies and blocks or attenuates signals of frequencies outside this band.

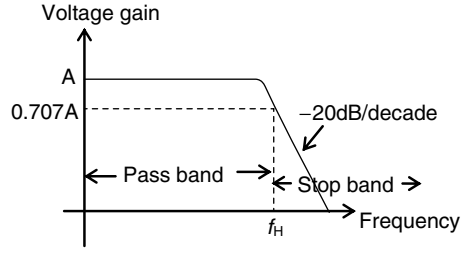
Filters can be classified in a number of ways:

1. Analog or digital: Analog filters are designed to process analog signals, while digital filters process analog signals using digital techniques.
2. Passive or active: Elements used in passive filters are resistors, capacitors, and inductors. Active filters on the other hand employ transistors or op-amps in addition to passive components.
3. Audio or radio frequency filters: The type of element used dictates the operating frequency range of the filter and RC filters are used for audio or low-frequency operation, whereas LC or crystal filters are employed at RF or high frequencies, especially because of their high Q value.

Most commonly used filters are shown below.

First-Order Low-Pass Butterworth Filter





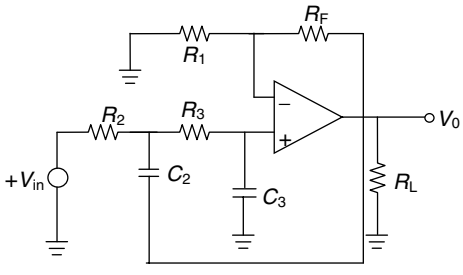
$$V_0 = \left(1 + \frac{R_F}{R_1}\right)\frac{V_{in}}{1 + j\left(\frac{f}{f_H}\right)}$$

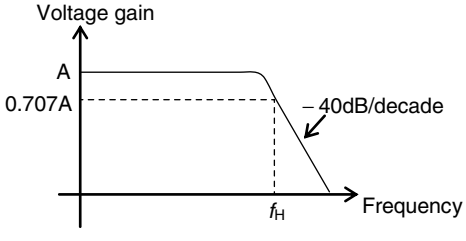
f = frequency of input signal

$$f_H = \frac{1}{2\pi RC} = \text{high cut-off frequency of filter}$$

$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_F}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}},\ \phi = \tan^{-1}\left(\frac{f}{f_H}\right)$$

Second-order Low-pass Butterworth Filter



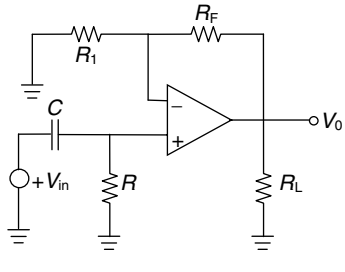


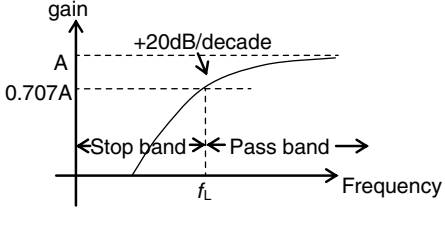
$$f_H = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$$

$$\left|\frac{V_0}{V_{in}}\right| = \left|\frac{A_F}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}}\right|$$

$$A_F = 1 + \frac{R_F}{R_1} \text{ pass band gain}$$

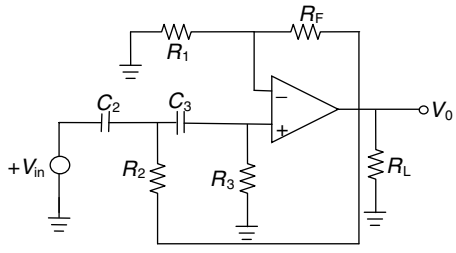
First-Order High-Pass Butterworth Filter

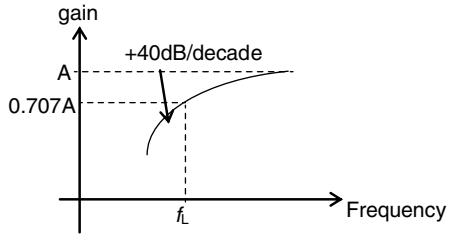




$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_F\left(\frac{f}{f_L}\right)}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}}, \quad f_L = \frac{1}{2\pi RC}$$

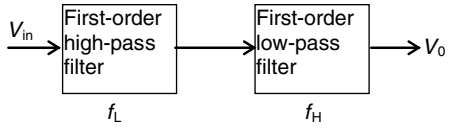
Second-order High-pass Butterworth Filter

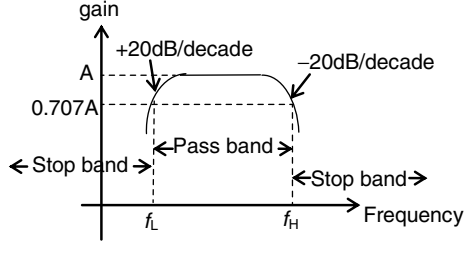




$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_F}{\sqrt{1+\left(\frac{f_L}{f}\right)^4}}, \quad f_L = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$$

Wide Band Pass Filter





If figure of merit or Q factor Q < 10, then the filter is called as wide band pass filter.

$$Q = \frac{f_0}{BW} = \frac{f_0}{f_H - f_L}$$

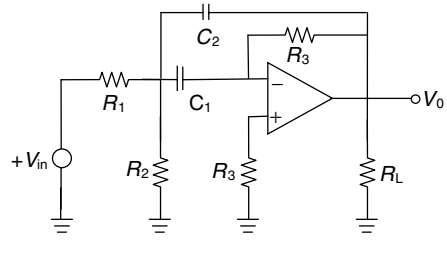
$f_0 = \sqrt{f_H f_L}$

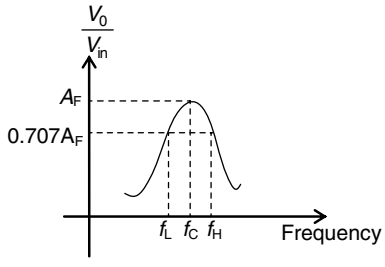
f_H = high cut-off frequency

f_L = low cut-off frequency

f_0 = resonance frequency

Narrow Band Pass Filter





if $C_1 = C_2 = C$

$$R_1 = \frac{Q}{2\pi f_c C A_F}, R_2 = \frac{Q}{2\pi f_C C(2Q^2 - A_F)}$$

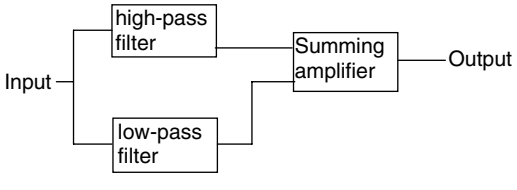
$$R_3 = \frac{Q}{\pi f_c}, A_F = \frac{R_3}{2R_1}, A_F = \text{gain at } f_c$$

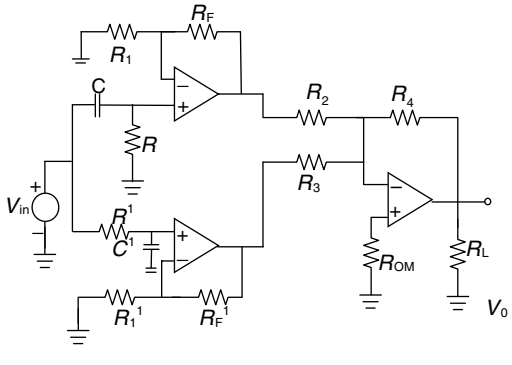
$$A_F < 2Q^2$$

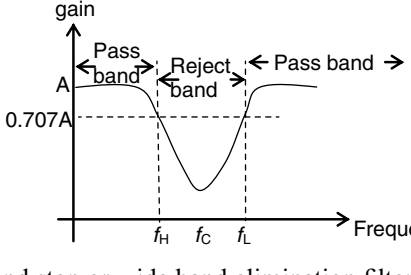
Another advantage of the multiple feedback filter is, its centre frequency f_c, can be changed, to a new frequency f_c^1, without changing the gain or bandwidth, this is accomplished by changing R_2 to R_2^1 so that

$$R_2^1 = R_2 \left(\frac{f_c}{f_c^1}\right)^2$$

Wide Band Reject Filter

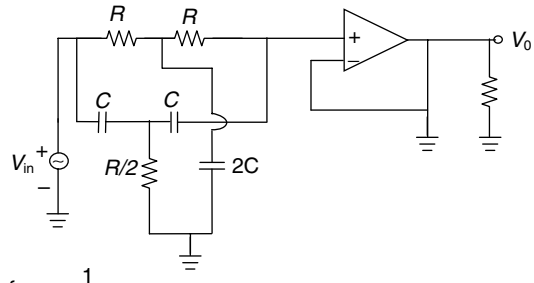




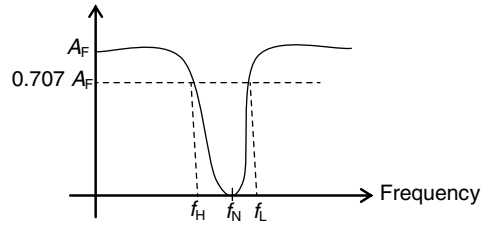


Wide band stop or wide band elimination filters have lower (Q < 10); narrow band reject filter or notch filter will have higher Q.

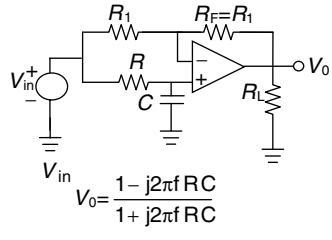
Narrow Band Reject Filter



$$f_N = \frac{1}{2\pi RC}$$



All Pass Filter



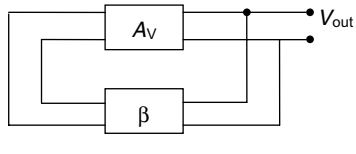
The phase shift between V_0 and V_{in} is a function of input frequency 'f'

$$\phi = -2\tan^{-1}\left(\frac{2\pi fRC}{1}\right)$$

Oscillators

Theory of Sinusoidal Oscillators

To build a sinusoidal oscillator, we need to use an amplifier with positive feedback, to use the feedback signal in place of the input signal. If the feedback signal is large enough and has the correct phase, there will be an output signal even though there was no external input signal.



In any oscillator, the loop gain $A_v\beta$ is greater than 1, when the power is first turned on. A small starting voltage (thermal noise) is applied to the input terminals and output voltage builds up, after the output voltage reaches a certain level, $A_v\beta$ automatically decreases to 1, and the peak-to-peak output becomes constant.

Gain without feedback = A_v

Gain with feedback $A_f = \dfrac{A_v}{A_V \beta}$

If $A_v \beta = 1 \Rightarrow A_f = \infty$

which means we can get the output with no input. However, oscillator works on circuit transients.

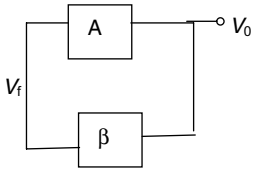
Barkhausen's Criterion

1. Magnitude of loop gain is unity.
2. Phase angle of loop gain is 0° or 360°

Steps to solve an oscillator problem are as follows:

(a) Find β, $\beta = \dfrac{V_f}{V_0}$

$\beta = \beta_{real} + \beta_{imaginary}$



(b) Find $A = \dfrac{V_0}{V_f}$

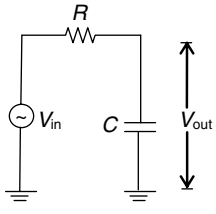
Equate = $A\beta = 1$

Equate real parts and imaginary parts to get the frequency of oscillations and conditions for sustained oscillation.

The Wien Bridge Oscillator

The Wien bridge oscillator is standard circuit for low to moderate frequencies in the range of 5 Hz to about 1 MHz.

Lag Circuit



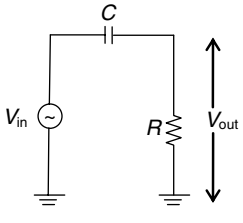
$$\frac{V_{out}}{V_{in}} = \frac{X_c}{\sqrt{R^2 + X_c^2}}$$

The phase angle

$$\phi = -\tan^{-1}\left(\frac{R}{X_c}\right)$$

Negative sign in phase angle represents the output voltage lags the input voltage.

Lead Circuit



$$\frac{V_{out}}{V_{in}} = \frac{R}{\sqrt{R^2 + X_c^2}}$$

$$\phi = \tan^{-1}\left(\frac{X_c}{R}\right)$$

The phase angle is positive, which means that the output voltage leads the input voltage.

Lead-lag Circuit

Wien bridge oscillator uses resonant feedback circuit called a lead-lag circuit.

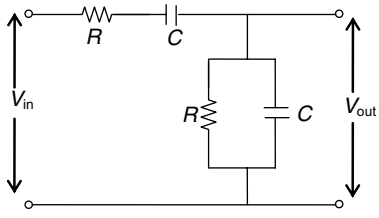


Figure 7 Lead-lag network

At very low frequencies, the series capacitor appears, open to the input signal, and there is no output signal, at very high frequencies, the shunt capacitor looks shorted, and there is no output. In between these extremes, the output reaches a maximum value at resonant frequency f_r, and at this frequency, the feedback fraction B reaches a maximum value of 1/3.

Resonant frequency $f_r = \dfrac{1}{2\pi RC}$

$$\beta\,(\text{gain}) = \frac{1}{\sqrt{9 - \left(\dfrac{X_c}{R} - \dfrac{R}{X_C}\right)^2}},$$

$$\phi = \tan^{-1}\left(\frac{X_E/R - R/X_c}{3}\right)$$

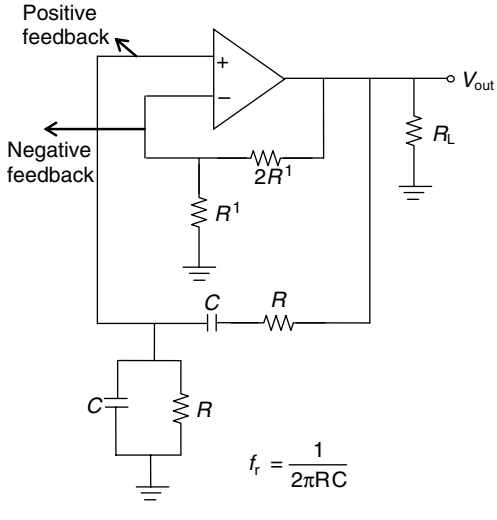


Figure 8 Wien bridge oscillator

It uses both positive and negative feedback.

The gain of the amplifier$(A_V) = 1 + \frac{2R^1}{R^1} = 3.$

At resonance ($X_c = R$), the gain of lead-lag network $\beta = \frac{1}{3}$

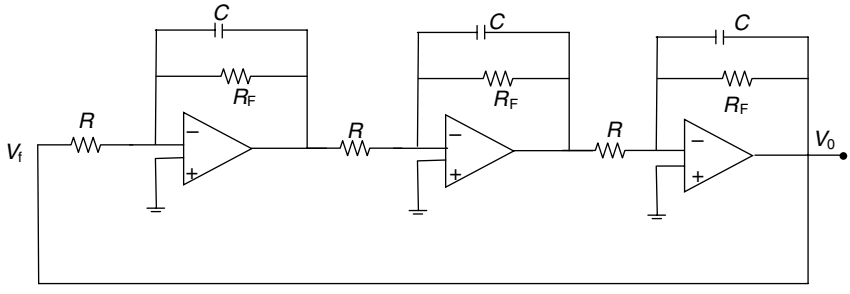
The loop gain $= A_V \beta = 1.$

The Wien bridge acts like a notch filter, a circuit with zero output at one particular frequencies, for a Wien bridge, the notch frequency equals to,

$$f_r = \frac{1}{2\pi RC}$$

Although it is superb at low frequencies, the Wienbridge oscillator is not suited to high frequencies (well, above 1 MH_Z). The main problem is the limited band width of op-amp.

RC–Phase Oscillator



Properties

1. Each section gives 120°phase shift.
2. Frequency of oscillations required is

$$F = \frac{\sqrt{3}}{2\pi R_f C}$$

3. Condition for sustained oscillations $R_F = 2R.$
4. Minimum gain required is $|A| \geq 2$

Phase-Shift Oscillator

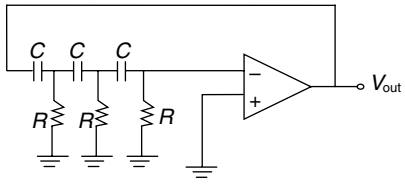


Figure 9 Phase-shift oscillator with three lead circuits in the feedback path

At some frequency, the total phase shift of the three lead circuits is 180°. The amplifier has an additional 180° of phase shift, because the signal drives the inverting input. As a result, the phase shift around the loop will be 360° equal to 0°.

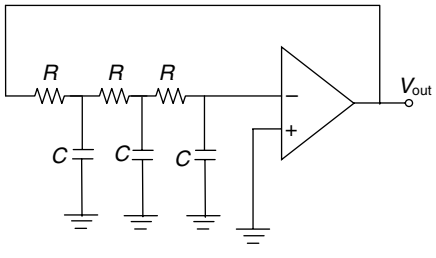
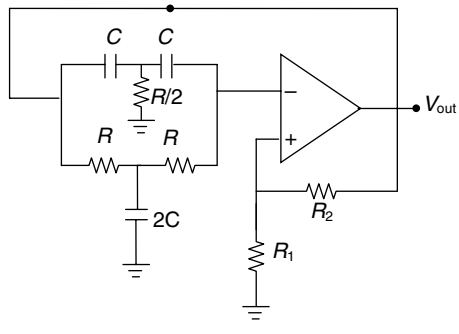


Figure 10 Phase shift oscillator with lag circuits

Properties

1. Each RC section does not produce 60° phase shift due to loading effect. However, three RC sections combinedly produces a phase shift of 180°.
2. Frequency of oscillations $f = \frac{1}{2\pi RC\sqrt{6}}$
3. Condition for sustained oscillations was $R_F = 29R_1.$
4. Minimum gain required was $|A| \geq 29$

Twin-T Oscillator



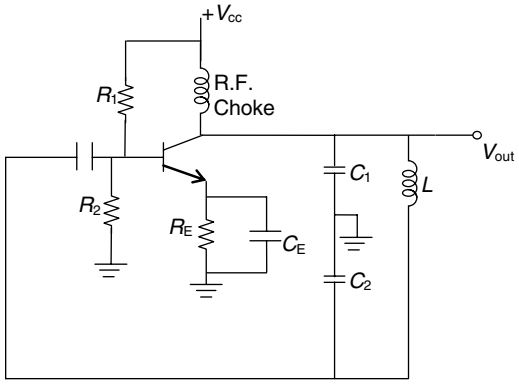
$$f_r = \frac{1}{2\pi RC}$$

The positive feedback to the non-inverting input is through a voltage divider. The negative feedback is through the twin T-filter.

To ensure that the oscillation frequency is close to the notch frequency, the voltage divider should have R_2 much larger than R_1. This forces the oscillator to operate at a frequency near the notch frequency.

It works only at one frequency is the limitation, and it cannot be easily adjusted over a large-frequency range.

The Colpitts Oscillator

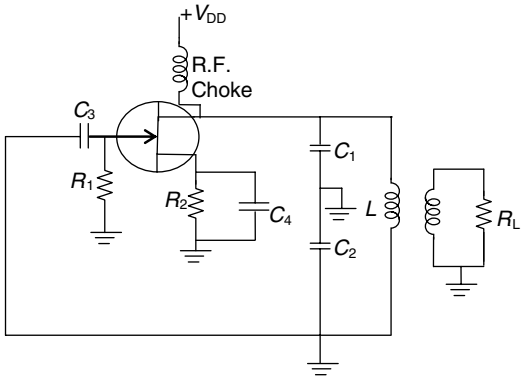


CE connection, Colpitts oscillator

$$\text{resonant frequency } f_r = \frac{1}{2\pi\sqrt{LC}}$$

$$C = \frac{C_1 C_2}{C_1 + C_2},$$

For $A_V\, B \geq 1$, $B = \frac{C_1}{C_2}$, $A_V = \frac{C_2}{C_1}$

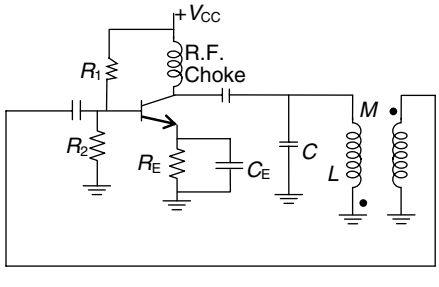


JFET oscillator has less loading effect on tank circuit.

$$\text{Resonant frequency } f_r = \frac{1}{2\pi\sqrt{LC}}$$

$$C = \frac{C_1 C_2}{C_1 + C_2},\ B = \frac{C_1}{C_2},\ A_{V(\min)} = \frac{C_2}{C_1}$$

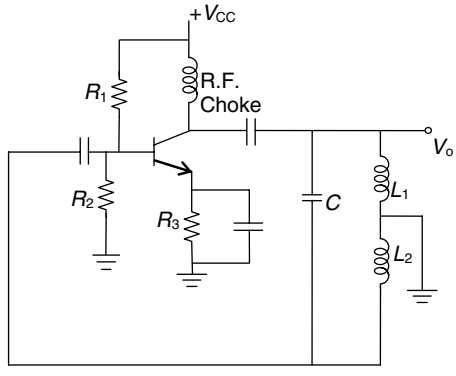
Armstrong Oscillator



$$f_r = \frac{1}{2\pi\sqrt{LC}},\ B = \frac{M}{L},\ A_{V(\text{mid})} = \frac{L}{M}$$

M-Mutual inductance at output.

Hartley Oscillator



Hartley oscillator

$$f_r = \frac{1}{2\pi\sqrt{LC}},\ L = L_1 + L_2,\ B = \frac{L_2}{L_1},\ A_{V(\min)} = \frac{L_1}{L_2}$$

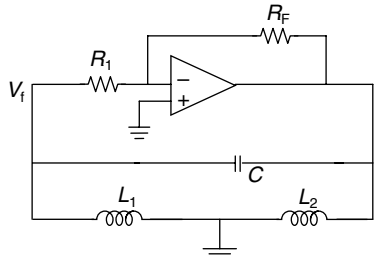


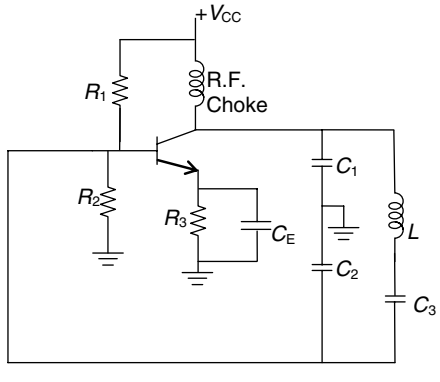
Figure 11 Hartley oscillator by using op-amp

$$\text{Frequency of oscillation } f = \frac{1}{2\pi\sqrt{L_{eq} \cdot C}}$$

$$L_{eq} = L_1 + L_2 + 2M \text{ (series aiding)}$$

$$= L_1 + L_2 - 2M \text{ (series opposing)}$$

Clapp Oscillator



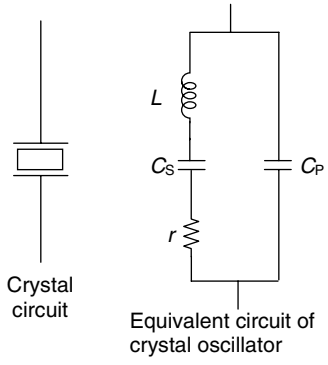
$$f_r = \frac{1}{2\pi\sqrt{LC}},$$

$$C = \frac{1}{1/c_1 + 1/c_2 + 1/c_3},\ B = \frac{C_1}{C_2}$$

$$A_{V(\text{mid})} = C_2/C_1$$

Crystal Oscillator

Piezoelectric crystal exhibits extremely stable resonance characteristics and very high Q factor.



→ Input impedance of crystal oscillator

$$Z = \frac{1}{SC_p + \dfrac{1}{SL + 1/SC_S}}$$

→ Crystal oscillator has two resonance frequencies

A series resonance is at $\omega_S = \dfrac{1}{\sqrt{LC_S}}$

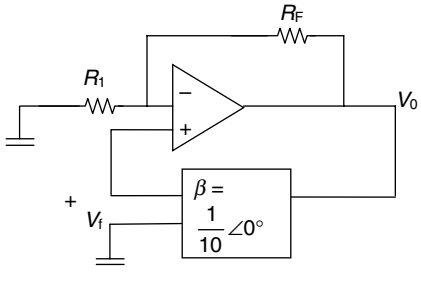
Parallel resonance is at $\omega_P = \dfrac{1}{\sqrt{L\left(\dfrac{C_S C_P}{C_S + C_P}\right)}}$

→ Crystal oscillator resonance frequencies range is of few kilo hertz to 100 mega hertz.

→ Crystal oscillators are fixed frequency circuits.

Example 17

Relation between R_1 and R_2 for sustained oscillations if $\beta = \dfrac{1}{10}\angle 0°$ for the following circuits.



(A) $R_F = 4R_1$ (B) $R_F = 10R_1$
(C) $R_F = 2R_1$ (D) $R_F = 9R_1$

Solution

$$A = 1 + \frac{R_F}{R_1}$$

$$A\beta = 1$$

$$\Rightarrow \left[1 + \frac{R_F}{R_1}\right]\frac{1}{10}\angle 0° = 1\angle 0°$$

$$1 + \frac{R_F}{R_1} = 10$$

$$R_F = 9R_1$$

Example 18

A Colpitts oscillator has a coil with an inductance of 50 μH and is tuned by a capacitor 400 pF across amplifier input and 200 pF across the output. What are the frequency of oscillation and the minimum gain for maintaining oscillations?

(A) 1.95 MHz, 3 (B) 1.95 MHz, 2
(C) 2.9 MHz, 3 (D) 2.9 MHz, 2

Solution

For Colpitts oscillator

$$f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}},\ C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

$$C_{eq} = \frac{400 \times 200}{600} = 133.33 \text{ pF}$$

$$f_0 = \frac{1}{2\pi\sqrt{50 \times 133.33 \times 10^{-18}}} = 1.95 \text{ MHz}$$

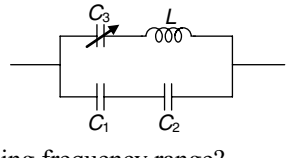
For maintaining oscillations, $A\beta \geq 1$

$$A_{loop} = A_{v0} \cdot \frac{C_2}{C_1} = 1$$

$$A_{v0} = \frac{C_1}{C_2} = \frac{400}{200} = 2$$

Example 19

A clapp oscillator has the following circuit components C_1 = 5,000 pF, C_2 = 500 pF, L = 50 μH, and C_3 is a 50 to 250 pF variable capacitor.



Find out the tuning frequency range?

(A) 1.98 to 10.34 MHz (B) 2.34 to 11.56 MHz
(C) 3.35 to 12.5 MHz (D) 5.34 to 15.4 MHz

Solution

$$f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}},\ \frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$$

$$C_{eq} = \frac{5000 \times 500 \times 50}{5000 \times 500 + 5000 \times 50 + 500 \times 50}$$

$$= 45.045 \text{ pF for } C_3 = 50 \text{ pF}$$

$$f_0 = \frac{1}{2\pi\sqrt{50 \times 45.045 \times 10^{-18}}} = 3.35 \text{ MHz}$$

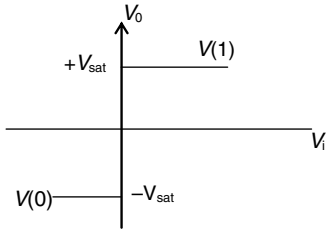
$$C_{eq} = 161.29 \text{ pF for } C_3 = 250 \text{ pF}$$

Then, $f_0 = 12.5$ MHz

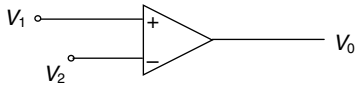
Waveform Generators and Wave-Shaping Circuits

Comparators

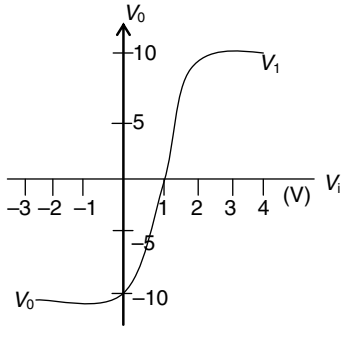
An analog comparator or simply comparator has two input voltages V_1 and V_2 and one output voltage V_0. Often one of the input (V_2) is a constant reference voltage V_R, and the other is a time-varying signal.



1. Transfer characteristics of ideal comparator

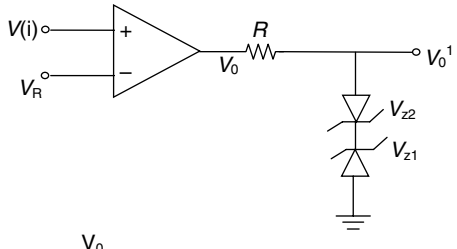


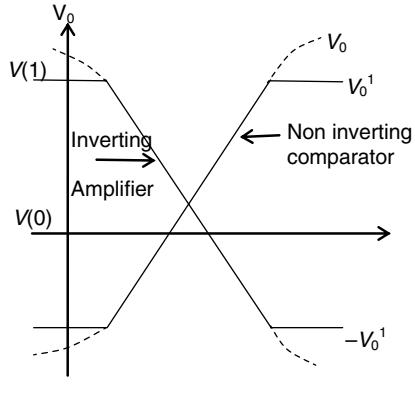
2. Op-amp operated in open loop becomes a comparator.



3. Transfer characteristics of practical comparator.

The input is compared with the reference, and the output is digitized into one of two states: $V_0 = V(0)$ when $v(i) < V_R$ and $V_0 = V(1)$ when $V_i > V_R$.





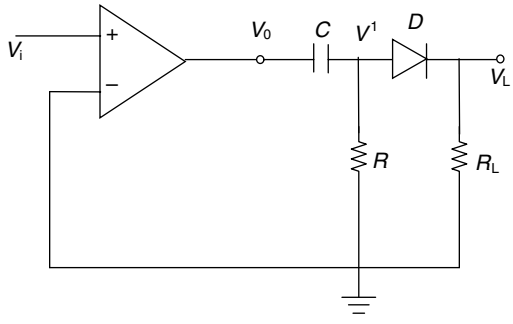
Practical comparator and transfer characteristics

To obtain limiting output voltages that are independent of the power supply voltages, a resistor R_1 and two back-to-back zenar diodes are added to clamp the output of comparator.

One more advantage of adding the zenar diodes is that the limiting may be much sharper for V_0^1 than for V_0 and disadvantage is poor transient response of the avalanche diode.

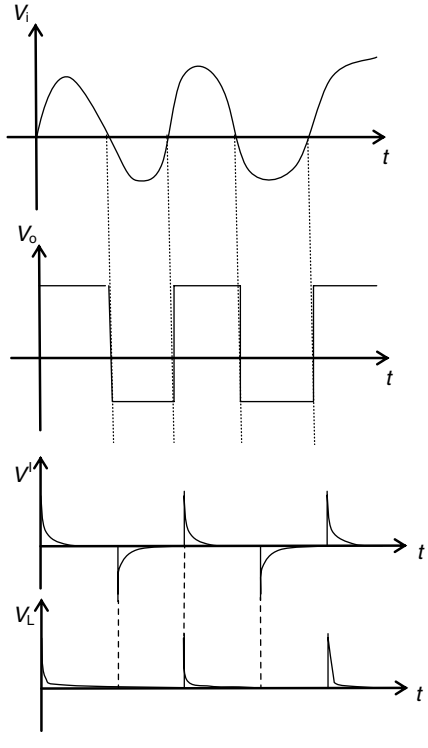
Square wave generation from sinusoid.

The comparator performs highly non-linear wave shaping because the output bears no resemblance to the input wave form.



A zero crossing detector converts the sinusoid input (V_i) into a square wave (V_0).

The pulse wave forms, V^1 and V_L, result from V_0 being fed into a short-time constant RC circuit in cascade with a diode clipper.

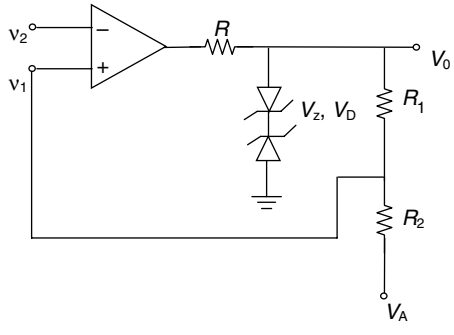


Here, a sinusoid has been converted into either a square wave or a pulse train.

Spurious positive and negative voltage spikes called noise super imposed on the input signal in the neighbourhood of the amplitude (V_R) may cause the output to chatter (change

from one binary voltage to another) several times before settling down to the correct level. This difficulty can be avoided if positive feedback or regeneration is added to a comparator.

Regenerative Comparator (Schmitt Trigger)



Schmitt trigger

$$V_0 = V_z + V_D,$$

Assume $v_2 < v_1$

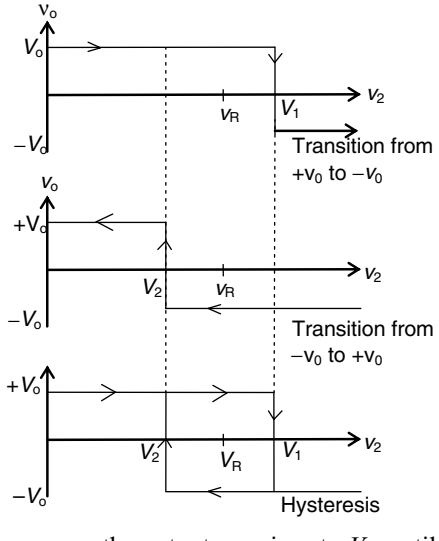
So that $V_0 = +V_0$,

and the voltage at the non-inverting terminal (v_1) is

$$V_1 = V_A + \frac{R_2}{R_1 + R_2}(V_0 - V_A)$$

If v_2 is now increased, the V_0 remains constant at V_0, and $v_1 = V_1 =$ constant until $v_2 = V_1$, and at this threshold critical, or triggering voltage, the output regeneratively switches to $v_0 = -V_0$ and remains at this value as long as $v_2 > V_1$.

The voltage at the non-inverting terminal (v_1) for $v_2 > V_1$ is $v_1 = V_A - \frac{R_2}{R_1 + R_2}(V_0 + V_A) = V_2$



If we decrease v_2, the output remains at $-V_0$, until v_2 equals the voltage at positive terminal, or until $v_2 = V_2$. At this stage, regenerative transition takes place and the output returns to $+V_0$ almost instantly. One of the most important uses made of the Schmitt trigger is to convert a slowly varying input voltage into an output wave from displaying an abrupt, almost discontinuous change.

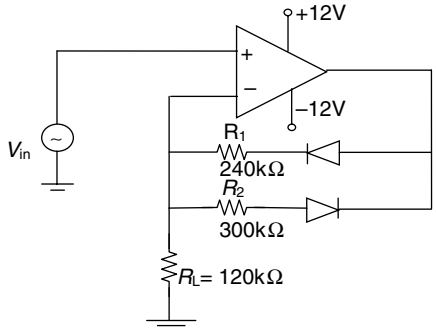
It is noted that $V_2 < V_1$, the difference between these two values is called hysteresis.

$$V_H = V_1 - V_2 = \frac{2R_2V_0}{R_1 + R_2}$$

UTP: (V_1) Output changes form $+V_{sat}$ to $-V_{sat}$
LTP: (V_2) Output changes form $-V_{sat}$ to $+V_{sat}$

Example 20

Find UTP, LTP, and hysteresis width for the following circuit assuming diodes are ideal.



Solution

UTP: $V_0 = +V_{sat}$; Upper diode is ON.

$$V_{UT} = +V_{sat} \cdot \frac{R_L}{R_1 + R_L}$$

$$V_{UTP} = \frac{12(120K)}{(360K)} = +4\text{volts}$$

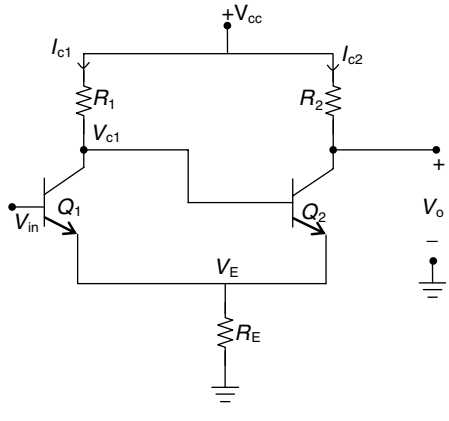
LTP: $V_0 = -V_{sat}$; Lower diode is 'ON'

$$V_{LTP} = \frac{V_{sat} \times R_L}{R_L + R_2}$$

$$V_{LTP} = \frac{-12(120K)}{(420K)} = -3.4\text{volts}$$

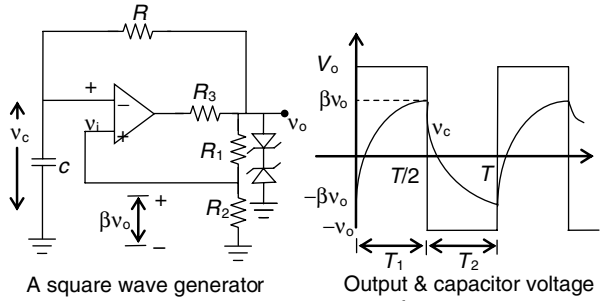
Hysteresis width = $V_{UTP} - V_{LTP} = 7.4$volts

Emitter-Coupled Schmitt Trigger



The basic emitter-coupled pair can be converted into a regenerative comparator. The resistances R_1 and R_2 are unequal ($R_1 > R_2$), and hence, Q_1 and Q_2 have different currents when saturated. This difference results in the hysteresis as different input voltages are required to saturate and cut off Q_1 and Q_2.

Square Wave Generator (Astable Multivibrator)



A square wave generator

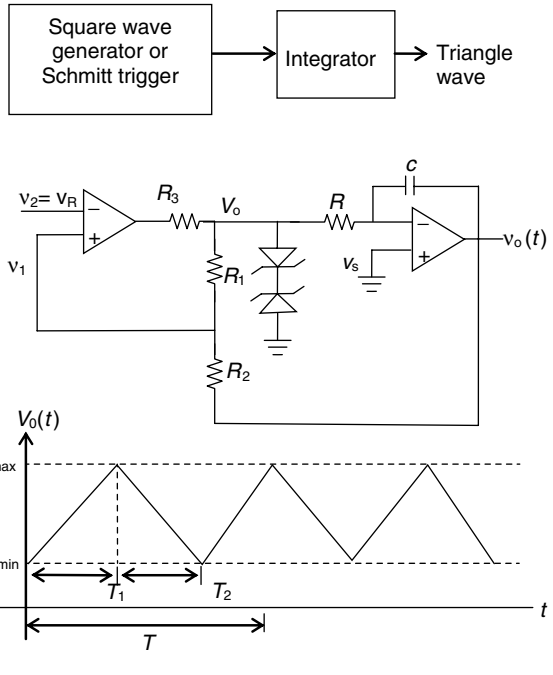
Output & capacitor voltage wave forms

The inverting Schmitt trigger can be used to obtain a free running square wave generator by connecting an RC network between output and the inverting input.

$$V_i = v_c - \beta v_0 = v_c - \frac{R_2}{R_1 + R_2}\ v_0$$

$$T = 2RC\,\ell_n\left(1 + \frac{2R_1}{R_2}\right), f_0 = \frac{1}{2RC} \text{ for } R_2 = 1.16R_1$$

Triangle Wave Generator



Output wave form,

$T_1 = T_2$ if $V_s = 0$,

$$V_{max} = V_R\left(\frac{R_1 + R_2}{R_1}\right) + V_0\,\frac{R_2}{R_1}$$

$$V_{min} = V_R\left(\frac{R_1 + R_2}{R_1}\right) - V_0\,\frac{R_2}{R_1}$$

Peak-to-peak swing

$$V_{max} - V_{min} = 2V_0\,\frac{R_2}{R_1}$$

$$T = \frac{4R_2RC}{R_1}\ f = \frac{1}{T}$$

The frequency is independent of v_0. The maximum frequency is limited by either the slew rate of the integrator or its maximum output current, which determines the charging rate of C.

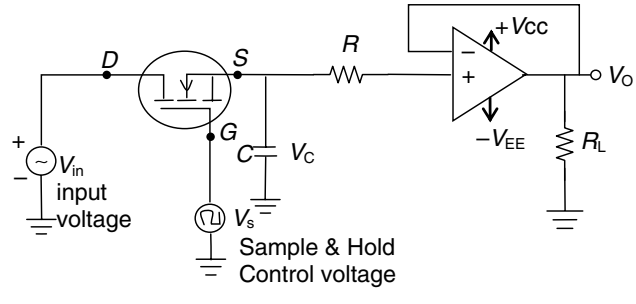
If unequal sweep intervals $T_1 \neq T_2$ is required apply $V_s \neq 0$ for integrator.

$$\text{Then } \frac{T_1}{T_2} = \frac{V_0 - V_s}{V_0 + V_s}$$

$$\text{duty cycle } \frac{T_1}{T_0} = \delta = \frac{1}{2}\left(1 - \frac{V_s}{V_0}\right)$$

Sample and Hold Circuit

The sample and hold circuit as it name implies, samples an input signal and holds on to its last sampled value until the input is sample again.



The analog signal V_{in} to be sampled is applied to the drain, and sample and hold central voltage (V_s) is applied to the gate of E-MOSFET.

During positive portion of V_s, the MOSFET conducts and acts as a closed switch. This allows the input voltage to charge capacitor C, that is, input voltage appears across C and in turn at the output.

When V_s is zero, the E-MOSFET is off (non-conductive) and acts as an open switch, the only discharge path for C is through op amp. However, the input resistance of op-amp is very high, So voltage across C is retained.

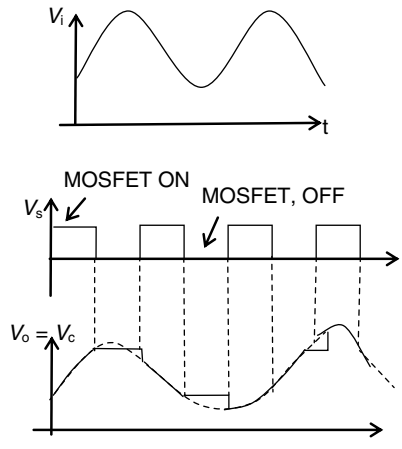
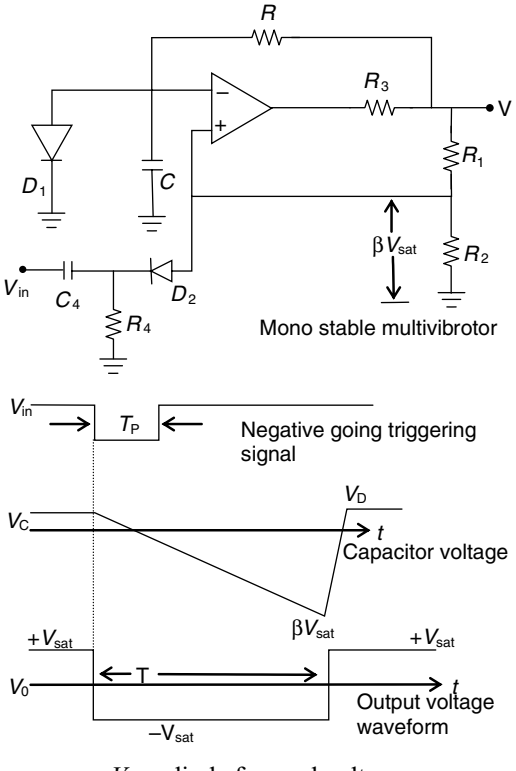


Figure 12 Input and output waveforms

To obtain close approximation of the input wave form, the frequency of the sample and hold control voltage must be significantly higher than that of the input. The sample and hold circuit is commonly used in digital interfacing and communications.

Monostable Multivibrator

Monostable multivibrator has one stable state and other is quasi stable state. The circuit is useful for generating single output pulse of adjustable time duration, in response to a triggering signal.



V_D – diode forward voltage

$$T = RC \ell n \frac{(1+V_D/V_{sat})}{1-\beta}$$

$$\beta = \frac{R_2}{R_1 + R_2}$$

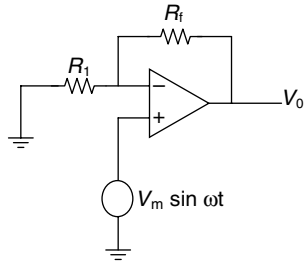
if $V_{sat} >> V_D$, $R_1 = R_2$ So that $\beta = 0.5$, then $T = 0.69$ RC

Let us assume that in the stable state, the output is at $+V_{sat}$. The diode D_1 conducts and V_c the voltage across capacitor gets clamped to 0.7 V.

The voltage at (+) input terminal through R_1, R_2 potentiometer divider is $+\beta V_{sat}$. Now, if a negative trigger of magnitude V_1 is applied to the (+) terminal. So that the effective signal at this terminal is less than 0.7 V. That is, $([\beta V_{sat} + (-V_1) < 0.7V)$. The output of op-amp will switch from $+V_{sat}$ to $-V_{sat}$ through the resistance R. The voltage at the (+) input terminal is now $-\beta V_{sat}$, when capacitor C voltage becomes just slightly more negative than this voltage. The output of op-amp switches back to $+V_{sat}$. The capacitor C now starts charging to $+V_{sat}$ through R until V_c clamped to 0.7V.

Example 21

The op-amp has a slew rate of $1V/\mu$ second. The unity gain frequency is 1 MHz and the output saturation levels are of ±14 V. What is the maximum output frequency at which undistorted output can be obtained?



(A) 15.4 kHz (B) 13.8 kHz
(C) 12.39 kHz (D) 11.36 kHz

Solution

$$\text{Slew rate} = \left.\frac{dV}{dt}\right|_{max} = \omega V_m$$

$$2\pi f_{max} V_m = \text{Slew rate}$$

$$f_{max} = \frac{\text{slew rate}}{2\pi V_m}$$

Here, slew rate = 1 V/μs

$$V_m = 14 \text{ V}$$

$$f_{max} = \frac{1/10^{-6}}{2\pi \times 14} = 11.36 \text{ kHz}$$

Example 22

The values of R_f, R_1 for a non-inverting amplifier to provide maximum low-frequency gain for a bandwidth of 100 kHz are

(A) 9 kΩ, 1 kΩ (B) 19 kΩ, 1 kΩ
(C) 29 kΩ, 1 kΩ (D) Cannot be determined

Solution

For 1 MHz bandwidth, gain = 1 (unity)

For 0.1 MHz, gain = $\frac{1}{0.1} = 10$

Closed loop gain = $10 = 1 + \frac{R_f}{R_1}$

$\Rightarrow R_1 = 1\ \text{k}\Omega,\ R_f = 9\ \text{k}\Omega.$

Example 23

The maximum peak-to-peak amplitude of the input signal of frequency 100 kHz for undistorted output?

(A) 15.9 V (B) 3.18 V
(C) 2.12 V (D) Not possible

Solution

Slew rate = $2\pi f_{max}.V_m$

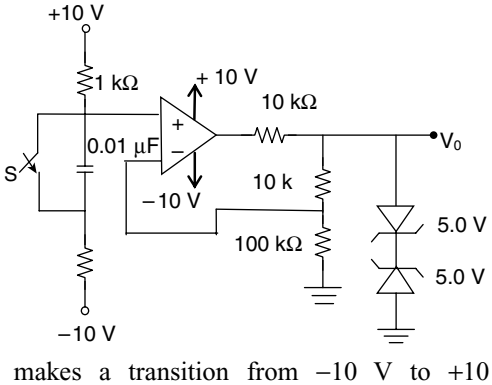
$$\text{Peak amplitude of input} = \frac{\text{Slew rate}}{2\pi f_{max}}$$

$$= \frac{1/10^{-6}}{2\pi \times 100 \times 10^3} = 1.59\ \text{V}$$

Peak to peak (P–P) = $2 \times 1.59\ \text{V} = 3.18\ \text{V}$

Example 24

The switch S in the circuit was initially closed and opened at time $t = 0$, you may neglect the zener diode forward voltage drops. What is the behaviour of V_{out} for $t > 0$?



(A) It makes a transition from −10 V to +10 V at $t = 12.98\ \mu\text{S}$.
(B) It makes a transition from −5 V to +5 V at $t = 2.57\ \mu\text{S}$.
(C) It makes a transition from +5 V to −5 V at $t = 2.57\ \mu\text{S}$.
(D) It makes a transition from +10 V to −10 V at $t = 12.95\ \mu\text{S}$.

Solution

It is a limiter circuit

It makes a transition from +5 V to −5 V

$$20\,(1 - e^{-t/Rc}) = 5 \times \frac{100}{110}$$

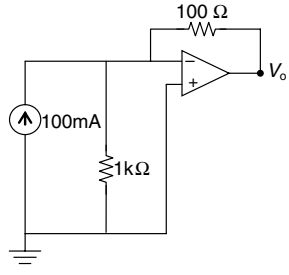
= Voltage across 100 kΩ

$RC = 0.01 \times 10^{-6} \times 10^3$

$t = 2.57\ \mu\text{S}$

Example 25

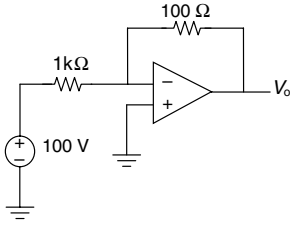
In the circuit shown, the output voltage is



(A) −9 V (B) −10 V (C) +10 V (D) +9 V

Solution

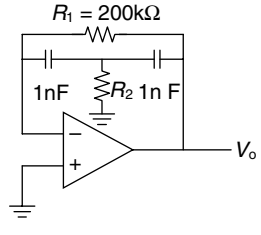
We can observe the current source 100 mA, in parallel with resistance 1 kΩ as



So $V_0 = \frac{-100}{1000} \times 100 = -10\text{V}$

Example 26

In the active filter circuit, if $Q = 1$, a pair of poles will be realized with ω_o, equal to



(A) 1,000 rad/s (B) 100 rad/s
(C) 10 rad/s (D) 1 rad/s

Solution

$$\frac{V_o(s)}{V_i} = \frac{s/R_2C_1}{s^2 + \frac{C_1 + C_2}{R_1\,C_1\,C_2}s + \frac{1}{R_1\,R_2\,C_1\,C_2}}$$

$$A_v(s) = \frac{(\omega_o/Q)\,A_o s}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2}$$

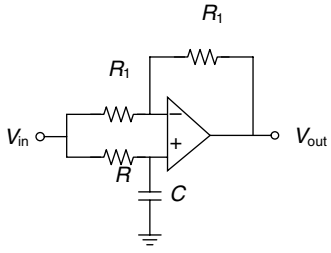
By comparing we have $\frac{\omega_o}{Q} = \frac{C_1 + C_2}{R_1\,C_1\,C_2}$

$$\omega_o = Q\left(\frac{C_1 + C_2}{R_1\,C_1\,C_2}\right) = 1 \times \frac{(1+1) \times 10^{-9}}{200 \times 10^3 \times 10^{-18}}$$

= 1000 rad/s.

Example 27

For the circuit with an ideal op-amp, the maximum phase shift of the output V_{out} with reference to input V_{in} is



(A) $-90°$ (B) $0°$ (C) $+90°$ (D) $\pm 180°$

Solution

$$V_+ = \frac{V_{in}}{1 + j\omega RC}$$

$$V_- = V_+ \text{ (as its ideal op Amp)}$$

$$\frac{V_{in} - V_-}{R_1} = \frac{V_- - V_o}{R_1}$$

$$V_o = 2V_- - V_{in} = 2V_+ - V_{in} =$$

$$\left[\frac{2}{1 + j\omega RC} - 1\right] V_{in} = \frac{1 - j\omega RC}{1 + j\omega RC} \cdot V_{in}$$

$$\angle (V_o/V_i) = -2 \tan^{-1} \omega RC$$

for $-90° \le 0 \le +90°$, phase shift $\angle (V_o/V_i) = \pm 180°$

Power Supplies

The function of voltage regulator is to provide a stable dc voltage for powering other electronic circuits.

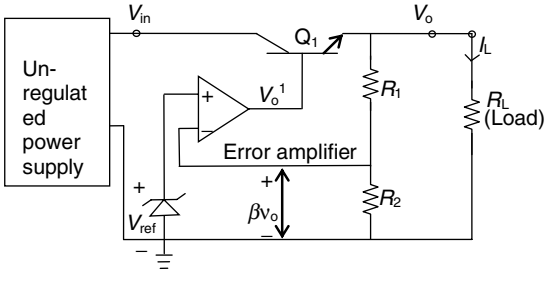


Figure 13 A regulated power supply

The circuit consists of the following four parts:

1. Reference voltage circuit
2. Error amplifier
3. Series pass transistor(Q_1)
4. Feedback network.

The power transistor Q_1 is in series with the unregulated dc voltage V_{in} and regulated output V_0. So it absorbs the difference between these two voltages, for fluctuations in voltages. Q_1, is connected as emitter follower, and it provides sufficient current gain to drive load. The output voltage is sampled by $R_1 - R_2$ divider and feedback to the (–) input terminal, of the error amplifier, The sampled voltage is compared with the reference voltage V_{ref} (obtained by a zener diode). The output of error amplifier drives the Q_1 transistor.

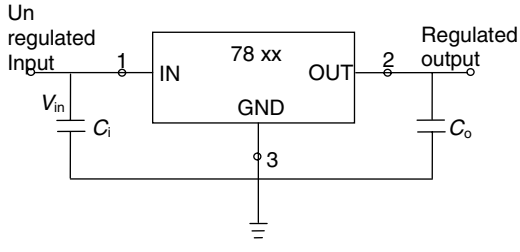
$$\beta = \frac{R_2}{R_1 + R_2}$$

This in turn, reduces the output voltage V_0, of the diff amp ($v_0^1 = \beta v_0$), so V_0 follows v_0^1, so V_0 also reduces. Hence, an increase in V_0 is nullified, and reduction in output voltage also regulated.

IC Voltage Regulators

78xx series are three terminal, positive-fixed voltage regulator available in 05, 06, 08, 12, 15, 18, and 24V.

The last (XX) two numbers indicate o/p voltages.



The three terminal regulators have the following limitations:

1. No short circuit protection.
2. Output voltage (positive or negative) is fixed.

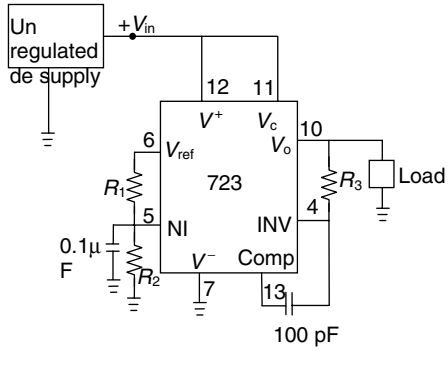
These limitations have been overcome in 723 general-purpose regulator.

Advantages

Adjustable to wide range of both positive and negative voltages. It can be boosted to provide 5 A or more current.

Limitations

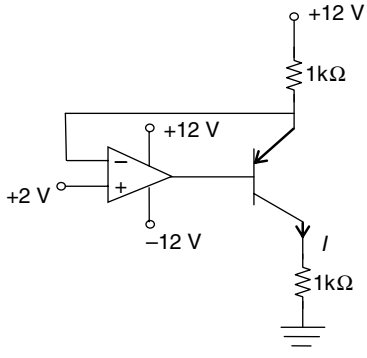
No built-in thermal protection.
No short circuit current limits.



$$V_0 = V_{ref} \frac{R_2}{R_1 + R_2}$$

Example 28

An op-amp circuit is shown in the figure, the current '*I*' is



(A) 0 (B) 5 mA (C) 10 mA (D) 12 mA

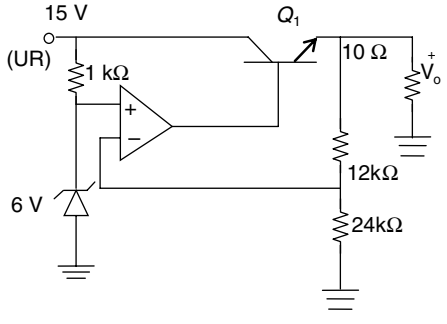
Solution

The current through emitter $I_E = \frac{(12-2)\text{V}}{1\text{k}\Omega} = 10\text{mA}$

The current through collector = $I_C \approx I_E \approx 10$ mA

Example 29

A regulated power supply, shown in figure below, has an unregulated input (UR) of 15 V and generates a regulated o/p V_{out}. Use the component values shown, the power dissipation across the transistor Q_1 in the figure is



(A) 4.8 W (B) 5.0 W (C) 5.4 W (D) 6.0 W

Solution

The zener is in break down region

$$V_+ = V_Z = +6\text{ V} = V_{in}$$

$$V_o = V_{in}\left(1+\frac{RF}{R_1}\right)$$

$$V_{out} = V_o = 6\left(1+\frac{12\,k}{24\,k}\right) = 9\text{ V}.$$

The current in 10 Ω resistor is very high when compared with current in 12 kΩ + 24 kΩ resistor, so it is negligible

$$I_C \approx I_E \approx \frac{V_{out}}{R_L} = \frac{9}{10} = 0.9\text{ A}$$

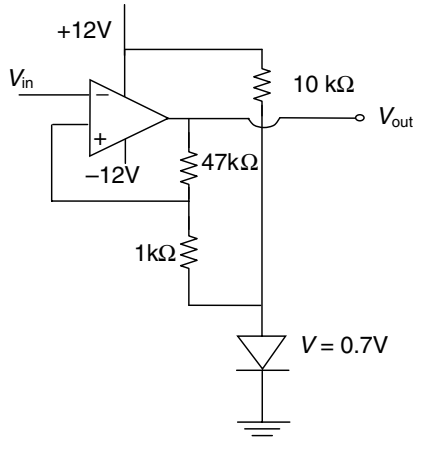
$$V_{CE} = 15 - 9 = 6\text{ V}$$

The power dissipated in transistor is P

$$= V_{CE} \times I_C = 6 \times 0.9 = 5.4\text{ W}$$

Example 30

The Schmitt trigger circuit is shown in the circuit if $\pm V_{sat}$ = ± 10 V, the tripping point for the increasing input voltage will be?



(A) 1 V (B) 0.893 V
(C) 0.477 V (D) 0.416 V

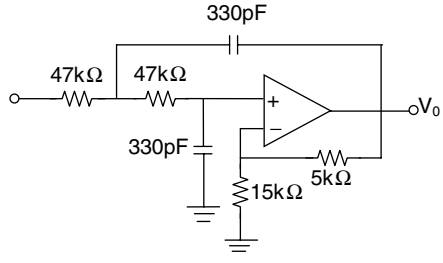
Solution

$$\text{Tripping point} = \frac{R_1}{R_1+R_2}V_R + \frac{R_2}{R_1+R_2}.V_0$$

$$= \frac{1}{48}\times 10.7 + \frac{47}{48}\times 0.7 = 0.893\text{ V}$$

Example 31

The pole frequency and Q of the filter shown in figure is



(A) 0.6, 10.3 kHz (B) 0.5, 10.3 kHz
(C) 0.5, 5.15 kHz (D) 0.6, 5.15 kHz

Solution

$$A_v = \frac{5}{15} + 1 = 1.33$$

$$Q = \frac{1}{3-A_v} = \frac{1}{3-1.33} = 0.6 \text{ (Same for LPF \& HPF)}$$

$$f_P = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} = \frac{1}{2\pi RC} = 10.3\text{ kHz for butterworth filter.}$$

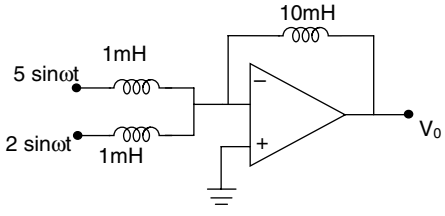
Pole frequency is same as cut off.

EXERCISES

Practice Problems I

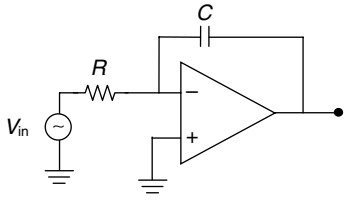
Direction for questions 1 to 41: Select the correct alternative from the given choices.

1. Calculate the output V_o of the figure given.



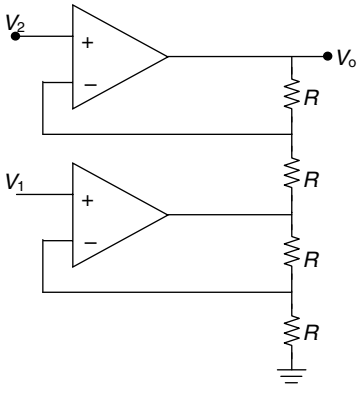
(A) 7 sinω*t* Volt (B) 3 sinω Volt
(C) −70 sinω*t* Volt (D) −10 sinω*t* Volt

2. An op-amp integrator with $R = 10\ M\Omega$ and $C = 0.1\ \mu F$ is shown below. An input of $4\sin 100t$ V is applied. Calculate the time in which output V_o reach 20 mV.



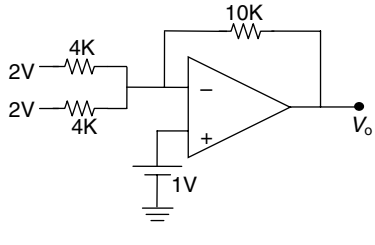
(A) 1.047sec (B) 10.47sec
(C) 10.47μsec (D) 10.47msec

3. What is the output V_0 of the figure given below.



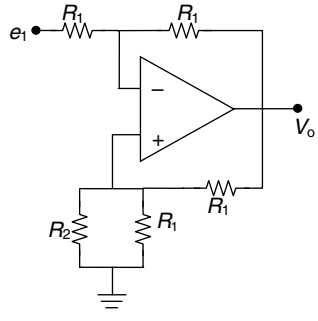
(A) $V_1 - V_2$ (B) $V_1 + V_2$
(C) $2(V_1 - V_2)$ (D) $2(V_2 - V_1)$

4. What is the output V_o of the figure given.



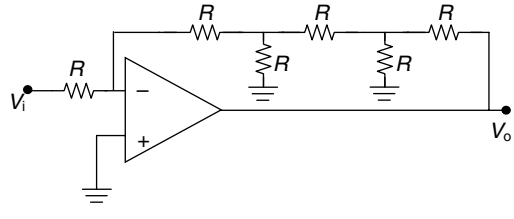
(A) 10 V (B) −6 V (C) −4 V (D) −10 V

5. What is the current in R_2. Given $R_1 = 1\ k\Omega$, $R_2 = 2\ k\Omega$ and $e_1 = 1$volt



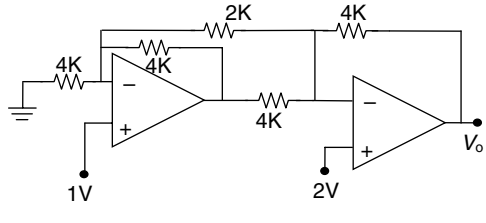
(A) −0.5 mA (B) −1 mA (C) −2 mA (D) None

6. Calculate $\frac{V_0}{V_i}$ of the figure given



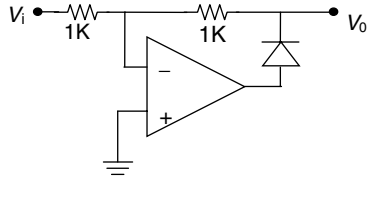
(A) 4 (B) −8 (C) −4 (D) None

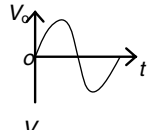
7. What is the output V_o?

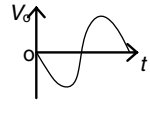


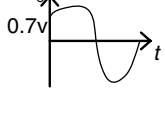
(A) 2 V (B) 4V (C) 6V (D) 0 V

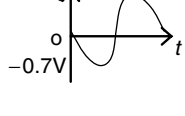
8. What is the output wave form for the input sinusoidal for the circuit given. Assume the forward voltage drop of diode is 0.7 V



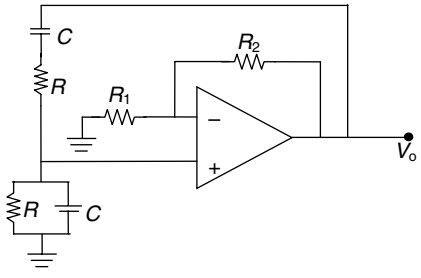
(A) 

(B) 

(C) 

(D) 

9. A Wien bridge oscillator is shown below with $R = 2\ k\Omega$, $C = 0.16\ \mu F$.



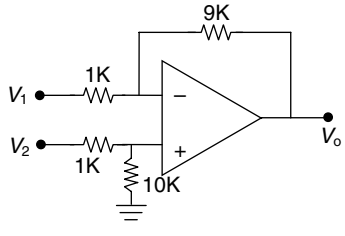
If $R_1 = 0.5\ k\Omega$, the value of R_2 to sustained oscillations is

(A) 0.5 kΩ (B) 1 kΩ
(C) 2 kΩ (D) 1.5 kΩ

10. The frequency of o/p is

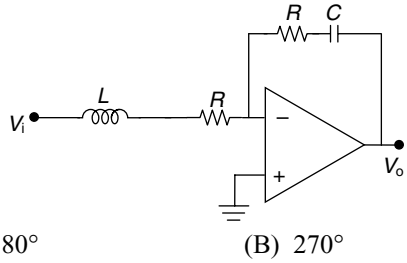
(A) 50 Hz (B) 1 kHz
(C) 5 kHz (D) 500 Hz

11. The CMRR of the figure given is



(A) 900 (B) 9
(C) 90 (D) Infinite

12. Given op-amp is ideal $R = \dfrac{\sqrt{L}}{C}$. What is the phase angle between V_o and V_i at $\omega = \dfrac{1}{\sqrt{LC}}$?

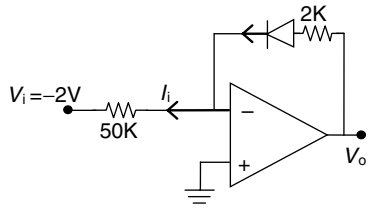


(A) 180° (B) 270°
(C) 0° (D) 90°

13. The op-amp shown is ideal. The V–I characteristic of diode is given by

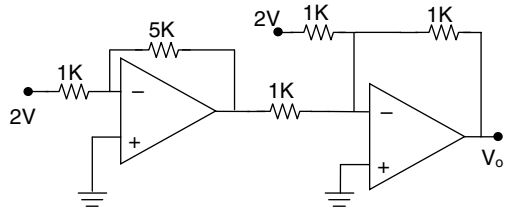
$$I = I_0\left[e^{V_d/\eta V_T} - 1\right]$$ where

$V_T = 26$ mV, $I_o = 10\ \mu A$, and V_d = voltage across diode. The output V_0 for $V_i = -2$ V is _____



(A) 0.122 V (B) 0.6 V (C) 1.2 V (D) None

14. What is the output V_o of the figure given.



(A) 8 V (B) −8 V (C) 10 V (D) −10 V

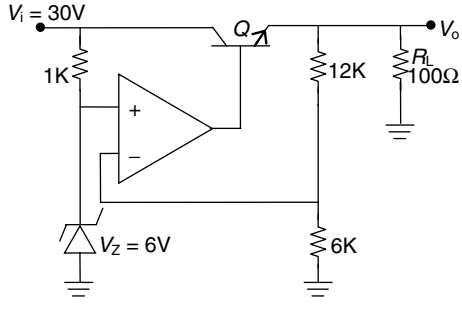
15. An op-amp has open loop gain 'A' of 2×10^3, the input impedance Z_i = 100 kΩ and output impedance Z_o = 2 kΩ. The op-amp is used in non-inverting mode with closed loop gain 100. The effective input and output impedances are _____

(A) $Z_{if} = 2.1\ m\Omega$, $Z_{of} = 42\ k\Omega$
(B) $Z_{if} = 4.8\ k\Omega$, $Z_{of} = 95\ \Omega$
(C) $Z_{if} = 2.1\ m\Omega$, $Z_{of} = 95\ \Omega$
(D) $Z_{if} = 4.8\ k\Omega$, $Z_{of} = 42\ k\Omega$

16. A differential amplifier has a typical common mode gain 30db and CMRR of 70dB. What is the output voltage V_o when Input voltages are 0.14 mV and 0.16 mV

(A) 2.047 V (B) 1.99 V (C) 4.74 V (D) 4.4 V

17. An op-amp voltage regulator is given below:



The regulated output V_o is

(A) 10 V (B) 20 V (C) 9 V (D) 18 V

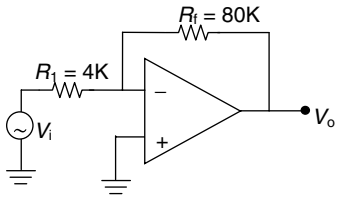
18. The power dissipation by transistor is

(A) 1.08 W (B) 2.16 W (C) 4 W (D) 3.2 W

19. For a non-inverting amplifier $R_1 = 20\ k\Omega$, $R_f = 100\ k\Omega$, is used. A peak-to-peak voltage of 2 V is applied at I/P. Given slew rate = 0.5 V/μsec, what is maximum operating frequency?

(A) 6.66 kHz (B) 13.33 kHz
(C) 16 kHz (D) 8 kHz

20. An op-amp circuit given below:



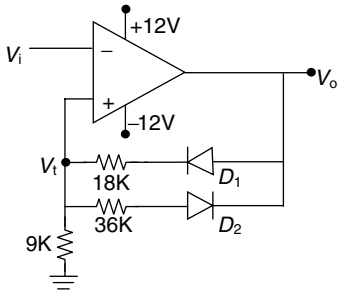
The feedback implemented is

(A) voltage series (B) voltage shunt
(C) current series (D) current shunt

21. Feedback ratio β is

(A) 95.2% (B) 5.2%
(C) 5% (D) 4.7%

22. Consider diodes and op-amp are ideal, calculate UTP and LTP.



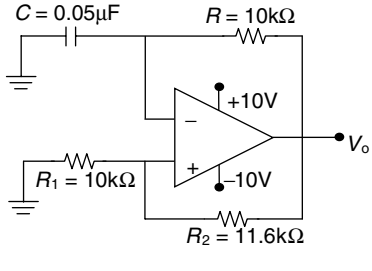
(A) $V_{UTP} = 8$ V $V_{LTP} = -8$ V
(B) $V_{UTP} = 9.6$ V $V_{LTP} = -9.6$ V
(C) $V_{UTP} = 4$ V $V_{LTP} = -2.4$ V
(D) $V_{UTP} = -4$ V $V_{LTP} = 2.4$ V

23. An op-amp has unity gain frequency of 400 MHz with band width of 60 kHz. Calculate gain in dB

(A) 56.5dB (B) 20dB
(C) 76.48dB (D) None

Direction for questions 24 and 25:

A square wave generator (astable) using op-amp is shown below.



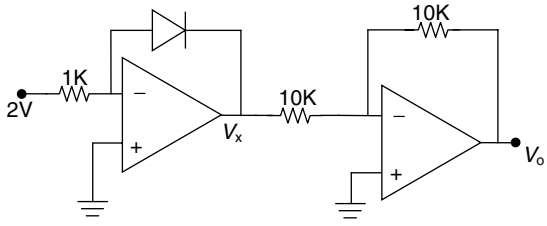
24. The frequency of the square wave output is

(A) 500 Hz (B) 2.5 kHz
(C) 1 kHz (D) None

25. The feedback ratio β of the circuit is

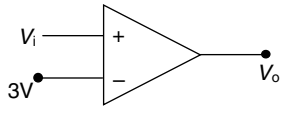
(A) 0.463 (B) 1
(C) 0.72 (D) 0.537

26. Calculate the o/p V_o of the figure given. Given V_T = 25 mV



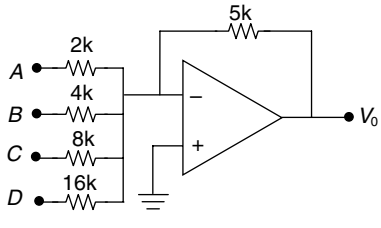
(A) −17.3 mV (B) 17.3 mV
(C) 0.69 mV (D) −0.69 mV

27. A comparator is shown below. A sinusoidal input of peak value 6 V is applied. The length (in degrees) for which the output high is



(A) 180° (B) 60° (C) 120° (D) 150°

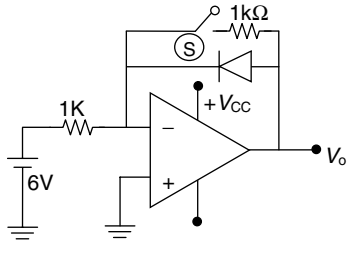
28. Calculate the output voltage of the figure given below if the digital input 0101 =.



Digital I/p is 0 V (or) +5 V for 0 (or) 1, respectively

(A) −7.81 V (B) −4.87 V
(C) −5.87 V (D) −3.87 V

29. Consider the op-amp and diode are ideal



What is the output V_o when switch 'S' is open?

(A) 0.7 V (B) $+V_{cc}$
(C) 0 V (D) $-V_{EE}$

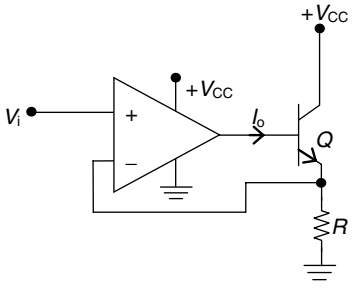
30. What is the output V_o when switch S is closed?

(A) −60 V (B) 0 V (C) −6 V (D) $-V_{EE}$

31. In an inverting op-amp, the input bias current is −2 μA. The input and feedback resistance are both 50 kΩ. Calculate the output voltage for input voltage of 1.5 V.

(A) −1.6 V (B) −2 V
(C) −1.5 V (D) −3 V

32. Assume that $V_i = 3$ V, $R = 20\ \Omega$, β of a transistor is 80, $V_{CC} = 12$ v. Calculate I_o,



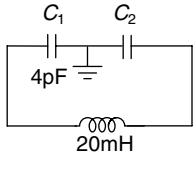
(A) 3.8 mA (B) 1.8 mA (C) 0.15 A (D) 4 mA

33. The feedback network of Hartley oscillator have $L_1 = 10$ mH, $L_2 = 5$ mH, and $C = 100$PF. The mutual inductance between L_1 and L_2 is 2.5 mH. The frequency of oscillation is _____.

(A) 0.13 MHz (B) 11.3 kHz
(C) 0.113 MHz (D) None

Direction for questions 34 and 35:

The feedback network used in Colpitts oscillator is given below.



34. The value of C_2 to have frequency of oscillation 1 MHz is _____.

(A) 0.8PF (B) 4PF (C) 1.8PF (D) 2.2PF

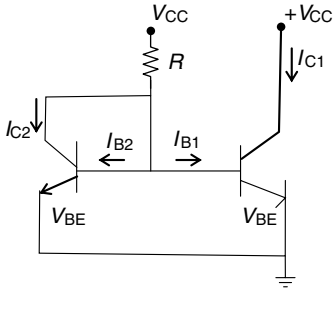
35. Feedback ratio β is _____.

(A) 0.45 (B) 0.2 (C) 0.9 (D) None

36. The RC network of wien bridge oscillator has $R_1 = R_2 = 80$ kΩ, let us assume $C_1 = C_2 = C$ then what is the value of C required for the frequency of oscillation 5 kHz?

(A) 200 pF (B) 400 pF (C) 50 pF (D) 1 pF

37. The current mirror in the figure is designed to provide $I_C = 0.5$ mA, $V_{CC} = 10$ V, $\beta = 100$, $V_{BE} = 0.7$ V. The value of R is



(A) 18.23 kΩ (B) 8.5 kΩ
(C) 12.9 kΩ (D) 15.3 kΩ

38. If V_{BE} changes by -2.2m V/°C what is the permissible temperature range if I_{C1} is to remain within 1% of its normal design value of the above problem?

(A) 21°C (B) 42°C
(C) 93°C (D) 12°C

39. Match List-I and List-II.

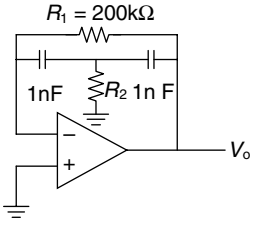
	List-I		List-II
P.	Wien bridge oscillator	**1.**	Low-output Impedance
Q.	Voltage shunt feedback amplifier	**2.**	RF frequency range
R.	Crystal oscillator	**3.**	Audio frequency range
S.	Current shunt feedback amplifier	**4.**	High-input impedance
		5.	High-output impedance

	P	Q	R	S
(A)	2	1	3	5
(B)	5	4	2	1
(C)	3	4	2	1
(D)	3	1	2	5

40. The slew rate of an op-Amp is 0.5 V/micro seconds. The maximum frequency of a sinusoidal input of $2V_{(rms)}$ that can be handled without excessive distortion is

(A) 3 kHz (B) 30 kHz
(C) 200 kHz (D) 2 MHz

41. In the Active filter circuit, if $Q = 2$, a pair of poles will be realized with ω_o, equal to



(A) 2000 rad/s (B) 200 rad/s
(C) 20 rad/s (D) 2 rad/s

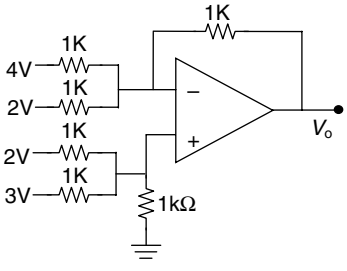
Practice Problems 2

Direction for questions 1 to 39: Select the correct alternative from the given choices.

1. An op-amp has a open loop gain 60dB and common mode gain is 1.2. Calculate CMRR in dB

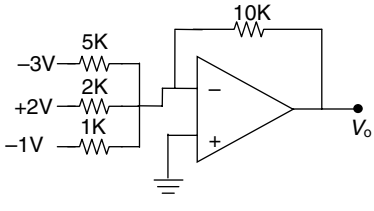
(A) 50dB (B) 58.42dB
(C) 72dB (D) 58.8dB

2. What is the output V_o of the figure given



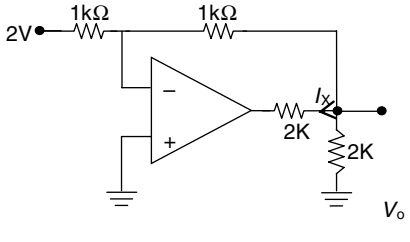
(A) −1 V (B) +1 V (C) 0 V (D) 2 V

3. What is the output V_o of the figure given



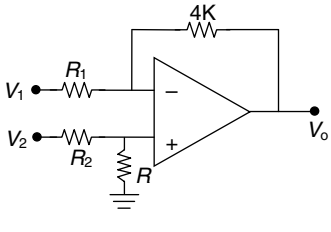
(A) 0 V (B) 6 V (C) −6 V (D) −14 V

4. What is the current I_x of the figure given



(A) 3 mA (B) 2 mA (C) 1.5 mA (D) 0

5. What is the value of R as if the magnitude of gains in inverting and non-inverting modes are equal. ($R_1 = R_2$)



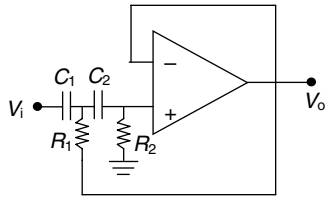
(A) 4 kΩ (B) 2 kΩ (C) 1 kΩ (D) 8 kΩ

6. What is the cut-off frequency of the figure given.

$C_1 = C_2 = 0.08\mu F$

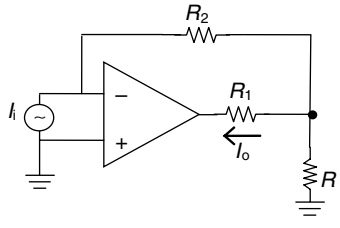
$R_1 = 7.07\ k\Omega$

$R_2 = 14.14\ k\Omega$



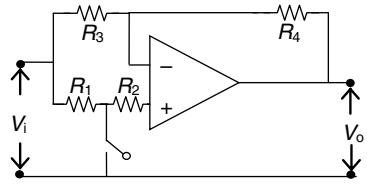
(A) 2 kHz (B) 20 kHz (C) 0.2 kHz (D) None

7. In the circuit given below, I_o/I_i is



(A) $1+\frac{R_2}{R}$ (B) $1+\frac{R_1}{R}$ (C) $\frac{R_2}{R}$ (D) $\frac{R_1}{R}$

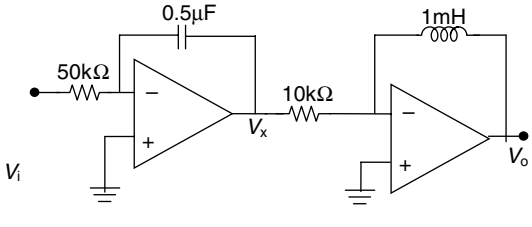
8. What is the ratio of gain of the circuit given below when switch open to switch close condition?



(A) $-R_3 / R_4$ (B) $R_1 + \frac{R_3}{R_4}$

(C) $-R_4 / R_3$ (D) $R_2 + \frac{R_4}{R_3}$

9. Calculate the output V_o of the figure given.



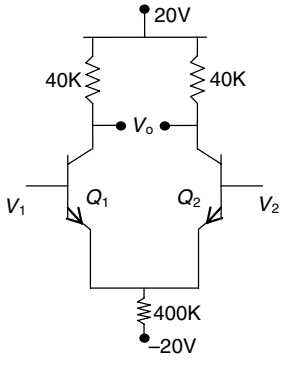
Where $V_i = 10\cos 100t$ Volt

(A) $0.04\cos 100t$ mV (B) $0.2\sin 100t$ V
(C) $-4\cos 100t$ mV (D) $-4\sin 100t$ V

Direction for questions 10 to 12:

A differential amplifier is given has following specifications

$$r_\pi = 2\ m\Omega,\ \beta = 4 \times 10^3$$

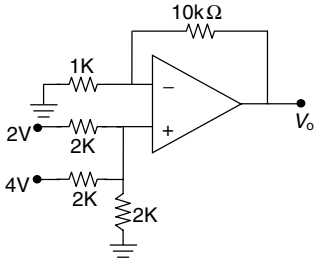


10. The differential mode gain is
(A) 100 (B) 80 (C) 90 (D) 50

11. Common mode gain is
(A) 0.125 (B) 0.05 (C) 1 (D) 0

12. CMRR in dB is
(A) 64.08dB (B) 21.8dB (C) 41.3dB (D) None

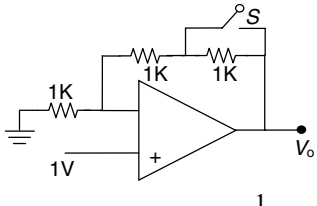
13. What is the output V_o of the figure given



(A) 11 V (B) 33 V (C) 22 V (D) 5.5 V

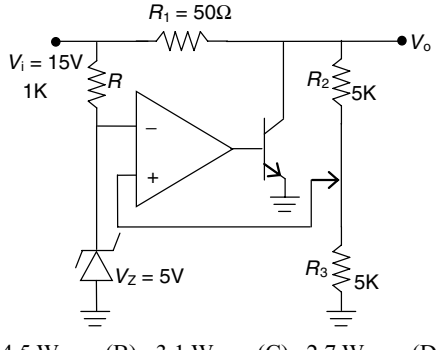
14. The CMRR of a differential amplifier is 60dB. If the differential mode gain is 1,400, what is the common mode gain A_C?
(A) 1.4 (B) 2.1 (C) 0.8 (D) None

15. An op-amp shown below give output is x when the switch S is open. What is the output when switch S is closed.



(A) x (B) 2x (C) $\frac{1}{2}x$ (D) $\frac{2}{3}x$

16. Calculate the power rating of R_1 if the maximum input voltage is 15 V.



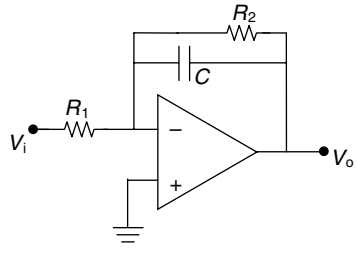
(A) 4.5 W (B) 3.1 W (C) 2.7 W (D) None

17. The change in the op-amp input off set voltage V_{io} caused by variation in supply voltage is 60 μv. Calculate the change in supply voltage. Given
SVRR = 104dB
(A) 0 V (B) 9.5 V (C) 2 V (D) None

18. For non-inverting amplifier how much is the feedback resistance required to produce an output of 10 V for input of 1.5 V. Given input resistance is 2.5 kΩ.
(A) 2.26 kΩ (B) 0.37 kΩ
(C) 14.2 kΩ (D) 0.37 kΩ

19. An amplifier using op-amp with a slew rate 0.5V/μsec has a gain 20dB. If this amplifier has to faithfully amplify sinusoidal signals from dc to 30 kHz without any distortion, what is the limit of the input signal level?
(A) 266 mV (B) 2.6 V (C) 26.6 mV (D) None

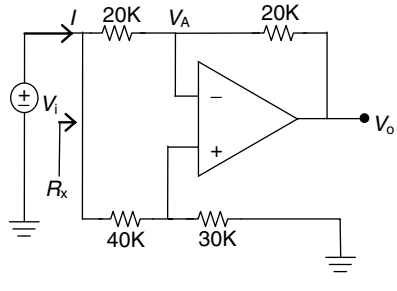
20. Recognize the type of filter shown below:



(A) low-pass filter (B) high-pass filter
(C) band-pass filter (D) None

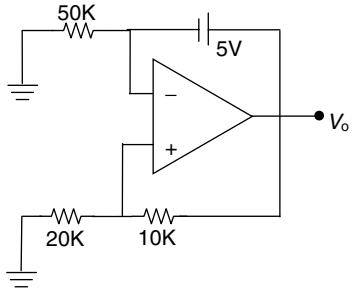
21. If R_1 = 10 kΩ, R_2 = 1 kΩ and C = 0.01 μf, the cut-off frequency f_o is_____
(A) 1.6 kHz (B) 1.45 kHz
(C) 160 Hz (D) None

22. Calculate R_x of the figure given



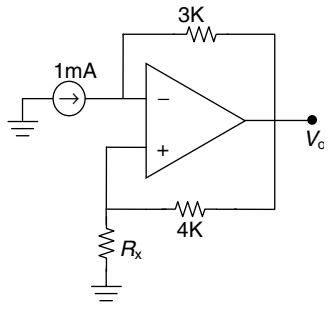
(A) 20 kΩ (B) 60 kΩ
(C) 23.3 kΩ (D) $\frac{40\text{k}\Omega}{3}$

23. Calculate V_o of the given circuit



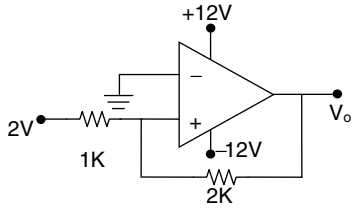
(A) 15 V (B) 0 V (C) –5 V (D) 5 V

24. What is the value of R_x to get $V_o = -4.5$ V



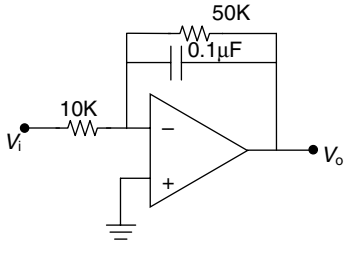
(A) 2 kΩ (B) 1 kΩ (C) 1.5 kΩ (D) 4 kΩ

25. What is the output V_o of the figure given



(A) +12 V (B) ±12 V (C) –12 V (D) 6 V

26. What is the very low-frequency gain of low-pass filter shown in the figure given below.

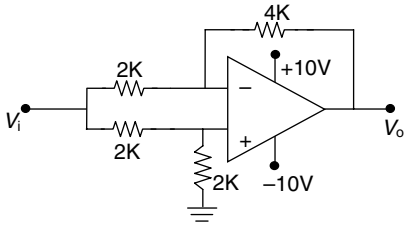


(A) ∞ (B) 6 (C) 5 (D) 0

27. An op-amp based non-inverting amplifier has a gain of 20 and bandwidth of 200 kHz. If the gain of the amplifier is reduced to unity, the band width will changes to _____

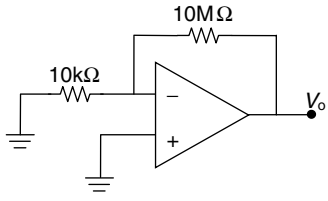
(A) 200 kHz (B) 4 MHz
(C) 1 MHz (D) 10 MHz

28. In the op-amp circuit shown, the voltage ratio V_o/V_i is



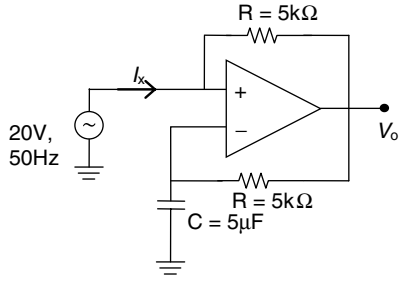
(A) –0.5 (B) –1 (C) 0.5 (D) 4

29. An op-amp has offset voltage of 1.2 mV and is ideal in all other respects. If this op-amp is used in the circuit shown in the figure what is the output voltage



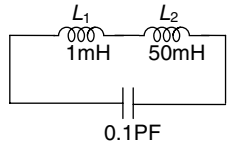
(A) 1.2 mV (B) ±1.2 V (C) 0.6 V (D) 0 V

30. In the figure given calculate I_x from the source



(A) 31.4 mA lead by 90°
(B) 31.4 mA lag by 90°
(C) 62.8 mA lead by 90°
(D) 62.8 mA lag by 90°

31. The feedback network of Hartley oscillator is shown below. The minimum gain of a transistor required for oscillation is _____.

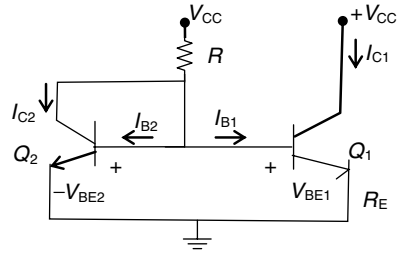


(A) 0.02 (B) 1 (C) 50 (D) None

32. The resonant circuit oscillator has a frequency of 5 MHz. If the capacitance is increased by 50%, the new frequency of oscillation is _____

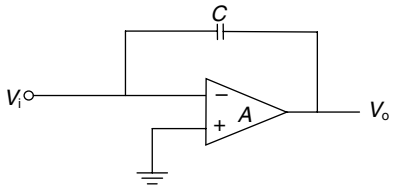
(A) 5 MHz (B) 10 MHz
(C) 2.5 MHz (D) 4.08 MHz

33. For low collector current I_{C1} = 50 μA, this circuit is used. Determine the value of R_E, given I_{C2} = 0.5 mA, β = 100, V_T = 25 mV.



(A) 1.139 kΩ
(B) 4.34 kΩ
(C) 7.57 kΩ
(D) Its not possible to calculate

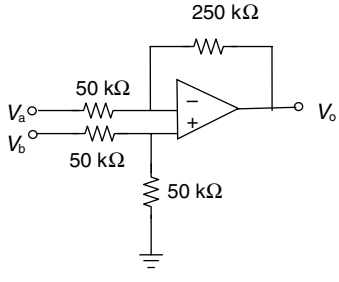
34. An amplifier of gain A is bridged by a capacitor C as shown. The effective input capacitance is



(A) $\frac{C}{A}$ (B) C (1 – A)

(C) C (1 + A) (D) C A

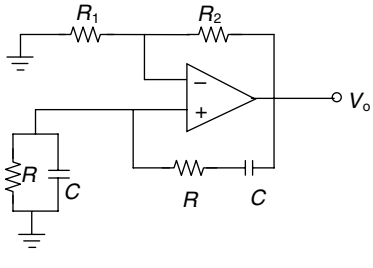
35. What is the output voltage V_o of the given circuit?



(A) $-5V_a + 2.5\ V_b$ (B) $-5\ V_a + 3\ V_b$

(C) $-2.5\ V_a + 2.5\ V_b$ (D) $-2.5\ V_a + 5\ V_b$

36. Consider the following statements for the circuit shown in figure?



(1) For $R = 1$ kΩ, $C = \left(\frac{1}{2\pi}\right)$ μ F, $f = 1$ kHz

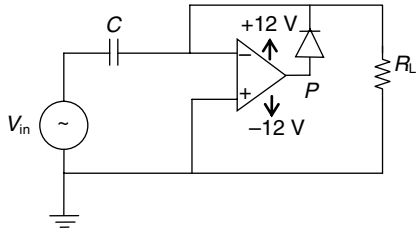
(2) for $R = 3$ kΩ, $C = \left(\frac{1}{18\pi}\right)$ μ F, $f = 3$ kHz

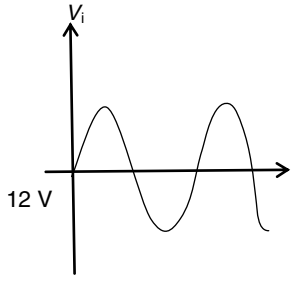
Which of the statements given are true?

(A) (1) only (B) (2) only

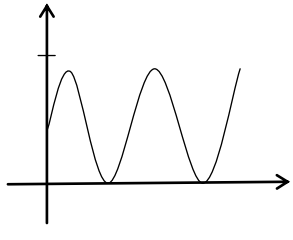
(C) both (D) Neither

37. For the given sinusoidal input voltage, the voltage waveform at point P of the clamper circuit shown in figure is.

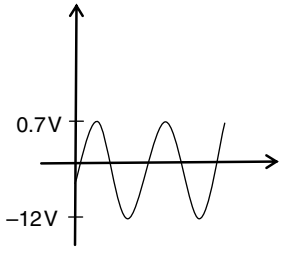




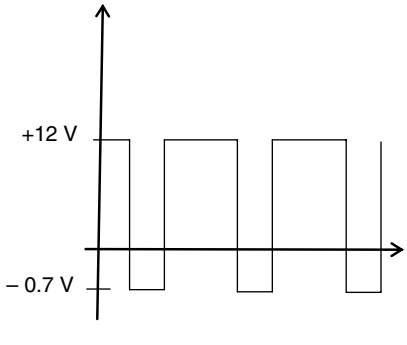
(A)



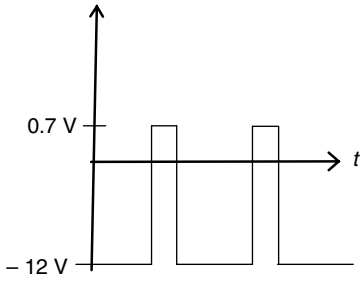
(B)



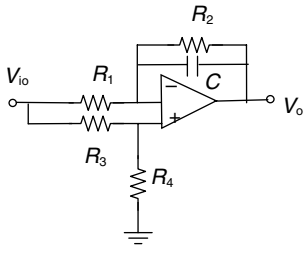
(C)



(D)

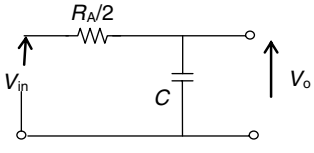


38. A general filter circuit is shown in the figure if $R_1 = R_2 = R_A$, and $R_3 = R_4 = R_B$, then the circuit acts as

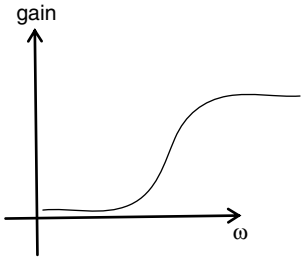


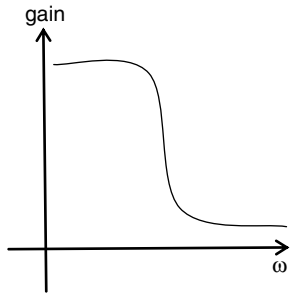
(A) All pass filter (B) Band-pass filter
(C) High-pass filter (D) Low-pass filter

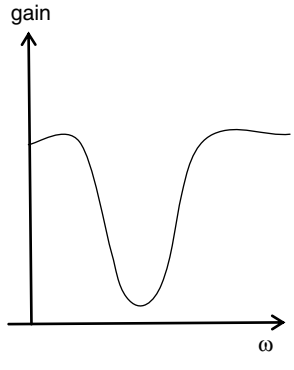
39. The output of the above filter is given to input of the circuit shown in this figure.

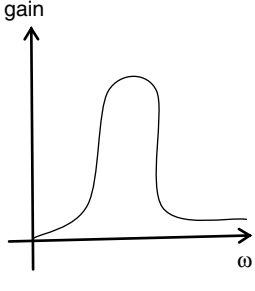


The gain *V*s frequency characteristic of the output V_o will be

(A)


(B)


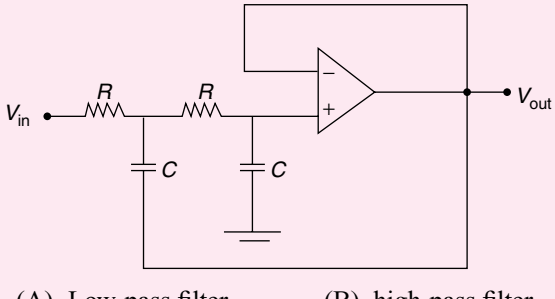
(C)


(D)


Previous Years' Questions

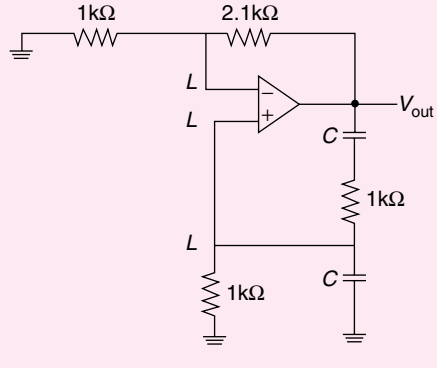
1. An ideal op-amp is an ideal **[2004]**
(A) Voltage-controlled current source
(B) Voltage-controlled voltage source
(C) Current-controlled current source
(D) Current-controlled voltage source

2. The Circuit in Figure is a **[2004]**



(A) Low-pass filter (B) high-pass filter
(C) band-pass filter (D) band-reject filter

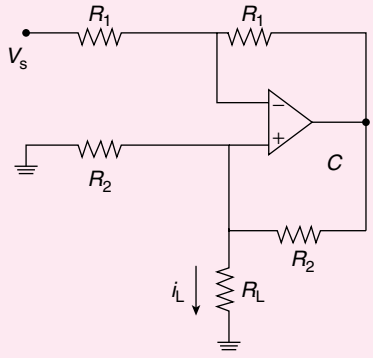
3. The value of *C* required for sinusoidal oscillations of frequency 1 kHz in the following circuit is **[2004]**



(A) $\frac{1}{2\pi}\mu F$ (B) $2\pi\,\mu F$

(C) $\frac{1}{2\pi\sqrt{6}}\mu F$ (D) $2\pi\sqrt{6}\,\mu F$

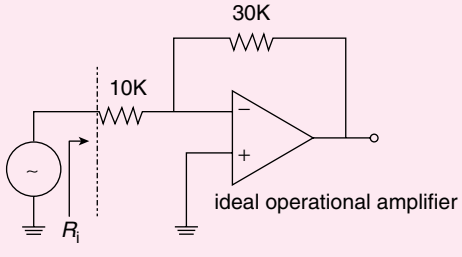
4. In the following op-amp circuit, the load current I_L is **[2004]**



(A) $-\frac{V_S}{R_2}$ (B) $\frac{V_S}{R_2}$

(C) $-\frac{V_S}{R_L}$ (D) $\frac{V_S}{R_L}$

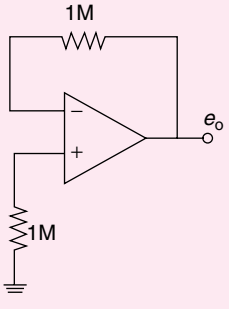
5. The input resistance R_i of the amplifier shown in figure is **[2005]**



(A) $\frac{30}{1}$ kΩ (B) 10 kΩ

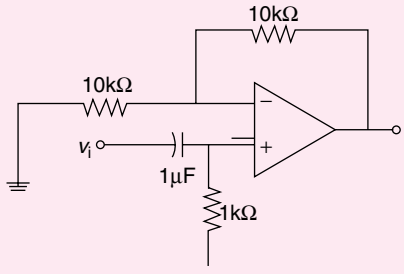
(C) 40 kΩ (D) Infinite

6. The voltage e_0 indicated in figure has been measured by an ideal voltmeter. Which of the following can be calculated? **[2005]**



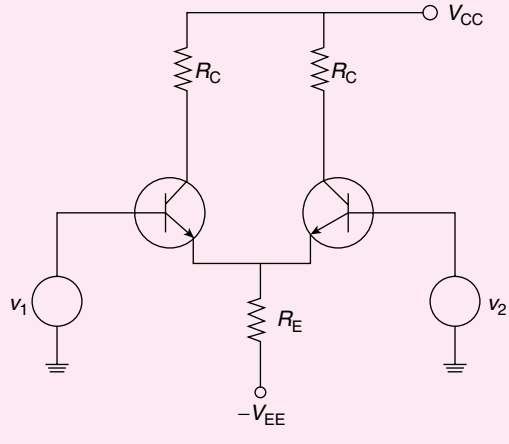
(A) Bias current of the inverting input only
(B) Bias current of the inverting and non-inverting inputs only
(C) Input offset current only
(D) Both bias currents and input offset current

7. The op-amp circuit shown in figure is a filter. The type of filter and its cut-off frequency are respectively. **[2005]**



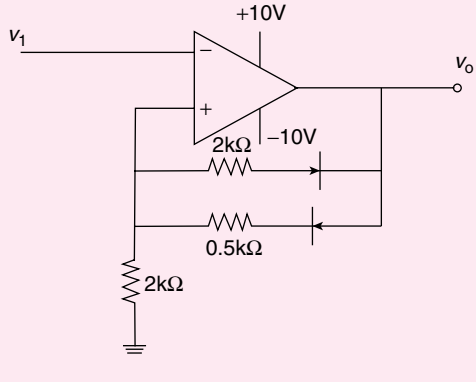
(A) high pass, 1,000 rad/sec
(B) low pass, 1,000 rad/sec
(C) high pass, 10,000 rad/sec
(D) low pass, 10,000 rad/sec

8. In an ideal differential amplifier shown in figure, a large value of R_E **[2005]**

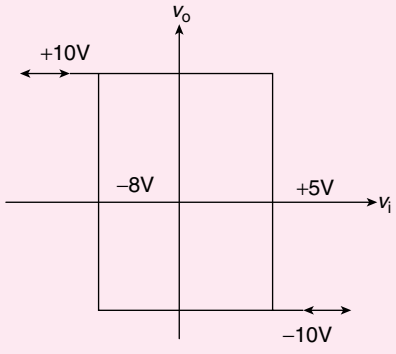


(A) increases both differential and common - mode gains.
(B) increases the common-mode gain only.
(C) decreases the differential-mode gain only.
(D) decreases the common-mode gain only.

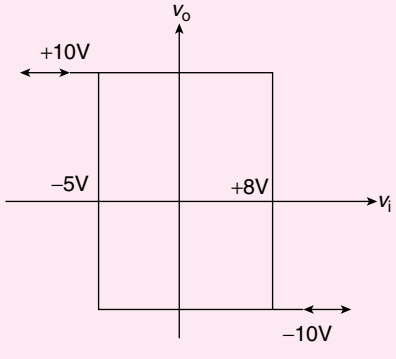
9. Given the ideal operational amplifier circuit shown in figure indicate the correct transfer characteristic ideal diodes with zero cut-in voltage. **[2005]**



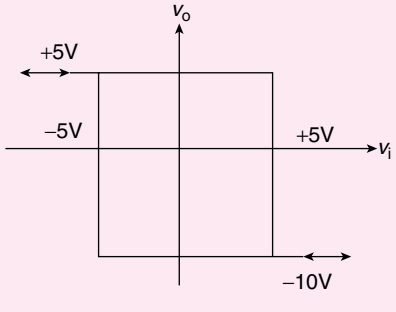
(A)



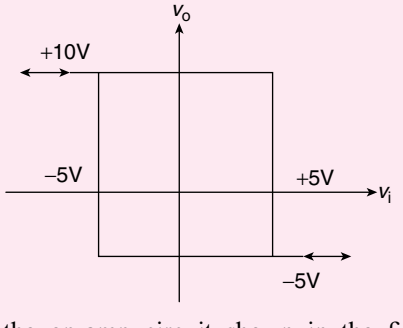
(B)



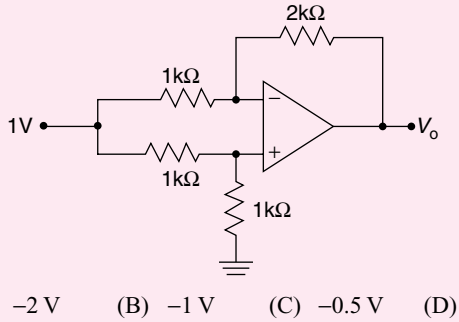
(C)



(D)

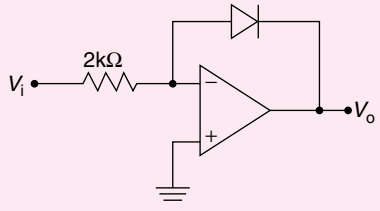


10. For the op-amp circuit shown in the figure V_0 is: **[2007]**



(A) −2 V (B) −1 V (C) −0.5 V (D) 0.5 V

11. In the op-amp circuit shown assume that the diode current follows the equation $I = I_S\exp(V/V_T)$. For V_i= 2 V, $V_0 = V_{01}$, and for $V_i = 4$ V, $V_0 = V_{02}$. The relationship between V_{01} and V_{02} is **[2007]**

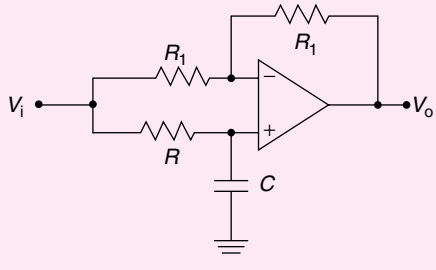


(A) $V_{02} = \sqrt{2}V_{01}$ (B) $V_{02} = e^2V_{01}$

(C) $V_{02} = V_{01}\,\ell n\,2$ (D) $V_{01} - V_{02} = V_T \ln 2$

Direction for questions 12 and 13:

Consider the op-amp circuit shown in the figure.



12. The transfer function $V_0(s)/V_i(s)$ is: **[2007]**

(A) $\dfrac{1-sRC}{1+sRC}$ (B) $\dfrac{1+sRC}{1-sRC}$

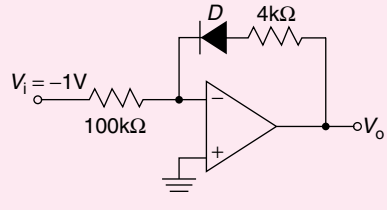
(C) $\dfrac{1}{1-sRC}$ (D) $\dfrac{1}{1+sRC}$

13. If $V_i = V_1\sin(\omega t)$ and $V_0 = V_2\sin(\omega t + \phi)$, then the minimum and maximum values of ϕ (in radians) are respectively. **[2007]**

(A) $\dfrac{-\pi}{2}$ and $\dfrac{\pi}{2}$ (B) 0 and $\dfrac{\pi}{2}$

(C) $-\pi$ and 0 (D) $\dfrac{-\pi}{2}$ and 0

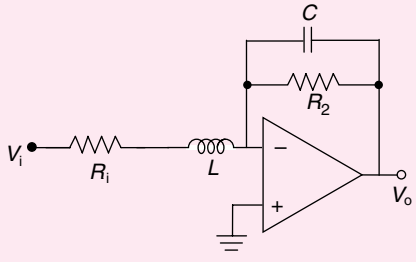
14. Consider the following circuit using an ideal OPAMP. The I-V characteristics of the diode is described by the relation $I = I_0\left(e^{\frac{V}{V_T}} - 1\right)$ where V_T = 25 mV, I_o = I μA and V is the voltage across the diode (taken as positive for forward bias).



For an input voltage $V_1 = -1$ V, the output voltage V_0 is **[2008]**

(A) 0 V (B) 0.1 V
(C) 0.7 V (D) 1.1 V

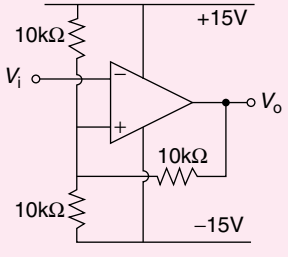
15.



The op-amo circuit shown above represents a **[2008]**

(A) high-pass filter (B) low-pass filter
(C) band-pass filter (D) band-reject filter

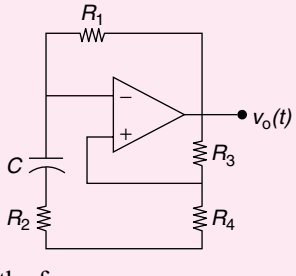
16. Consider the Schmitt trigger circuit shown below.



A triangular wave which goes from −12 V to 12 V is applied to the inverting input of the OPAMP. Assume that the output of the OPAMP swings from +15 V to −15 V. The voltage at the non-inverting input switches between **[2008]**

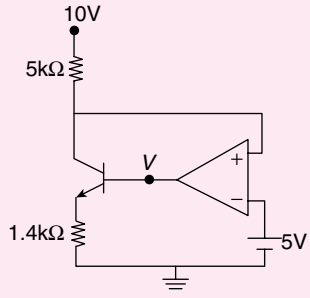
(A) −12 V and +12 V (B) −7.5 V and +7.5 V
(C) −5 V and +5 V (D) 0 V and 5 V

17. In the following stable multivibrator circuit, which properties of $V_0(t)$ depend on R_2? **[2009]**



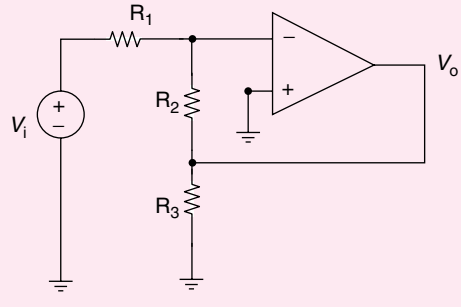
(A) Only the frequency
(B) Only the amplitude
(C) Both the amplitude and the frequency
(D) Neither the amplitude nor the frequency

18. In the circuit shown below, the op-amp is ideal, the transistor has $V_{BE} = 0.6$ V and $\beta = 150$. Decide whether the feedback in the circuit is positive or negative and determine the voltage V at the output of the op-amp. **[2009]**



(A) Positive feedback, $V = 10$ V
(B) Positive feedback, $V = 0$ V
(C) Negative feedback, $V = 5$ V
(D) Negative feedback, $V = 2$ V

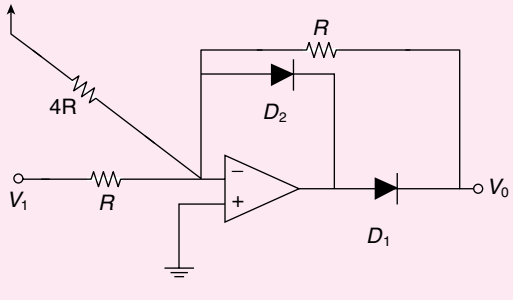
19. Assuming the op-amp to be ideal, the voltage gain of the amplifier shown below is **[2010]**



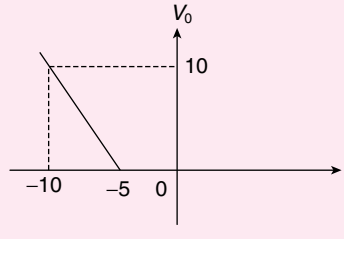
(A) $-\frac{R_2}{R_1}$ (B) $-\frac{R_3}{R_1}$

(C) $-\frac{R_2 \| R_3}{R_1}$ (D) $-\left(\frac{R_2 + R_3}{R_1}\right)$

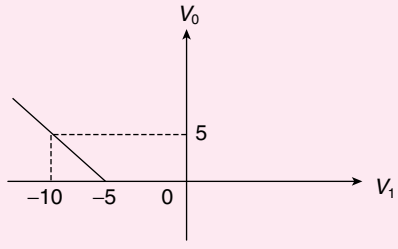
20. The transfer characteristic for the precision rectifier circuit shown below is (assume ideal OP-AMP and practical diodes) **[2010]**



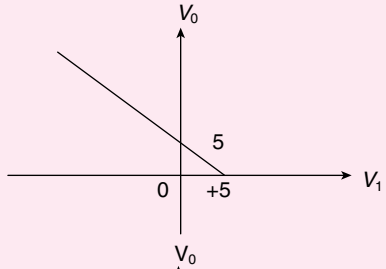
(A)



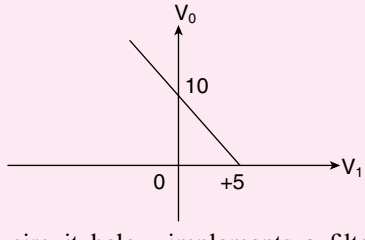
(B)



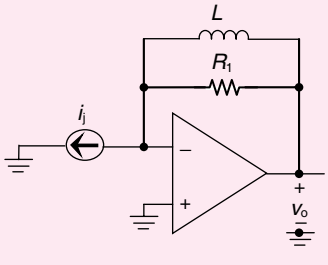
(C)



(D)

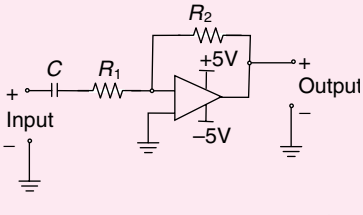


21. The circuit below implements a filter between the input current i_i, and the output voltage v_o. Assume that the op-amp is ideal. The filter implemented is a **[2011]**



(A) low-pass filter (B) band-pass filter
(C) band-stop filter (D) high-pass filter

22. The circuit shown is a **[2012]**



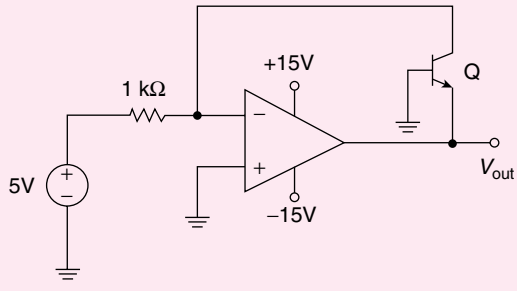
(A) Low-pass filter with $f_{3dB} = \dfrac{1}{(R_1 + R_2)C}$ rad/s

(B) High-pass filter with $f_{3dB} = \dfrac{1}{R_1 C}$ rad/s

(C) Low-pass filter with $f_{3dB} = \dfrac{1}{R_1 C}$ rad/s

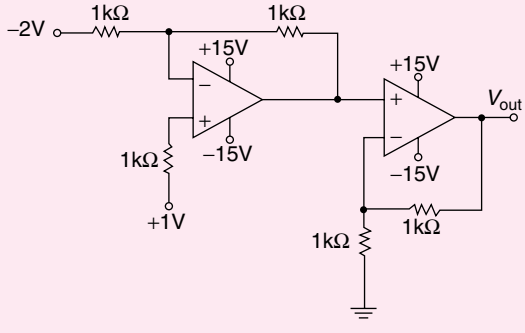
(D) High-pass filter with $f_{3dB} = \dfrac{1}{(R_1 + R_2)C}$ rad/s

23. In the circuit shown below, what is the output voltage (V_{out}) if a silicon transistor Q and an ideal op-amp are used? **[2013]**



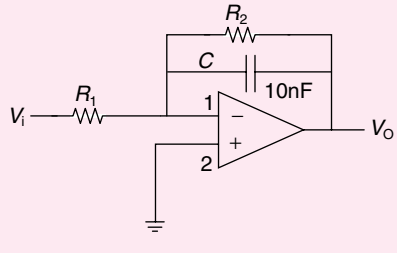
(A) −15 V (B) −0.7 V
(C) +0.7 V (D) +15 V

24. In the circuit shown below, the op-amps are ideal. Then, V_{out} in volts is **[2013]**



(A) 4 (B) 6 (C) 8 (D) 10

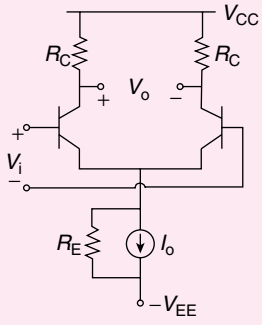
25. In the low-pass filter shown in the figure, for a cut-off frequency of 5 kHz, the value of R_2 (in kΩ) is _____ **[2014]**



26. In the circuit shown, the op-amp has finite input impedance, infinite voltage gain, and zero input offset voltage. The output voltage V_{out} is **[2014]**

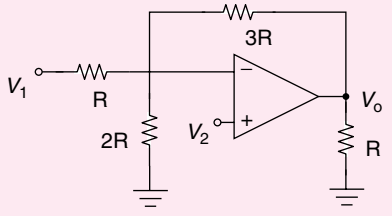
(A) $-I_2(R_1 + R_2)$ (B) $I_2 R_2$
(C) $I_1 R_2$ (D) $-I_1(R_1 + R_2)$

27. In the differential amplifier shown in the figure, the magnitudes of the common-mode and differential-mode gains are A_{cm} and A_d, respectively. If the resistance R_E is increased, then **[2014]**



(A) A_{cm} increases
(B) common-mode rejection ratio increases
(C) A_d increases
(D) common-mode rejection ratio decreases

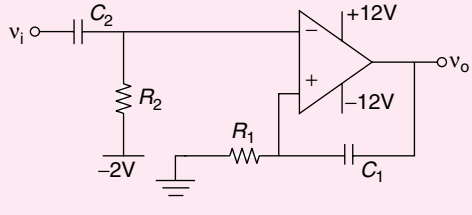
28. Assuming that the op-amp in the circuit shown is ideal, V_o is given by **[2014]**



(A) $\frac{5}{2}V_1 - 3V_2$ (B) $2V_1 - \frac{5}{2}V_2$

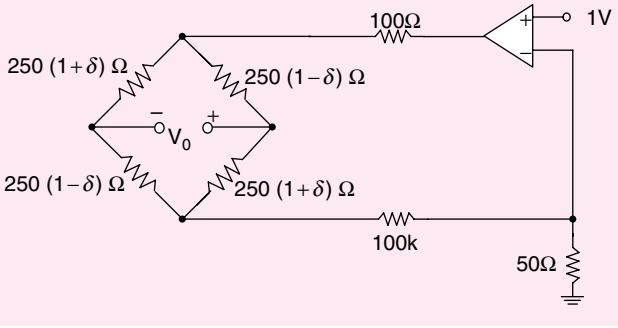
(C) $-\frac{3}{2}V_1 + \frac{7}{2}V_2$ (D) $-\frac{3}{2}V_1 + \frac{11}{2}V_2$

29. The circuit shown represents **[2014]**

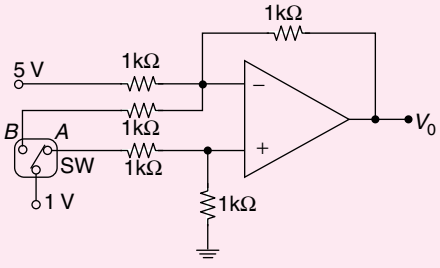


(A) a band-pass filter
(B) a voltage-controlled oscillator
(C) an amplitude modulator
(D) a monostable multivibrator

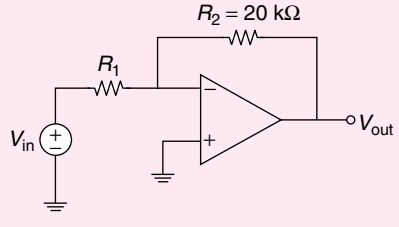
30. In the circuit shown, assume that the opamp is ideal. The bridge output voltage V_0 (in mV) for $\delta = 0.05$ is _____. **[2015]**



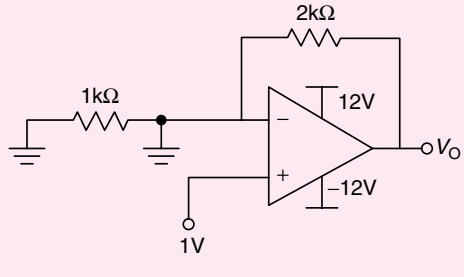
31. In the circuit shown, $V_0 = V_{0A}$ for switch SW in position A and $V_0 = V_{0B}$ for SW in position B. Assume that the opamp is ideal. The value of $\frac{V_{0B}}{V_{0A}}$ is _____. **[2015]**



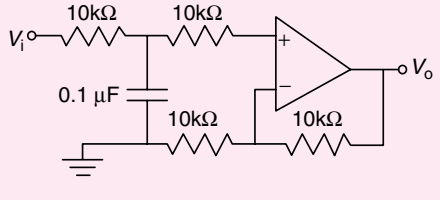
32. In the bistable circuit shown, the ideal opamp has saturation levels of ± 5 V. The value of R_1 (in kΩ) that gives a hysteresis width of 500 mV is ____. **[2015]**



33. Assuming that the opamp in the circuit shown below is ideal, the output voltage V_o (in volts) is _____. **[2015]**

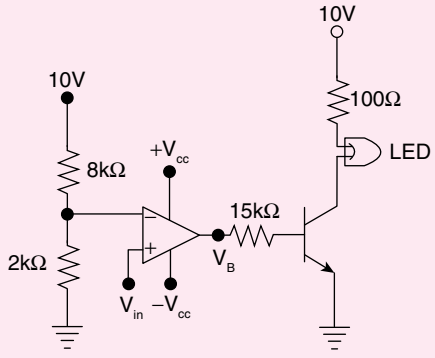


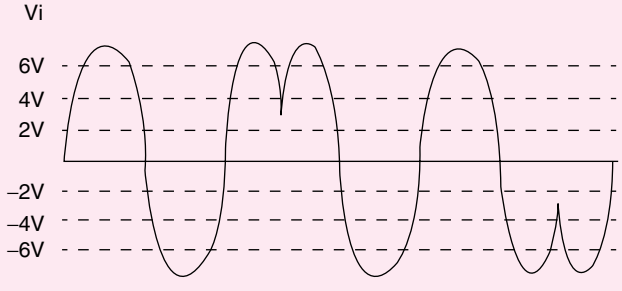
34. In the circuit shown using an ideal opamp, the 3-dB cut-off frequency (in Hz) is _____. **[2015]**



35. In the circuit shown, assume that the opamp is ideal. If the gain (v_o/v_{in}) is −12, the value of R (in kΩ) is _____. **[2015]**

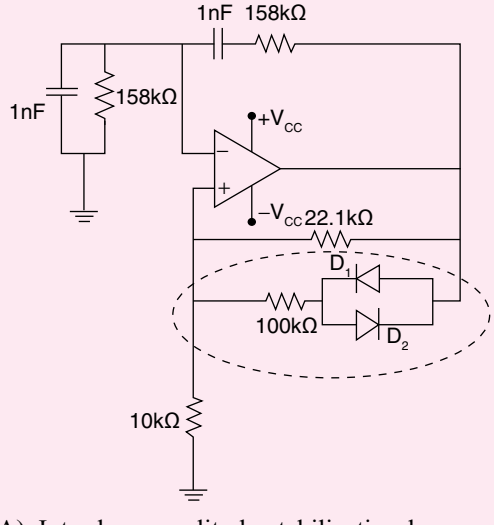
36. The following signal V_i of peak voltage 8V is applied to the non inverting terminal of an ideal opamp. The transistor has $V_{BE} = 0.7$ V, $\beta = 100$; $V_{LED} = 1.5$V, $V_{cc} = 10$ V and $-V_{cc} = -10$V **[2016]**





The number of times the LED glows is _____ .

37. Consider the oscillator circuit shown in the figure. The function of the network (shown in dotted lines) consisting of the 100kΩ resistor in series with the two diodes connected back to back is to **[2016]**



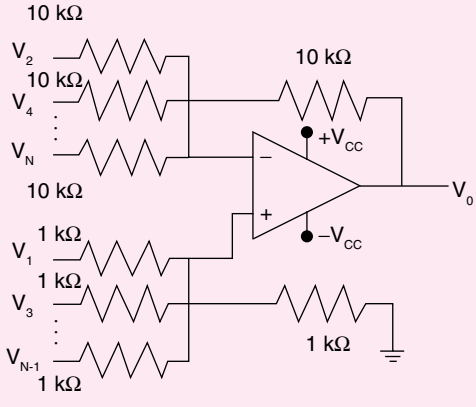
(A) Introduce amplitude stabilization by preventing the op-amp from saturating and thus producing sinusoidal oscillation of fixed amplitude.

(B) introduce amplitude stabilization by forcing the op-amp to swing between positive and negative saturation and thus producing square wave oscillations of fixed amplitude.

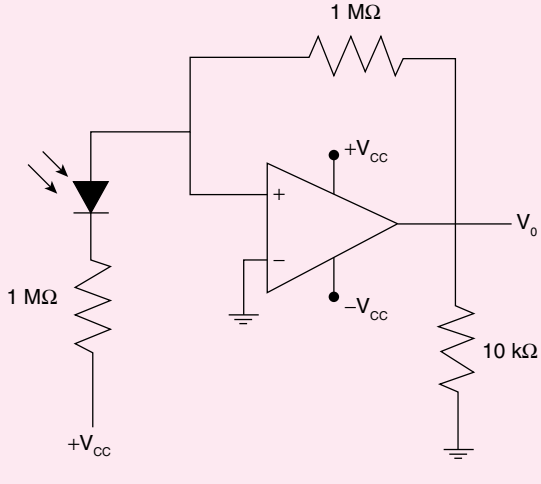
(C) introduce frequency stabilization by forcing the circuit to oscillate at a single frequency.

(D) enable the loop gains to take on a value that produces square wave oscillations.

38. An ideal opamp has voltage sources V_1, V_3, V_5, V_{N-1} connected to the non inverting input and V_2, V_4, V_6, V_N connected to the inverting input as shown in the figure below ($+V_{cc} = 15$ volt, $-V_{cc} = -15$ volt) the voltages V_1, V_2, V_3, V_4, V_5, V_6, are $1, -\frac{1}{2}, \frac{1}{3}, -\frac{-1}{4}, \frac{1}{5}, \frac{-1}{6}$ volt respectively. As N approaches infinitely, the output voltage (in volt) is _____ . **[2016]**

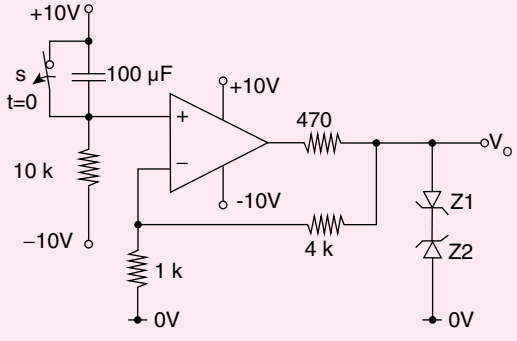


39. A p – I – n photodiode of responsivity 0.8 A/W is connected to the inverting input of an ideal op-amp as shown in the figure $+V_{cc} = 15V$, $-V_{cc} = -15V$, load resistor $R_L = 10k\Omega$. If 10μW of power is incident on the photodiode, then the value of the photocurrent (in μA) through the load is _____ . **[2016]**



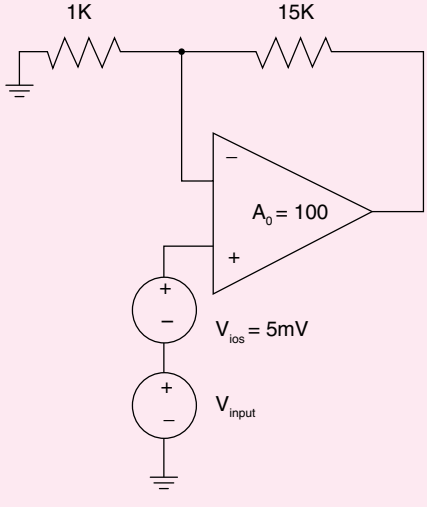
40. In the opamp circuit shown, the Zener diodes Z1 and Z2 clamp the output voltage V_0 to +5 V or –5V. The switch S is initially closed and is opened at time $t = 0$. **[2016]**

closed and is opened at time t = 0.



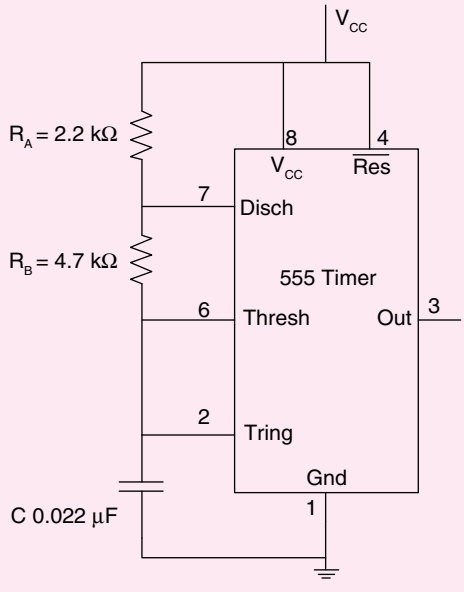
The time $t = t_1$ (in seconds) at which V_0 changes state is _____.

41. An opamp has a finite open loop voltage gain of 100. Its input offset voltage V_{ios} (= + 5mV) is modeled as shown in the circuit below. The amplifier is ideal in all other respects. V_{input} is 25mV. **[2016]**

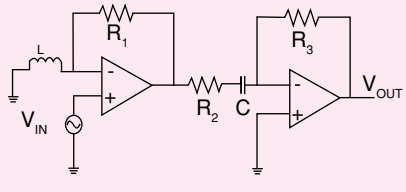


The output voltage (in mill volts) is ____

42. In the astable multivibrator circuit shown in the figure, the frequency of oscillation (in kHz) at the output pin 3 is _____. **[2016]**



43. For the circuit shown in the figure, $R_1 = R_2 = R_3 = 1$ Ω, $L = 1$ µH and $C = 1$ µF. If the input $V_{in} = \cos(10^6 t)$, then the overall voltage gain (V_{out}/V_{in}) of the circuit is _____. **[2016]**



Answer Keys

Exercises

Practice Problems 1

1. C	**2.** D	**3.** D	**4.** C	**5.** B	**6.** B	**7.** C	**8.** D	**9.** B	**10.** D
11. C	**12.** D	**13.** A	**14.** A	**15.** C	**16.** A	**17.** D	**18.** B	**19.** B	**20.** B
21. D	**22.** C	**23.** C	**24.** C	**25.** A	**26.** B	**27.** C	**28.** A	**29.** D	**30.** C
31. A	**32.** B	**33.** C	**34.** C	**35.** A	**36.** C	**37.** A	**38.** B	**39.** D	**40.** B
41. A									

Practice Problems 2

1. B	**2.** A	**3.** B	**4.** A	**5.** A	**6.** C	**7.** A	**8.** A	**9.** A	**10.** B
11. B	**12.** A	**13.** B	**14.** A	**15.** D	**16.** A	**17.** B	**18.** C	**19.** A	**20.** A
21. A	**22.** C	**23.** A	**24.** A	**25.** A	**26.** C	**27.** B	**28.** A	**29.** B	**30.** B
31. C	**32.** D	**33.** A	**34.** B	**35.** B	**36.** C	**37.** D	**38.** C	**39.** D	

Previous Years' Questions

1. B	**2.** A	**3.** A	**4.** A	**5.** B	**6.** C	**7.** A	**8.** D	**9.** B	**10.** C
11. D	**12.** A	**13.** C	**14.** B	**15.** B	**16.** C	**17.** A	**18.** D	**19.** A	**20.** B
21. D	**22.** B	**23.** B	**24.** C	**25.** 3.1 to 3.26		**26.** C	**27.** B	**28.** D	**29.** D
30. 249 to 251		**31.** 1.5	**32.** 1	**33.** 11 to 12		**34.** 159 to 160		**35.** 1	**36.** 3
37. A	**38.** 15 V	**39.** 800 µA		**40.** 0.798 sec		**41.** 413.8 mV		**42.** 5.67KHz	
43. −1									

Test

Analog Circuits

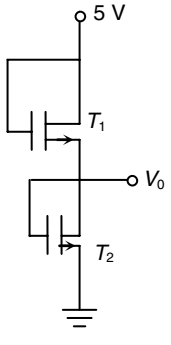
Time: 60 Minutes

Direction for questions 1 to 30: Select the correct alternative from the given choices.

1. A JFET has $\mu = 200$, $r_d = 300$ K, and $r_S = 1$ K. It is set up as a source follower. The output resistance is (R_0).
(A) 1000 kΩ (B) 333 kΩ
(C) 501 kΩ (D) 600 kΩ

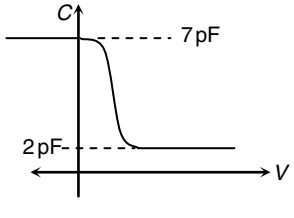
2. A bipolar transistor operating in active region has I_C = 2 mA, $\beta = 100$, and $V_T = 25$ mV. g_m and input resistance r_π in common emitter configuration is
(A) $g_m = 25$ mA/V and $r_\pi = 15.625$ kΩ
(B) $g_m = 80$ mA/V and $r_\pi = 4$ kΩ
(C) $g_m = 25$ mA/V and $r_\pi = 1.25$ kΩ
(D) $g_m = 80$ mA/V and $r_\pi = 1.25$ kΩ

3.



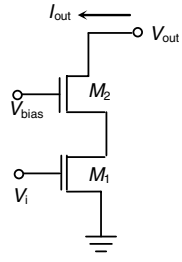
Both transistors are having $V_T = 1$ V. The device parameters K_1 and K_2 of T_1 and T_2 are 24 μA/V^2 and 6 μA/V^2. The output voltage is
(A) 1 V (B) 2 V (C) 3 V (D) 4 V

4. The high frequency capacitance–voltage characteristics of metal–SiO_2–Si (MOS) capacitor having an area of 1×10^{-4} cm^2. The permittivities of Si and SiO_2 are 1×10^{-12} F/cm and 3.5×10^{-13} F/cm. The maximum depletion layer width in Si is



(A) 0.143 μm (B) 0.357 μm
(C) 1 μm (D) 1.143 μm

5. Two identical NMOS transistors M_1 and M_2 are connected as shown in the figure. V_{bias} is chosen so that both the transistors are in saturation. The equivalent g_m of the pair is defined to $\frac{\delta I_{out}}{\delta V_i}$ at constant V_{out}



The equivalent g_m of the pair is
(A) the sum of individual g_m of the transistors
(B) the product of individual g_m of transistor
(C) nearly equal to g_m of M_1
(D) nearly equal to g_m of M_2

6. A junction transistor operating at room temperature with $I_C = 1$ mA, $\frac{KT}{q} = 22$ mV and $\beta = 50$. The value of g_m and r_π in mhos and ohm are, respectively,
(A) 0.0454, 1,100 (B) 0.0384, 1,200
(C) 0.08, 5,000 (D) 0.08, 1,250

7. In a full wave rectifier using centre tapped transformer R_L = 1 kΩ, each diode has a forward resistance of 300 Ω and the applied voltage is $V(t) = 240 \sin 50t$. The ripple factor r is
(A) 0.481 (B) 0.54 (C) 0.367 (D) 1.27

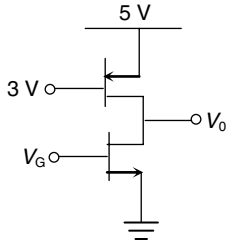
8. The cut-off frequency of a bipolar junction transistor increases with
(A) increase in base width
(B) increase in emitter width
(C) increase in collector width
(D) decrease in base width
(A) all (B) BC (C) D (D) B, C, D

9. An FET exhibits an I_{DSS} value of 10 mA when the drain voltage is 5 V and at a g_{m0} value of 5 mA/V. The value of V_P is
(A) 1 V (B) −2 V (C) 4 V (D) −6 V

10. Which of the following is correct?
(A) Zener breakdown voltage increases with temperature, while avalanche breakdown voltage decreases with temperature
(B) Both Zener and avalanche breakdown voltage increase with temperature.
(C) Both Zener and avalanche breakdown voltage decrease with temperature.
(D) Zener breakdown voltage decreases with temperature, while avalanche breakdown voltage increases with temperature.

Direction for questions 11 and 12:
Consider the CMOS circuit shown where gate voltage V_G of the n-MOSFET is increased from zero, while the gate

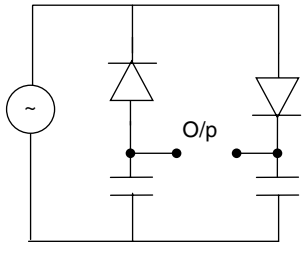
voltage of P-MOSFET is kept constant at 3 V. Assume that for both transistors, the magnitude of the threshold voltage is 1 V and product of transconductance parameter and the (W/L) rate, that is, quantity of μc_{ox} (W/L) is 1 mAV^{-2}.



11. For small increase in V_G beyond 1 V, which of the following gives correct description of region of operation of each MOSFET?
(A) Both the MOSFETs are in saturated region.
(B) Both the MOSFETs are in triode region.
(C) n-MOSFET is in saturation and P-MOSFET in triode region.
(D) n-MOSFET is in triode region and P-MOSFET in saturation.

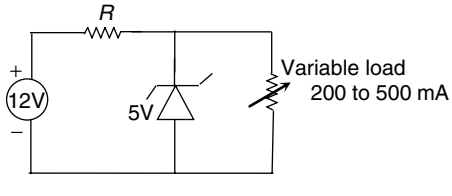
12. Estimate the output voltage V_0 for $V_G = 1.4$ V.
(A) 4.91 (B) 4 (C) 4.2 (D) 3

13. The circuit shown is



(A) bridge rectifier
(B) ring modulator
(C) frequency discriminator
(D) voltage doubler

14. In the voltage regulator, load current can vary from 200 mA to 500 mA. Assuming Zener diode is strictly ideal. The minimum value of R is



(A) 35 Ω (B) 70 Ω (C) 70/3 Ω (D) 14 Ω

15. In a full-wave centre tap rectifier, V_{dc} and V_m are the DC and peak values of voltage, respectively, across a resistive load. If PIV is the peak inverse voltage of diode then

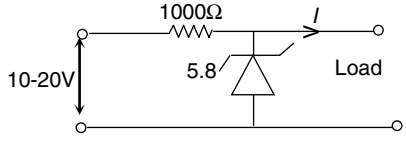
(A) $V_{DC} = \frac{V_m}{\pi}$, PIV = 2 V_m

(B) $V_{DC} = \frac{2V_m}{\pi}$, PIV = 2$V_m$

(C) $V_{DC} = \frac{2V_m}{\pi}$, PIV = V_m

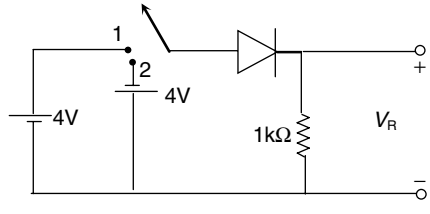
(D) $V_{DC} = \frac{V_m}{\pi}$, PIV = V_m

16. The Zener diode in the regulator circuit has a Zener voltage of 5.8 V and a Zener knee current of 0.5 mA. The maximum load current I drawn from the circuit ensuring proper functioning over input V range from 10 to 20 V is



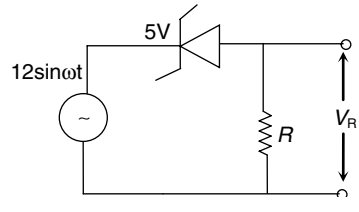
(A) 13.7 mA (B) 14.2 mA
(C) 3.7 mA (D) 24.2 mA

17. In the following circuit, switch was connected to position 1 at $t < 0$ and at $t = 0$, and t is changed to position 2. Assume diode has zero voltage drop and a storage time t_s. For $0 < t \le t_s$, V_R is given by

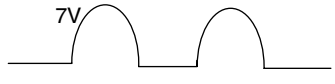


(A) $V_R = -4$ (B) $V_R = 4$
(C) $0 \le V_R < 4$ (D) $-4 \le V_R \le 0$

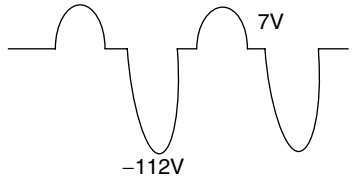
18. The waveform obtained across R is



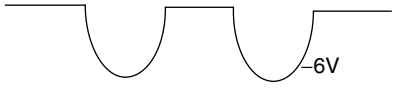
(A)



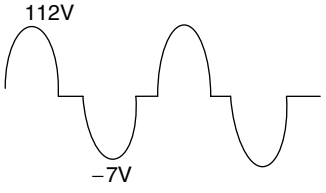
(B)



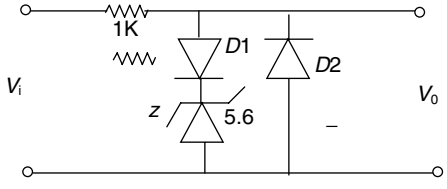
(C)



(D)

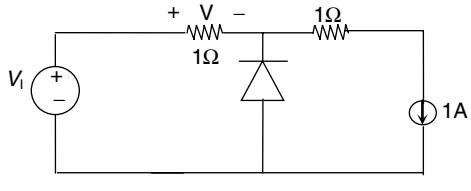


19. In the limiter circuit, an input voltage $V_i = 10 \sin 2\pi t$ is applied. Assume that the diode drop is 0.7 V when it is forward biased. The Zener breakdown voltage is 5.6 V. The maximum and minimum values of output voltage, respectively, are



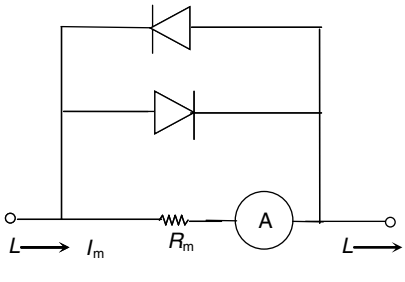
(A) 6.1 V, −0.7 V (B) 0.7 V, −7.5 V
(C) 6.3 V, −0.7 V (D) 6.3 V, −7.5 V

20. In the circuit, diode is ideal. The voltage V is



(A) min (v_1, 1) (B) max (v_1, 1)
(C) min ($-v_1$, 1) (D) max ($-v_1$, 1)

21. Two Si diodes are used to protect a delicate micro-ammeter from damage by excessive current. The meter shows full scale deflection when $I_m = 150\ \mu A$ and meter resistance R_m is 4.5 kΩ. The diodes can be represented in this low current application by a piecewise linear model with $V_0 = 0.7$ V and $I_d = 0\ \Omega$. What bias V will appear across the diodes when meter show full scale deflection?

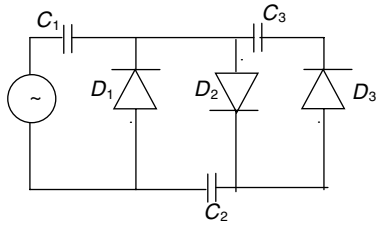


(A) 0.03 V (B) 0.675 V
(C) 0.675 mV (D) 0.7 V

22. The voltage across the secondary of a transformer in half wave rectifier with shunt capacitor filter is 50 V. The maximum voltage that will occur in reverse biased diode will be

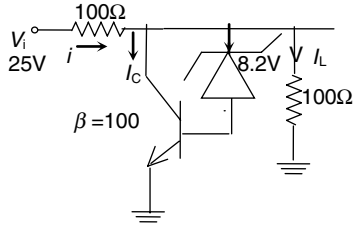
(A) 100 V (B) 88 V
(C) 50 V (D) 25 V

23. Identify the circuit



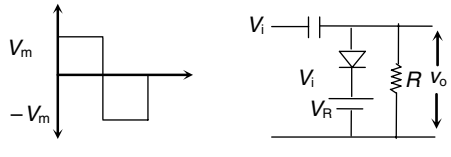
(A) voltage doubler (B) pulse train generator
(C) Darlington amplifier (D) voltage tripler

24. The current through the Zener is

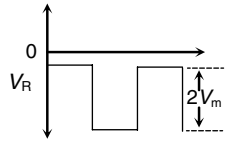


(A) 89 mA (B) 109 mA
(C) 78 mA (D) 0.78 mA

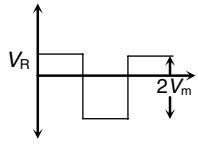
25. Identify the output waveform.



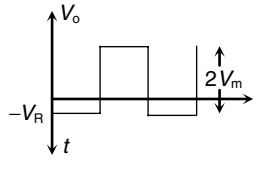
(A)



(B)

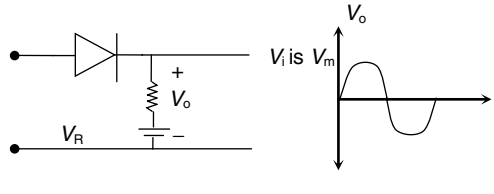


(C)

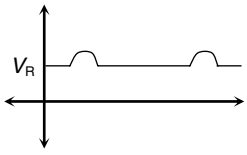


(D) None of these

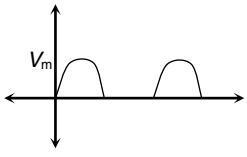
26. Identify the output.



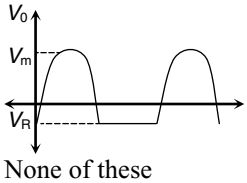
(A)



(B)



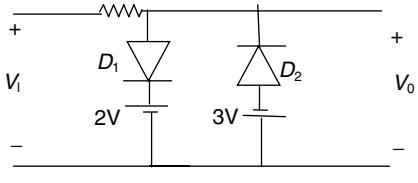
(C)



(D) None of these

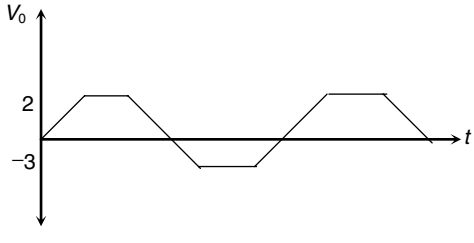
Direction for questions 27 and 28:

For input of $V_i = 5\sin\omega t$.

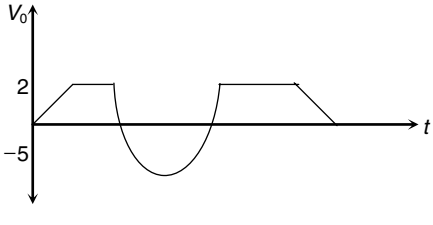


27. Find the output waveform.

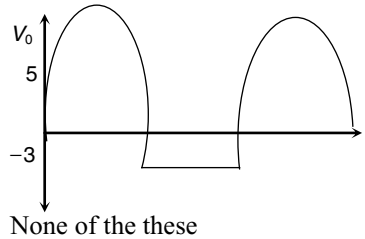
(A)



(B)



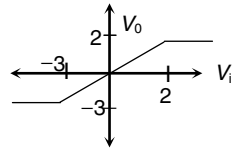
(C)



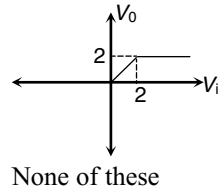
(D) None of these

28. The plot of V_0 versus V_i for the abovementioned question is

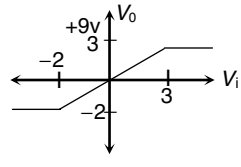
(A)



(B)

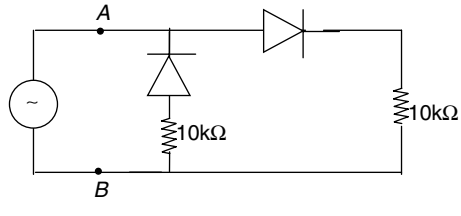


(C)



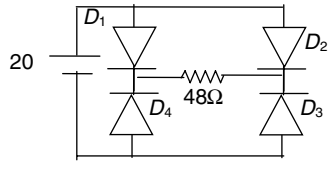
(D) None of these

29. A voltage source $V_{AB} = 2\sin\omega t$ is applied to the input terminals. The impedance by the circuit across the terminals A and B are



(A) 5 kΩ (B) 10 kΩ (C) 15 kΩ (D) 20 kΩ

30. Current through 48 Ω resistor in the following circuit.



(A) 152 mA (B) 162 mA
(C) 0 mA (D) 182 mA

Answer Keys

1. C	**2.** D	**3.** C	**4.** B	**5.** C	**6.** A	**7.** A	**8.** D	**9.** C	**10.** D
11. D	**12.** A	**13.** D	**14.** D	**15.** B	**16.** A	**17.** A	**18.** B	**19** C	**20.** D
21. B	22. A	23. A	24. D	25. B	26. A	27. A	28. A	29. B	30. C