☆ Counter:

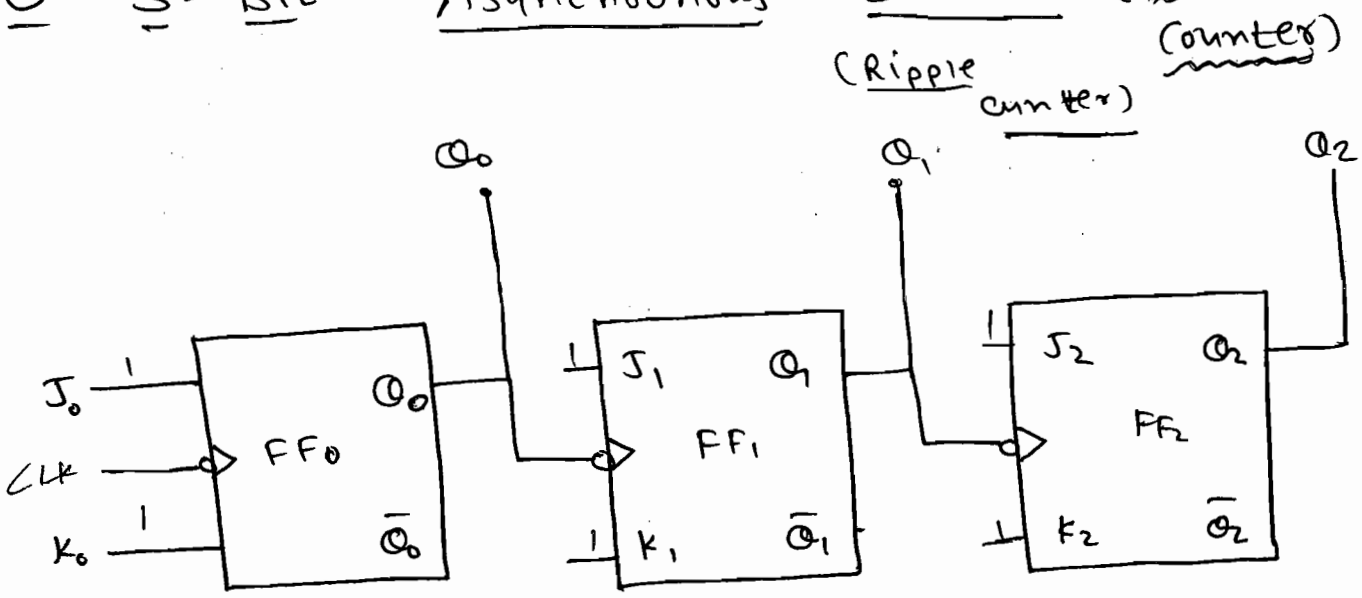
① Asynchronous (Ripple) Counter:

→ Any FF, but in toggle mode:

② Synchronous (parallel) Counters:

→ Any FF

① 3-Bit Asynchronous Counters: (UP (Ripple counter) counter)



→ As J=K=1 => All FFs are in toggle mode.

$\overline{Q(t+1)} = Q(t)$.

→ Q_0 is toggle for every clock pulse.

→ Q_1 is toggle when Q_0 Changes from '1 to 0'

→ Q_2 is toggle when Q_1 Chages from '1 to 0'.

CLK	Q_0 (LSB)	Q_1	Q_2 (MSB)	
0	0	0	0	0
1	1	0	0	1
2	0	1	0	2
3	1	1	0	3
4	0	0	1	4
5	1	0	1	5
6	0	1	1	6
7	1	1	1	7
8	0	0	0	8

→ Up counter

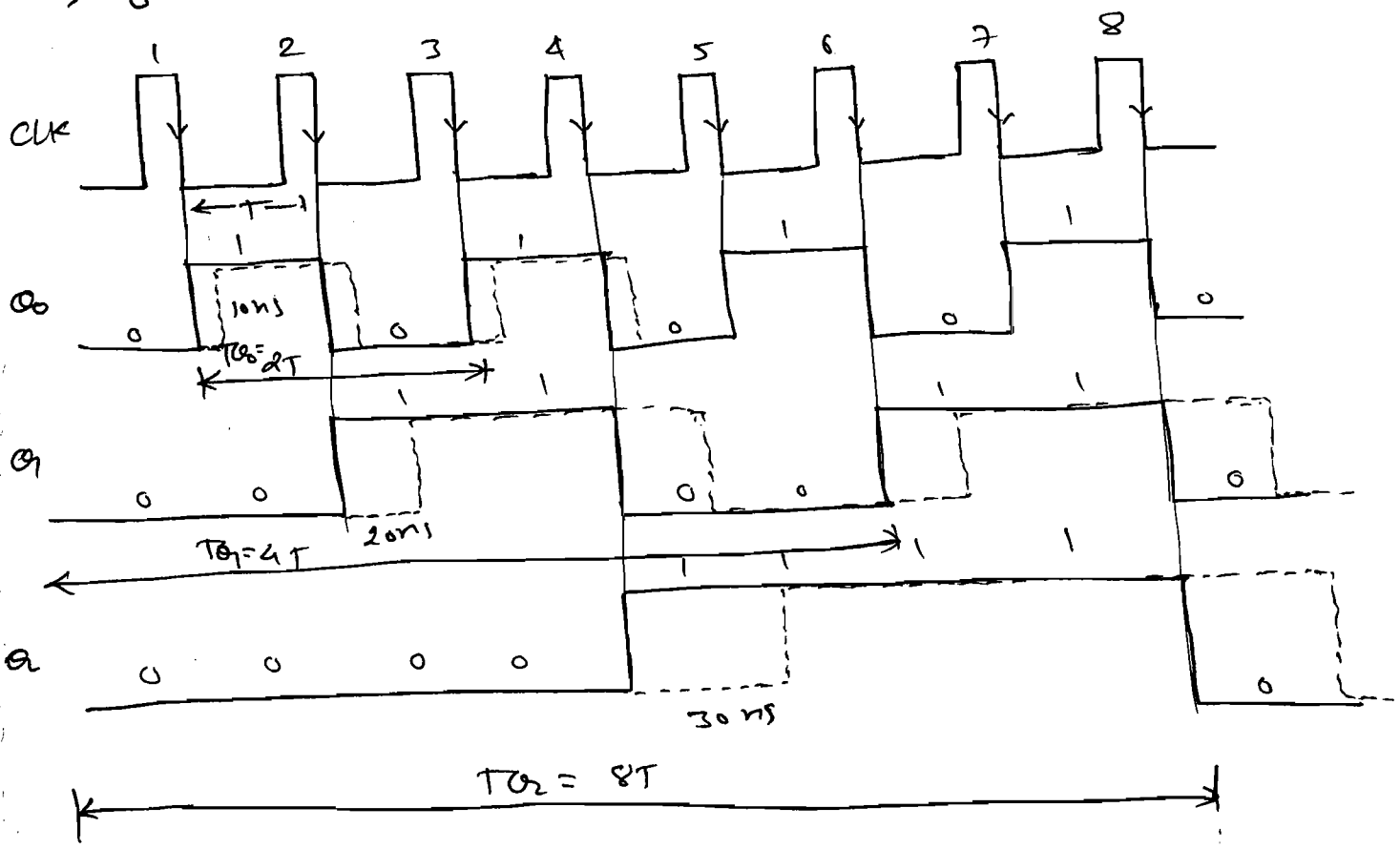
$t_{pd,FF} = 10ns$

Q_0 is delay by 10ns

Q_1 is delay by 20ns

Q_2 is delay by 30ns.

→ freq. is divided by after each flip flop.



* Max. Conv. time = 3x10ns = 30ns.

Clock period $T \geq 30ns$.

$\therefore f = \frac{1}{T} \leq \frac{1}{30 \times 10^{-9}}$.

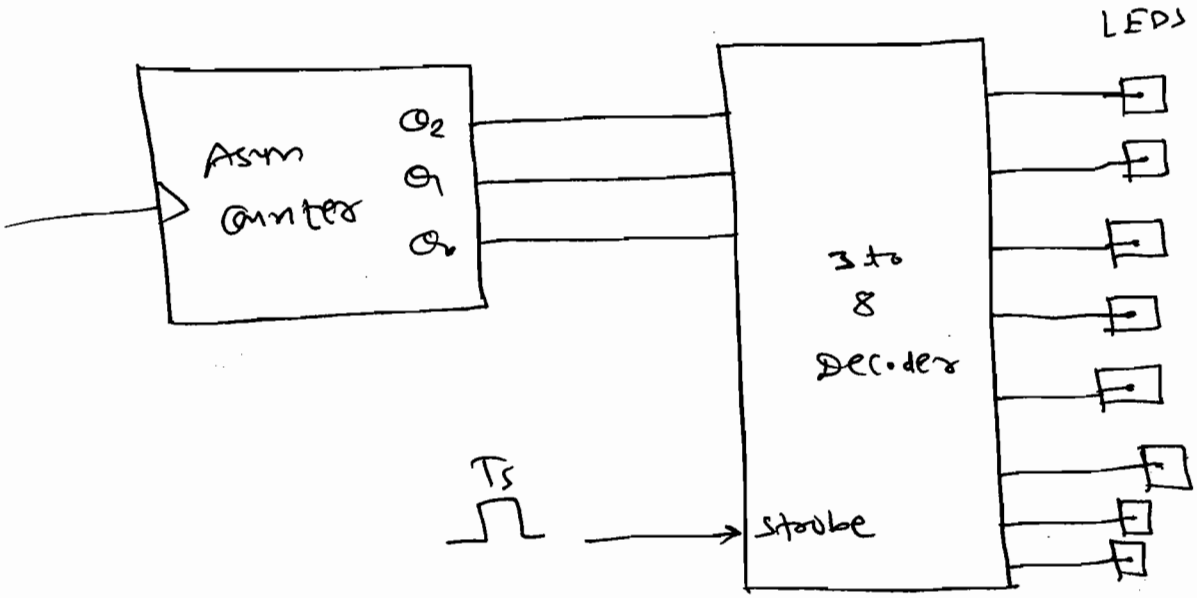
i.e. $f \leq \frac{1}{30 \times 10^{-9}}$.

In general,

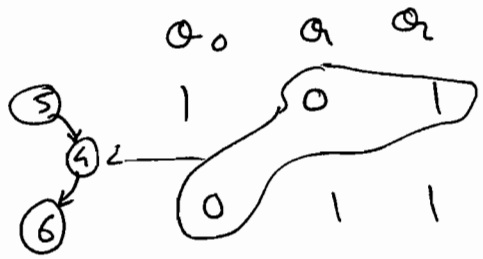
N- Bit Asynchronous Counter,

$$\therefore \quad f \leq \frac{1}{N \cdot t_{pd,FF}}.$$

→ Freq. of Async. Counter using strobe pulse.



~~Not~~



$$\therefore \quad f \leq \frac{1}{N \cdot t_{pd,FF} + T_S}.$$

→ Asynchronous Counter uses strobe where as strobe are not required in Synchronous.

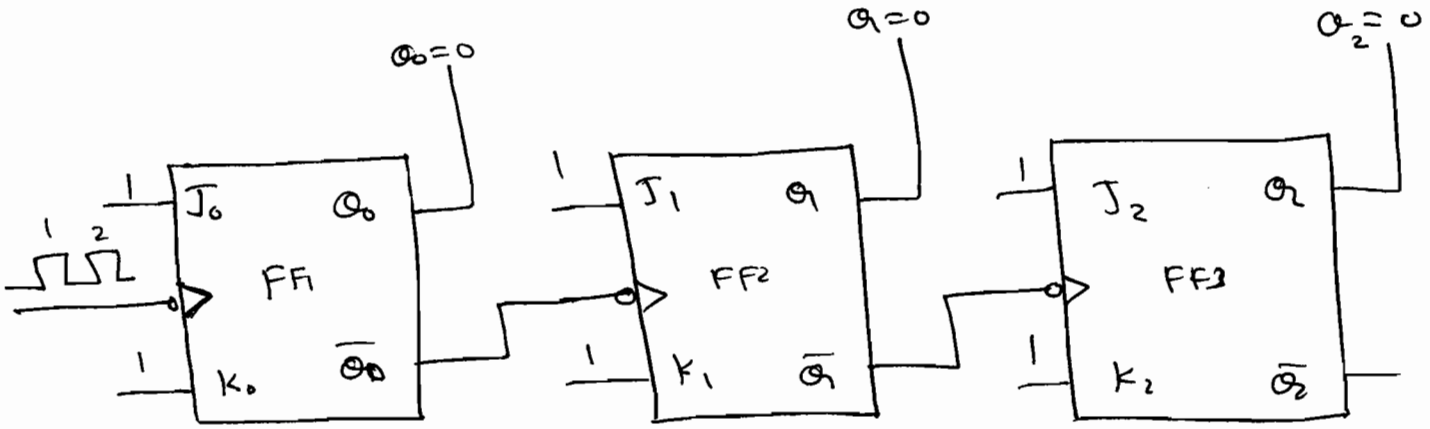
* 3-bit asynchronous counter. (Down counter).

→ In the following circuits,

(1) Q_0 Changes (toggles) for each clock pulse.

(2) Q_1 toggles when Q_0 changes from 0 to 1.

(3) Q_2 toggles when changes from 0 to 1.

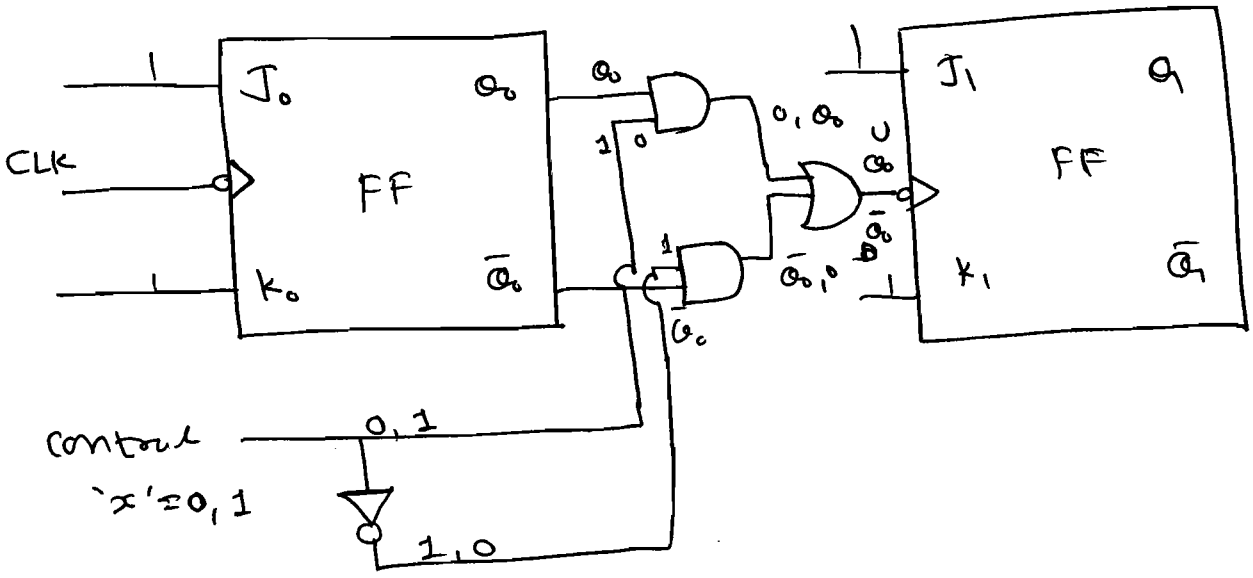


Note: All FFs are in toggle mode.

CLK	(LSB) Q_0	Q_1	(MSB) Q_2	Decimal
0	0	0	0	0
	↓	↓	↓	7
1	1	1	1	
2	0	1	1	6
3	1	0	1	5
4	0	0	1	4
5	1	1	0	3
6	0	1	0	2
7	1	0	0	1
8	0	0	0	0

→ Down counter.

* 2-Bit "Asynchronous Up-Down" Counter.



→ If $\boxed{x=0}$ ⇒ "$\bar{Q}_0$" is connected to the Clock of Next FF.

→ If $x=1$ ⇒ $\boxed{\text{Down Counter}}$

i.e. 00, 11, 10, 01, 00, ...

→ If $\boxed{x=1}$ ⇒ "Q_0" is connected to the Clock of Next FF.

⇒ $\boxed{\text{Up Counter}}$

i.e. 00, 01, 10, 11, 00, ...

Imp
NOTE: In the above Up-Down Counter if +ve edge triggered FF circuits then

① 'x' = 0 → It act as Up Counter.
② 'x' = 1 → It act as Down Counter

Hint: ✱ **Up Counter**

triggering @

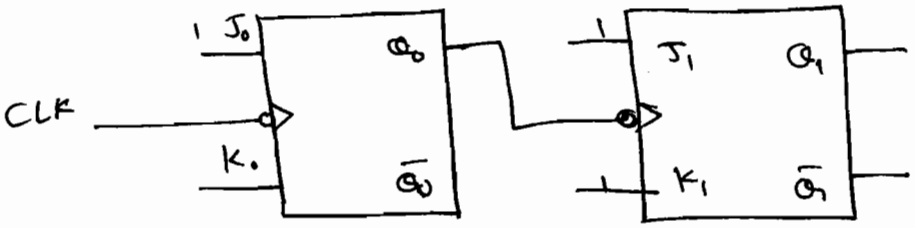
- neg. → positive (or)
- pos. → negative.

✱ **Down Counter**

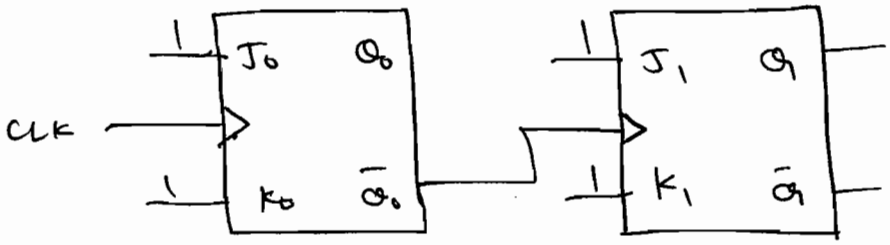
triggering @

- neg. → negative
- pos. → positive

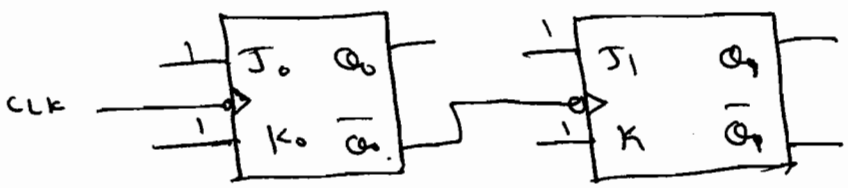
① Up Counter:



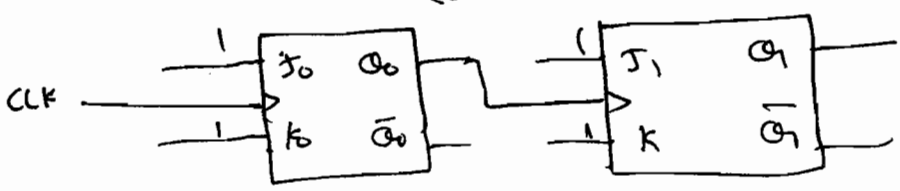
(or)



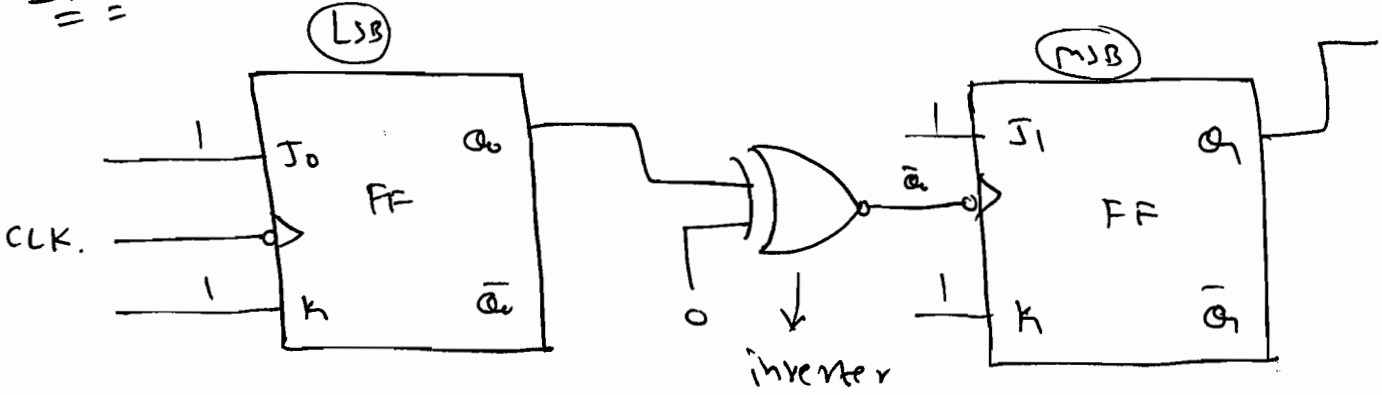
② Down Counter:



(or)



Ex-1



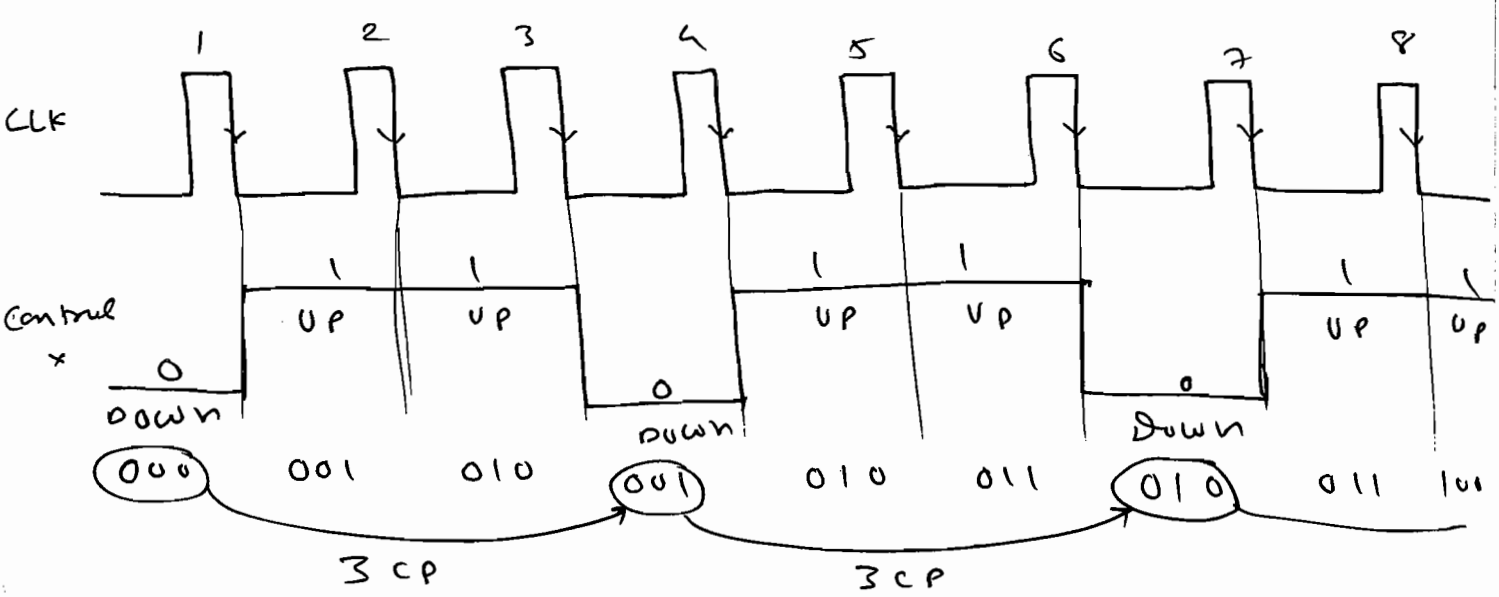
Ans

→ FF is -ve edge triggered, $\bar{Q}_0 \rightarrow$ CLK

hence it is **Down Counter.**

Imp

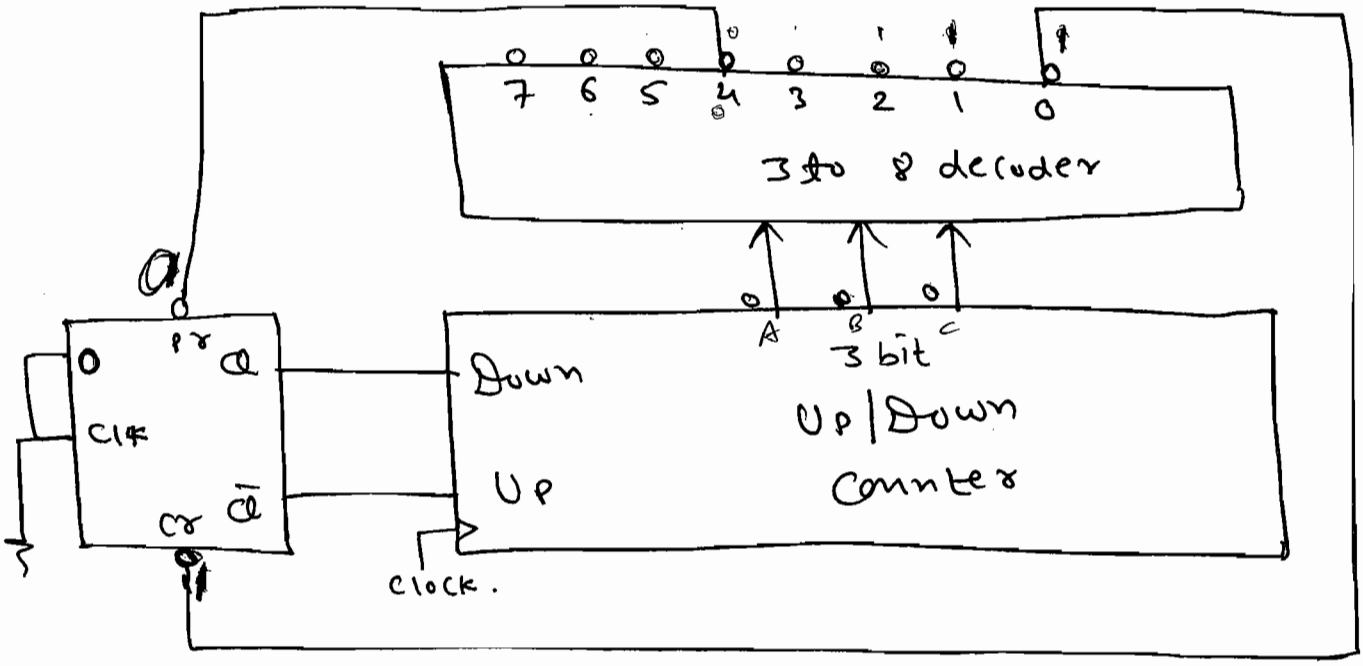
Ex-1 In a 3-bit asynchronous up-Down Counter the clock and control inputs are as given below: Determine the no. of clock pulses required to bring the counter to the initial counting seq. starting with 000.



→ In this Counter each increment requires three clock pulses.

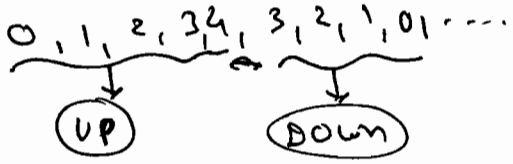
→ To increment 8 times No. of CLOCK pulses are $8 \times 3 = 24$.

Ex-2 In the following Up down Counter determine the counting sequences of the counter.



Ans:

CLK	A	B	C	
0	0	0	0	
1	0	0	1	UP
2	0	1	0	UP
3	0	1	1	UP
4	1	0	0	UP
5	0	1	1	Down
6	0	1	0	Down
7	0	0	1	Down
8	0	0	0	Down



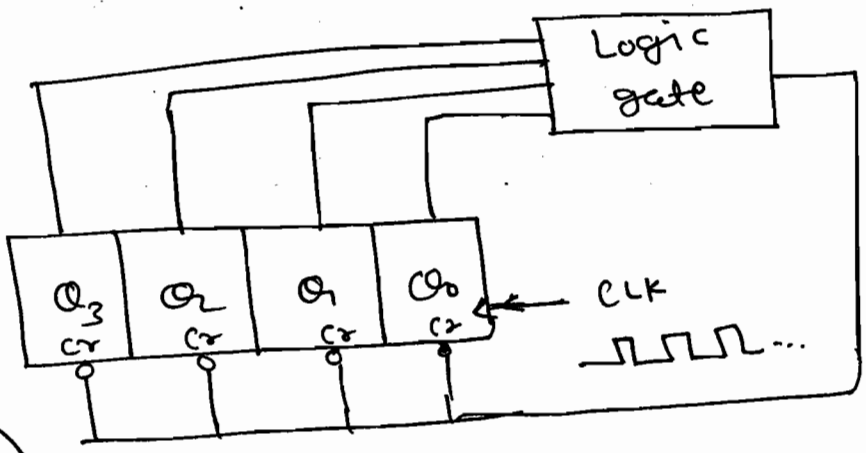
$\left[\because Pr=1,\ Cr=0 \right.$
$\left. \text{i.e } Q=0,\ \bar{Q}=1 \right]$
$\left[\because Pr=0,\ Cr=1 \right.$
$\left. \text{i.e. } Q=1,\ \bar{Q}=0 \right]$.

☆ Modulus of a Counter.

→ It is the number of CLK pulses required to bring the counter in the initial state.

→ A Mod-N Counter counts from 0 to N-1 and output freq. is f/N.

E.g.



Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
⋮			
1	0	0	1
10 → 1	0	1	0
⋮			
1	1	1	1

After the required value, F should be zero

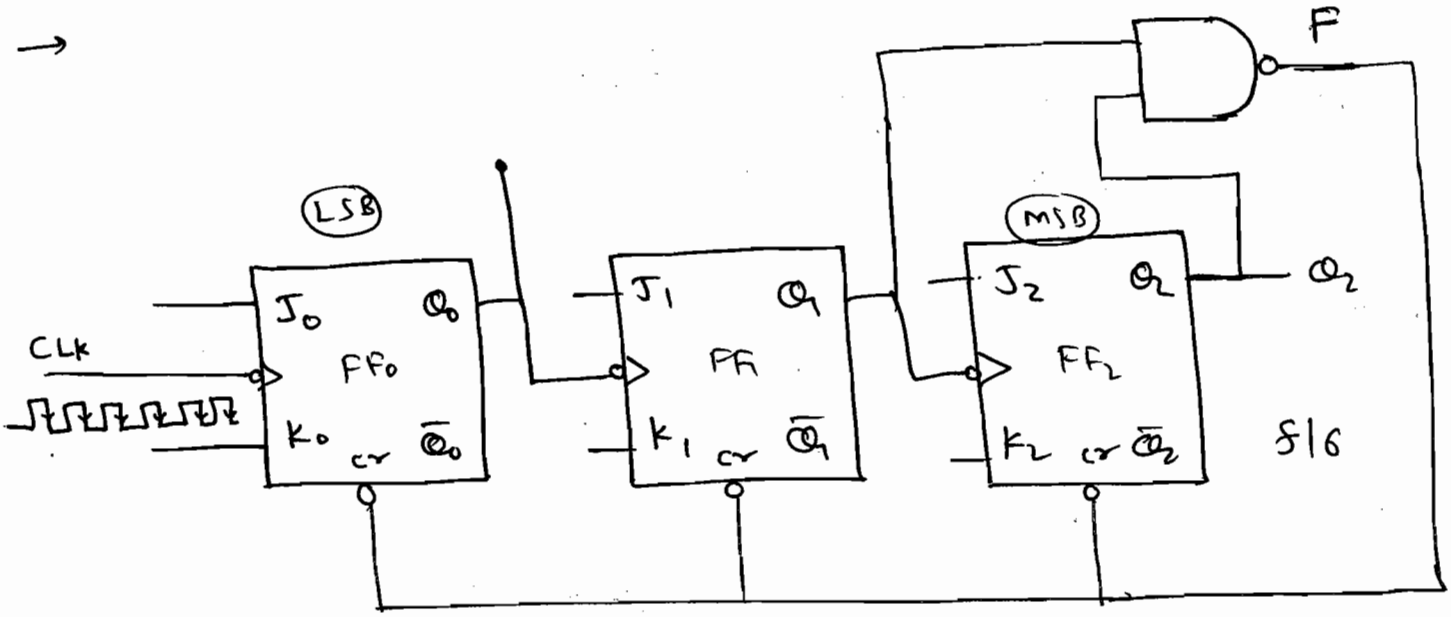
F=0.

i.e for e.g. 12

* Construct a Mod-6 Asynchronous Counter.

→ As soon as it reaches 6 CLK pulse it should be reset.

→



→ 0 to 5 ⇒ $2^N \geq$ No. of modes of counter.

$\therefore \quad 2^N \geq 6$

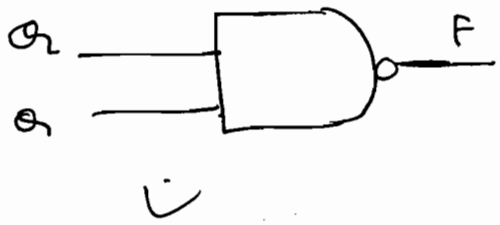
$N = 3$ FFs

CLK	Serial inputs	Q_2	Q_1	Q_0	Decimal
0	–	0	0	0	0
1	1	0	0	1	1
2	1	0	1	0	2
3	1	0	1	1	3
4	0	1	0	0	4
(6)	0	1	0	1	5
	0	1	1	0	6
		0	0	0	

(i) At 6^{th} CLK pulse $\boxed{Q_2 = 1,\ Q_1 = 1}$

(ii) Hence when $\boxed{Q_2 = 1,\ Q_1 = 1}$ ⇒ o/p of gate $\boxed{F = 0}$. All FFs are cleared.

⇒ $\boxed{\text{NAND gate}}$

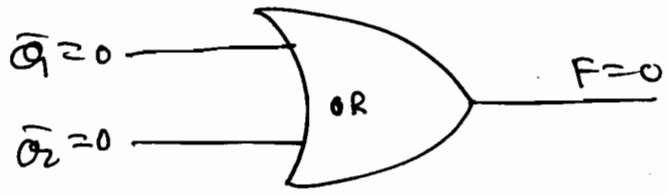


(i)

→ In the above mod-6 asynchronous counter determine the feedback logic gate if its inputs are $\bar{Q}_2$ & $\bar{Q}_1$

→ i.e. $\bar{Q}_2 = 0$ and $\bar{Q}_1 = 0$ ⇒ o/p of gate F=0.

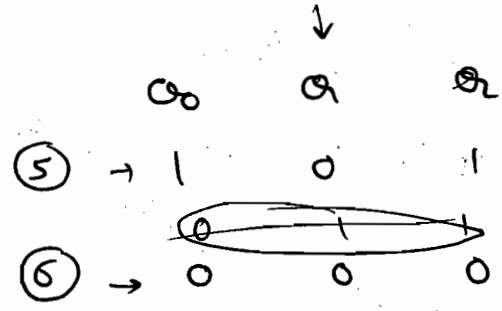
∴ ⇒ $\boxed{\text{OR gate.}}$



* Disadvantages:

→ In Asynchronous Counters whose modulus is not equal to 2^N the output produces unwanted spikes called as Glitches.

E.g.



Latch:

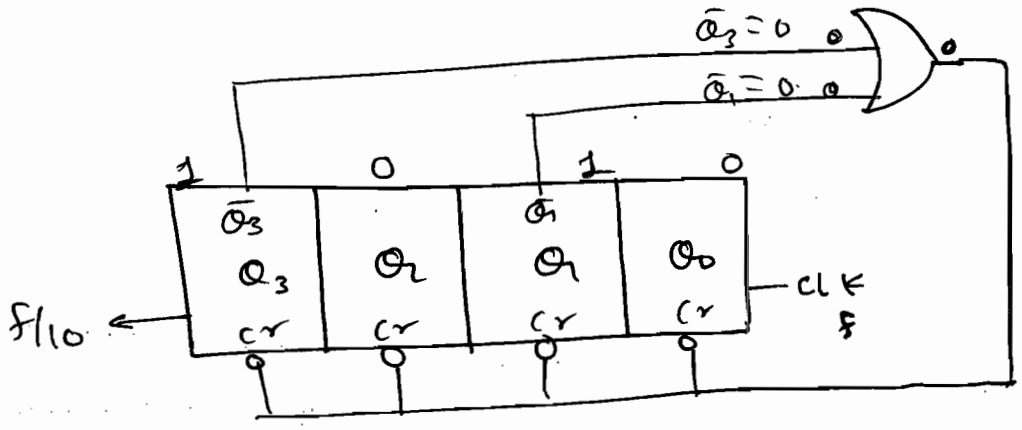
→ output is latched on input; output doesn't change even if input changes

→ Glitches.

② If the FF are having unequal clearing times then all the FFs cannot be cleared at the required CLOCK pulse. To overcome this a latch is used in the feedback path such that it output remains zero untill all the FFs are cleared.

Ex-1: Determine the modulus of the following Asynchronous counters:

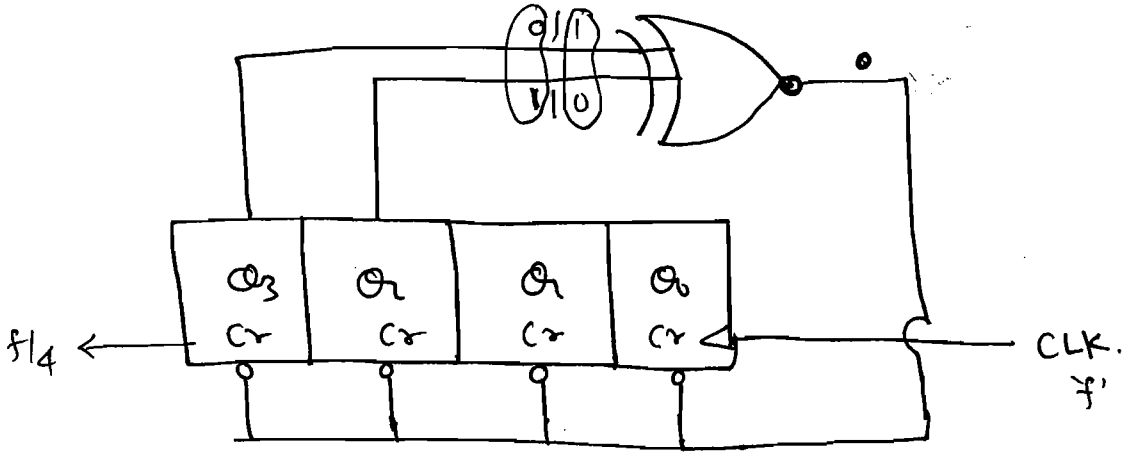
a)



→ For $Q_3 Q_2 Q_1 Q_0 = 1010$ → All the FFs are cleared.

→ It is Mod-10 Counter (decade counter)

(b)



Ans:

$f \propto \frac{1}{N}$

Q_3 Q_2 Q_1 Q_0

0 0 0 0

0 0 0 1

!

0 1 0 0 0000

:

1 0 0 0

1 1 1 1

0 1 2 3 ✗

4 will appear first i.e 01. will appear first than 10.

For $Q_3 Q_2 Q_1 Q_0 = 0100$ → All the FFs are cleared

→ It is Mod - 4 Counter.

→ The disadvantages of Asynchronous Counter is the freq. of operation is inversly proportional to the no. of FFs. To overcome this we use Synchronous or parallel Counters.

* Flip Flop Excitation table:

① S-R FF:

Q(t)	Q(t+1)	S	R
0 →	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

② D- Flip Flop:

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

③ T- Flip Flop.

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

④ J-K- Flip flop.

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

* Summary of FF excitation table:

Q(t)	Q(t+1)	FF Inputs J	K	S	R	D	T
0	0	0	X	0	X	0	0
0	1	1	X	1	0	1	1
1	0	X	1	0	1	0	1
1	1	X	0	X	0	1	0

Ex-1: Determine the excitation table of X-Y FF whose T.T. is as given below.

X	Y	Q(t+1)
0	0	1
0	1	Q(t)
1	0	$\overline{Q}(t)$
1	1	0

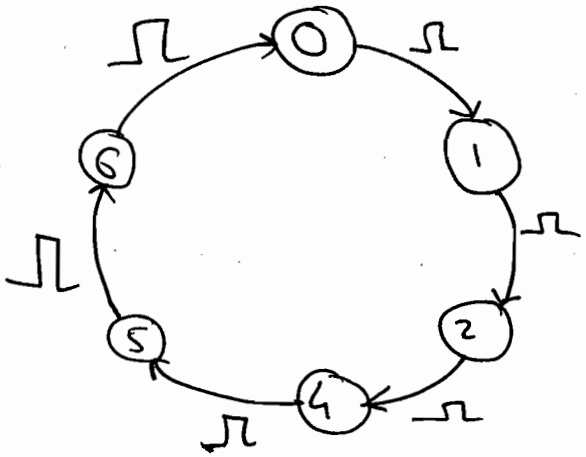
Q(t)	Q(t+1)	X	Y
0	0	X	1
0	1	1	0
1	0	1	X
1	1	0	X

* Design a Synchronous Counter using J-K FlipFlops. which Comes through the states 0, 1, 2, 4, 5, 6, 0, ...

(b) is it a self starting Counter?

Ans:

(a) State Diagram:



(b) State Assignment:

0 → 000

1 → 001

2 → 010

4 → 100

5 → 101

6 → 110.

(c) Excitation Table:

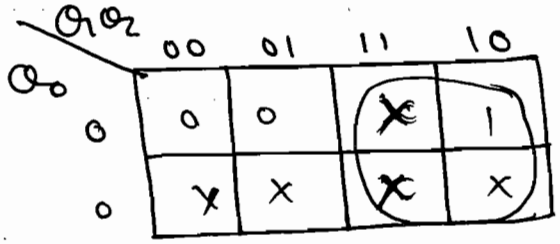
	Q_2	Q_1	Q_0	FF Inputs J_2K_2	J_1K_1	J_0K_0
0	0	0	0	0 X	0 X	1 X
1	0	0	1	0 X	1 X	X 1
2	0	1	0	1 X	X 1	0 X
4	1	0	0	X 0	0 X	1 X
5	1	0	1	X 0	1 X	X 1
6	1	1	0	X 1	X 1	0 X
7	0	0	0			

* (3), (7) are unused states. Takes them as dont cares.

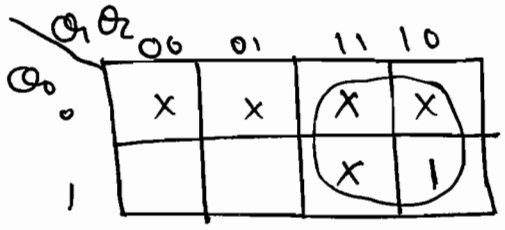
$J_0 = \bar{Q}_1$ $K_0 = 1$

$J_1 = Q_2 + Q_0$ $K_1 = 1$

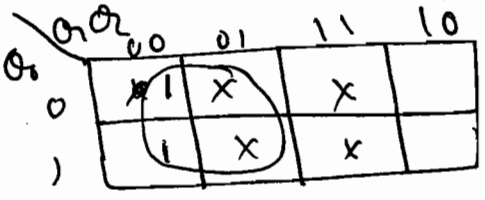
$J_2 = Q_1$ $K_2 = Q_1$



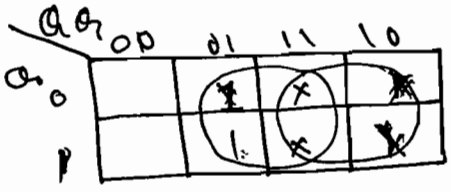
$J_2 = Q_1$.



$K_2 = Q_1$

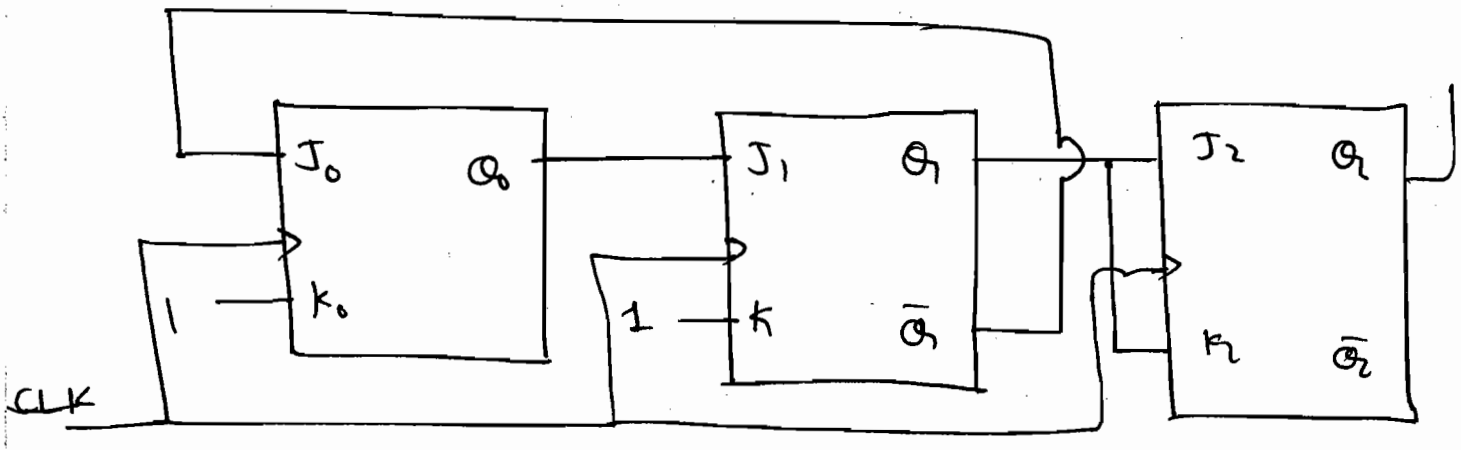


$J_0 = \bar{Q}_1$



$J_1 = Q_2 + Q_0$.

Ex/2 Sync

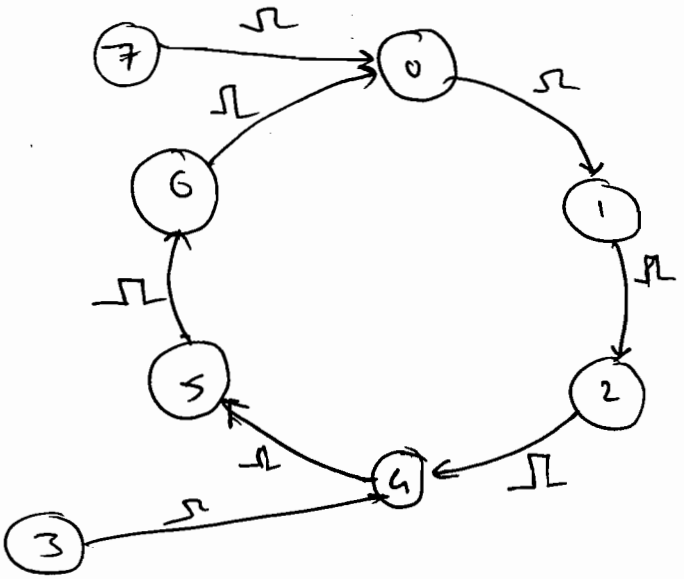


→ In Sync Counter, Freq of operation

$$f \leq \frac{1}{t_{pd} \cdot FF}$$

(b)

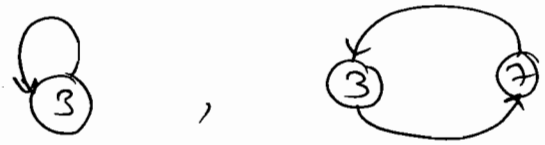
Present State			FF Inputs			Next State		
Q_2	Q_1	Q_0	J_2K_2	J_1K	J_0K_0	Q_2	Q_1	Q_0
0	1	1	1 ~	1 ~	0 ~	1	0	0 (4)
1	1	1	1 ~	1 ~	1 ~	0	0	0 (0)



It is a self starting Counter as we get (2) after (3) and (0) after (7)

→ The above counter is a self starting counter because it is able to enter the used states from all unused state.

e.g. of non self starting counter

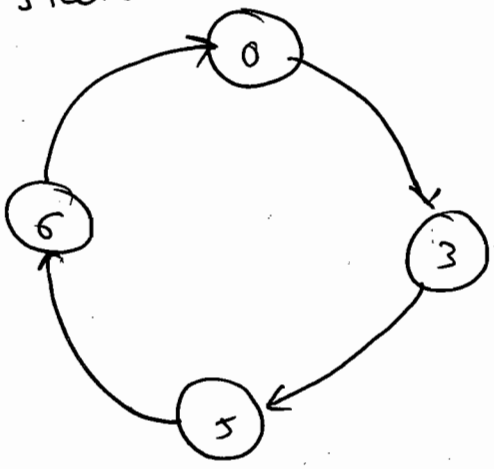


Ex-2 ⇒ A synchronous counter comes through the states 0, 3, 5, 6, 0, ... and FF inputs are $T_2 = Q_1$, $T_1 = 1$, $T_0 = \bar{Q}_1$. Is it a self starting counter.

⇒ Table for analysis:

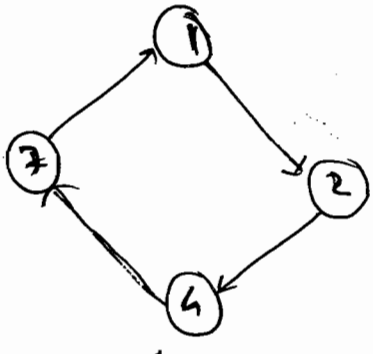
	Pr. State Q_2 Q_1 Q_0	FF Inputs $T_2 = Q_1$ $T_1 = 1$ $T_0 = \bar{Q}_1$	Next State Q_2 Q_1 Q_0	
①	0 0 1	0 1 1	0 1 0	②
②	0 1 0	1 1 0	1 0 0	④
④	1 0 0	0 1 1	1 1 1	⑦
⑦	1 1 1	1 1 0	0 0 1	①

Used state



→ It is an efficient counter.

Unused state

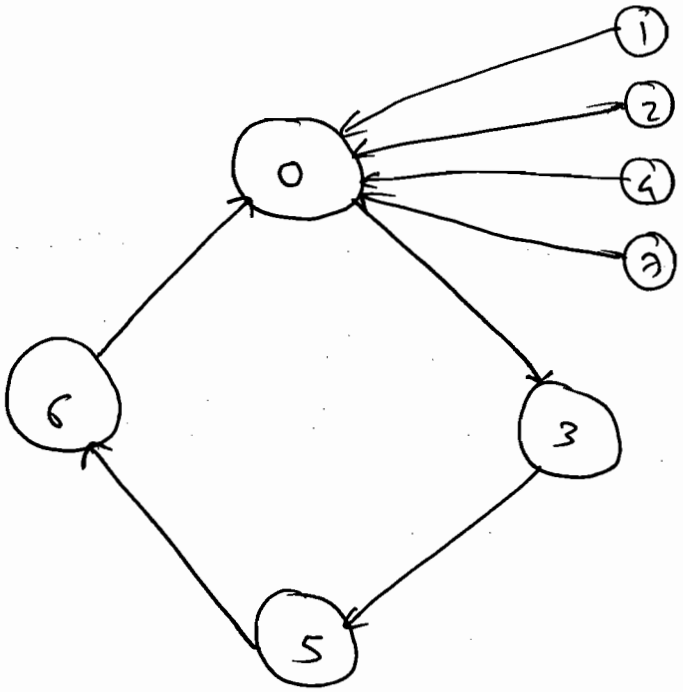


'Lock-out' of counter

Mostly self starting counter

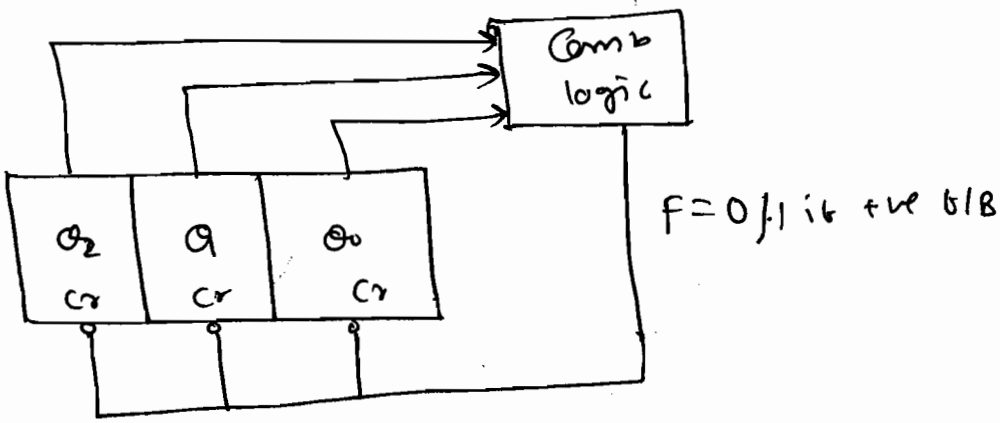
→ To avoid the Lock-out condition

① Redesign the Counter according to the following state diagram.

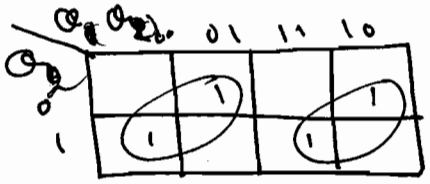


→ No. of FF state is increasing ⇒ no. of FF is increased in it will increase the Complexity of Ckt

② Clearing the Counter as soon it enters into Unsed state. as shown below:



$F(Q_2, Q_1, Q_0) = \Sigma m(1, 2, 4, 7)$.



$$\therefore \quad F = Q_2 \oplus Q_1 \oplus Q_0$$

(or)

$$F = Q_2 \odot Q_1 \odot Q_0$$

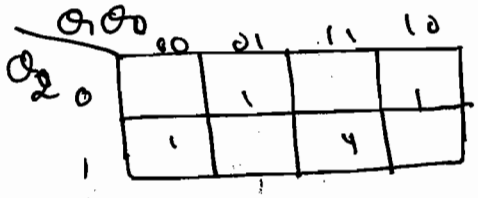
NOTE:

⇒ In the above synchronous counter the combinational logic is determine as follows:

→ When Counter enters into the states ①, ②, ④, ⑦ the F should become 1. So, that the counter can be clear.

→ The sum of minterm expression for F is

$$F(Q_2, Q_1, Q_0) = \Sigma [1, 2, 4, 7).$$

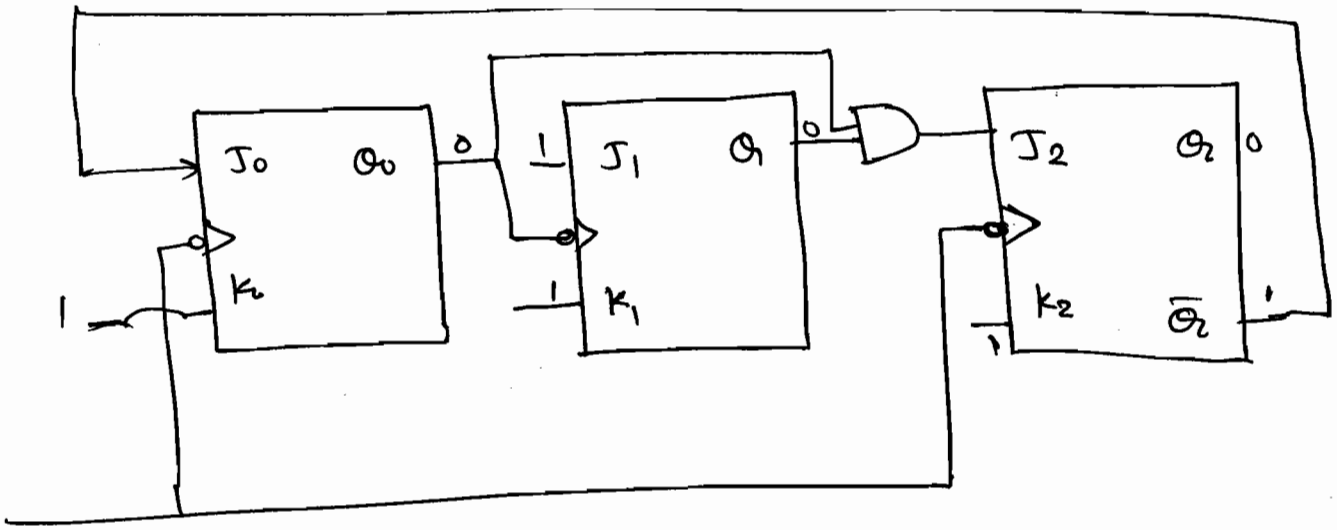


$$\therefore \quad F = Q_1 \oplus Q_2 \oplus Q_3$$

(or)

$$F = Q_1 \odot Q_2 \odot Q_3.$$

Ex-2 Determine the modulus of the following counter



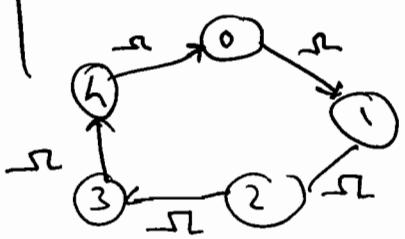
Ans: 'Q_1' is in Asynchronous mode. It toggle when Q_0 changes from 1 to 0!

Now $J_0 = \bar{Q}_2$, $J_2 = Q_1 Q_0$

$K_0 = 1$ $K_2 = 1$.

⇒ Table for analysis:

	P.S.			FF Inputs			N.S.			
	Q_2	Q_1	Q_0	J_2K_2		J_0K_0	Q_2	Q_1^*	Q_0	
							0	0	0	
(5)	0	0	0	0	1	1 1	0	0	1*	(1)
(1)	0	0	1	0	1	1 1	0	1	0	(2)
(2)	0	1	0	0	1	1 1	0	1	1	(3)
(3)	0	1	1	1	1	1 1	1	0	0	(4)
(4)	1	0	0	0	1	0 1	0	0	0	(0)



"Modulus = 5".

→ If $t_{pd,FF} = 10ns$ → $f_{max} = ?$

Max. conv. time = $10 + 10 = 20ns$.

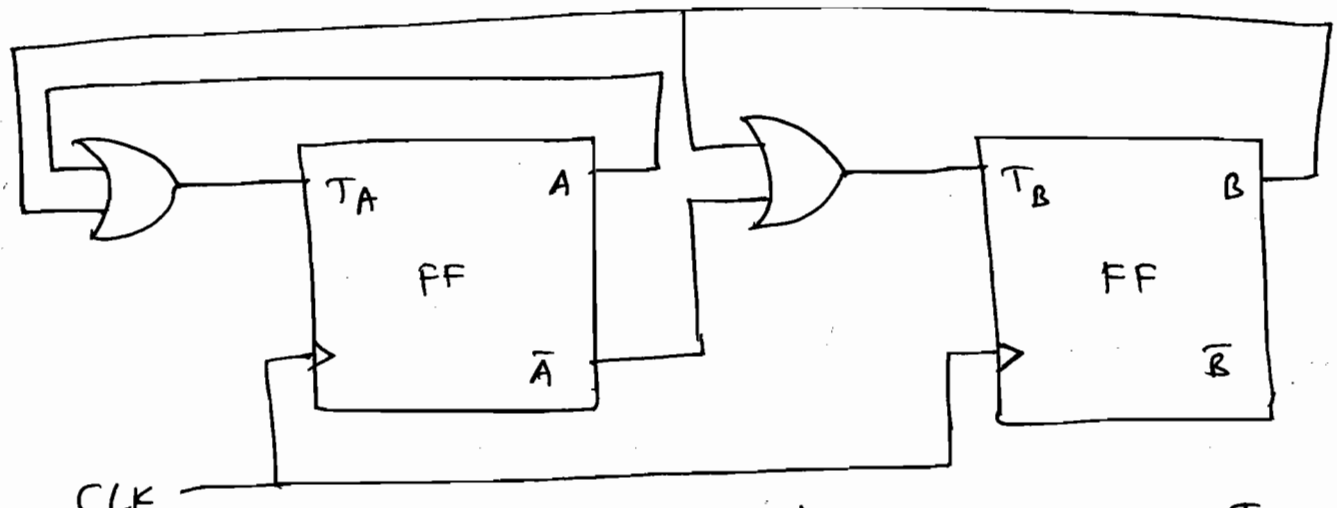
C ∵ FF_0, FF_2 are in synch. mode,
FF_1 is in Async mode].

Clock period $\boxed{T \geq 20ns.}$

$$\therefore f \leq \frac{1}{20 \times 10^{-9}}.$$

$$\therefore \boxed{f_{max} = \frac{1}{20 \times 10^{-9}} \text{ Hz}}$$

Ex-3 Determine the f^n of the following seq. circuit by obtaining its state diagram.

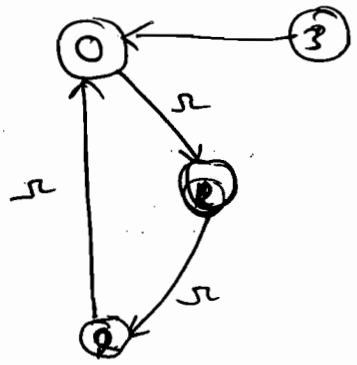


$T_A = A + B$

$T_B = \bar{A} + B$

	P.S.		FF inputs		N.S.		
	A	B	T_A	T_B	A	B	
⓪	0	0	0	1	0	1	①
①	0	1	1	1	1	0	②
②	1	0	1	0	0	0	⓪
③	1	1	1	1	0	0	⓪

State diagram:



→ it is a Mod-3, self starting synchronous counter.

* State Diagram:

Hint:

(i) No of states = 2^N ; N = No of FFs

(ii) No of branches from each state = 2^x;

x = no of direct inputs.

① 2-Bit Up/Down sync Counter:

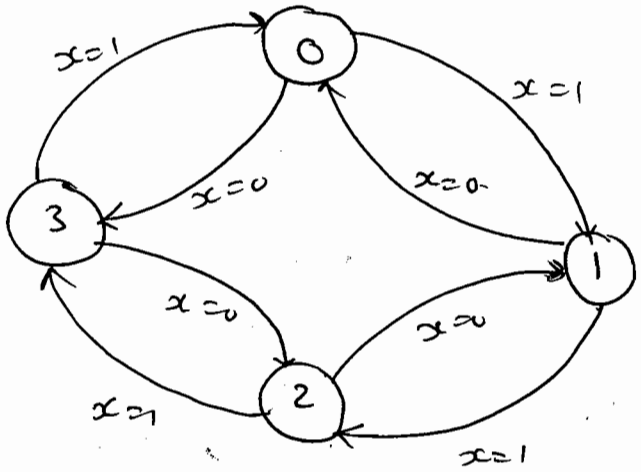
→ 2 FFs ⇒ No. of states = $2^2 = 4$.

(Q_1Q_0 = 00, 01, 10, 11)

↓ ↓ ↓ ↓

0 1 2 3

→ 1 direct i/p (i.e. x) ⇒ No. of branches from each state = $2^1 = 2$.

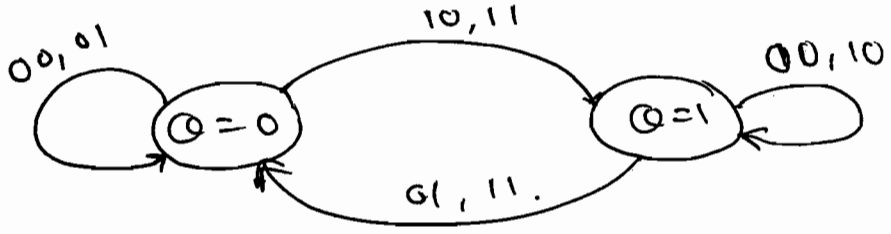


[State Diagram]

(2) J-K FF state diagram:

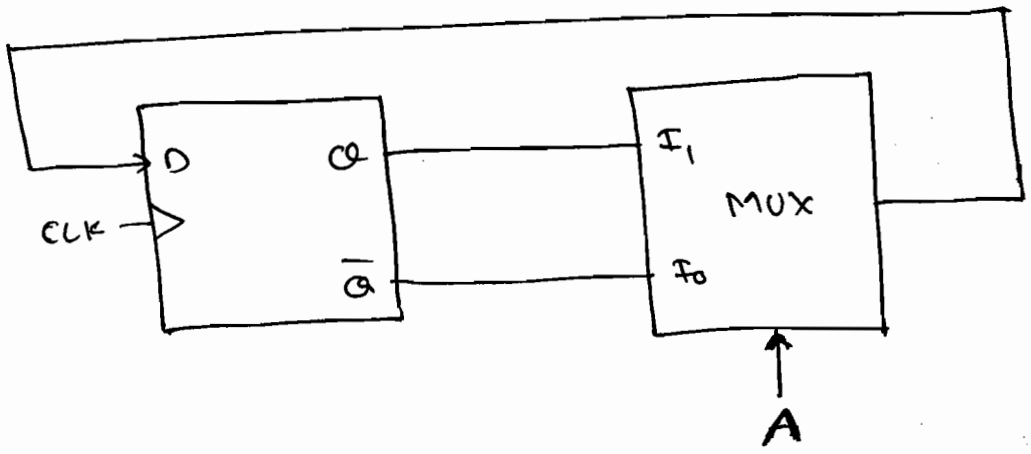
→ 1 FF ⇒ 2 states ($Q=0$, $Q=1$).

→ 2 Direct input ⇒ 4 branches from each state.



Q(t)	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

③ Gate - 2013



→ 1 FF ⇒ 2 States ($Q=0, Q=1$).

→ Input (i.e A) ⇒ 2 branches from each state.

For D-FF → $Q(t+1) = D$ — ①

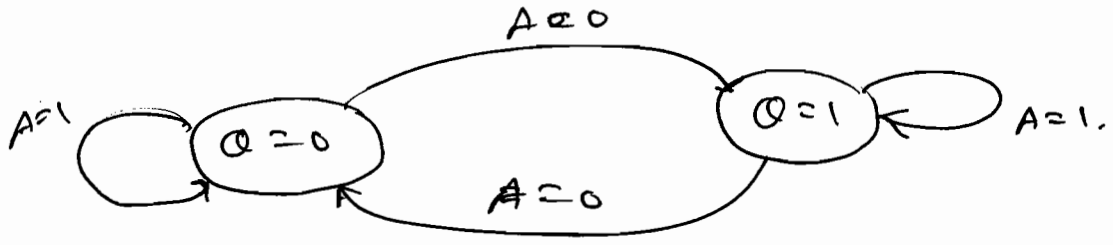
For MUX → $D = \bar{A}\cdot\bar{Q} + AQ$ — ②

from ① & ②

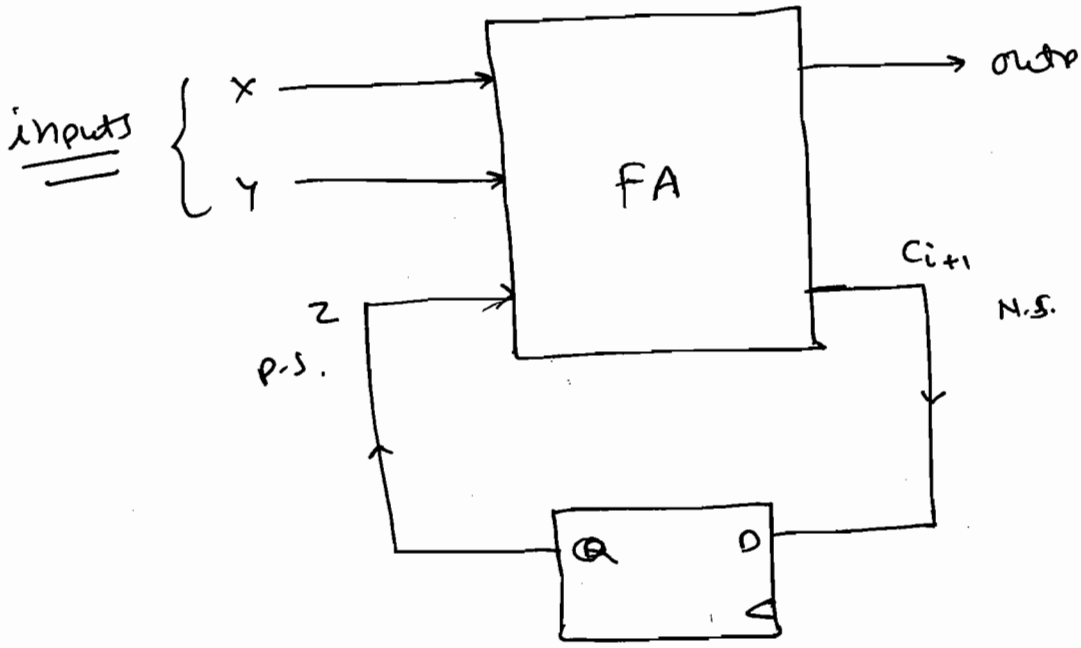
$\therefore$ $Q(t+1) = \bar{A}\cdot\overline{Q(t)} + A\cdot Q(t)$.

When $A=0$, $Q(t+1) = \overline{Q(t)}$

$A=1$, $Q(t+1) = Q(t)$.



(4) Serial Adder State diagram:

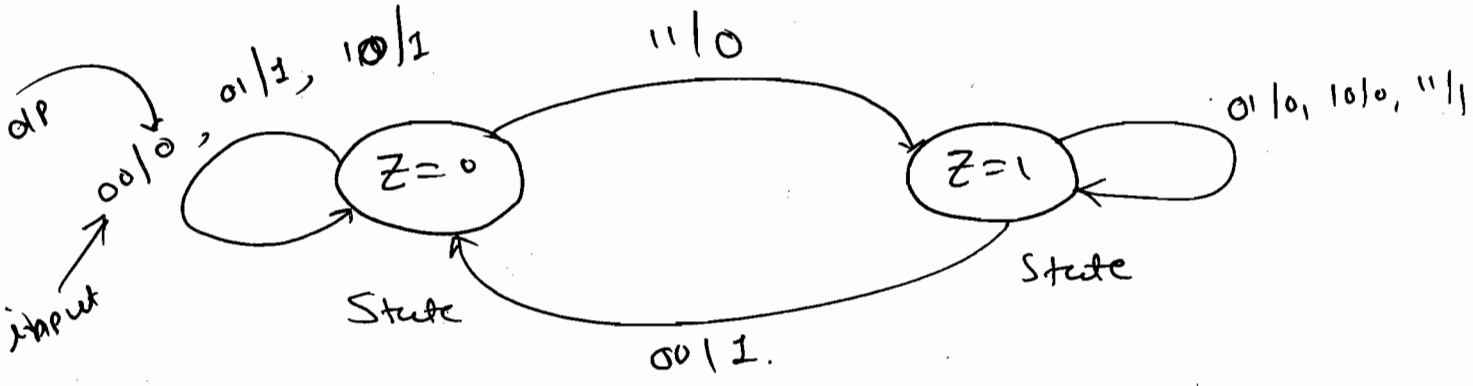


$z = Q = C_{i+1}$
$= Q(t+1)$

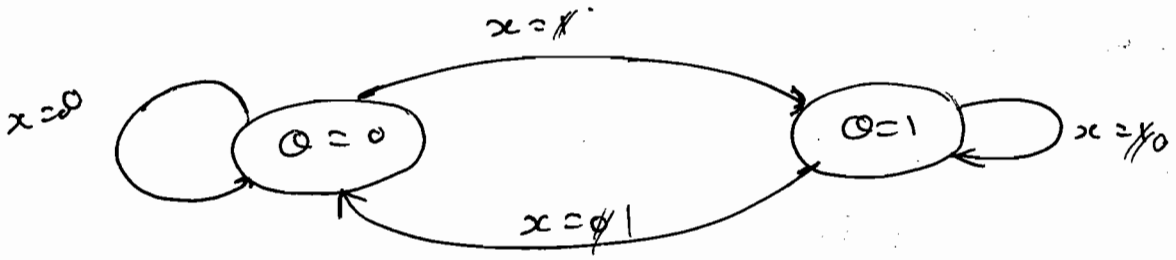
→ 1 FF → 2 states ($z=0, z=1$).

→ 1 input → $2^2 = 4$ branches from each state.

P.S.	input		N.S.	output
(z)	x	y	C_{i+1}	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

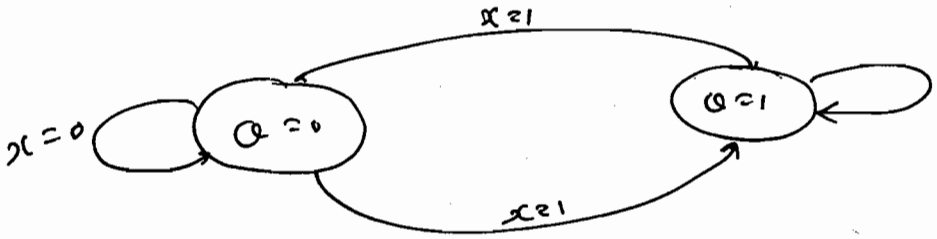


Ex-1 Identify the following FFs.



x	Q(t+1)
0	0
1	1

→ T-FF State diagram

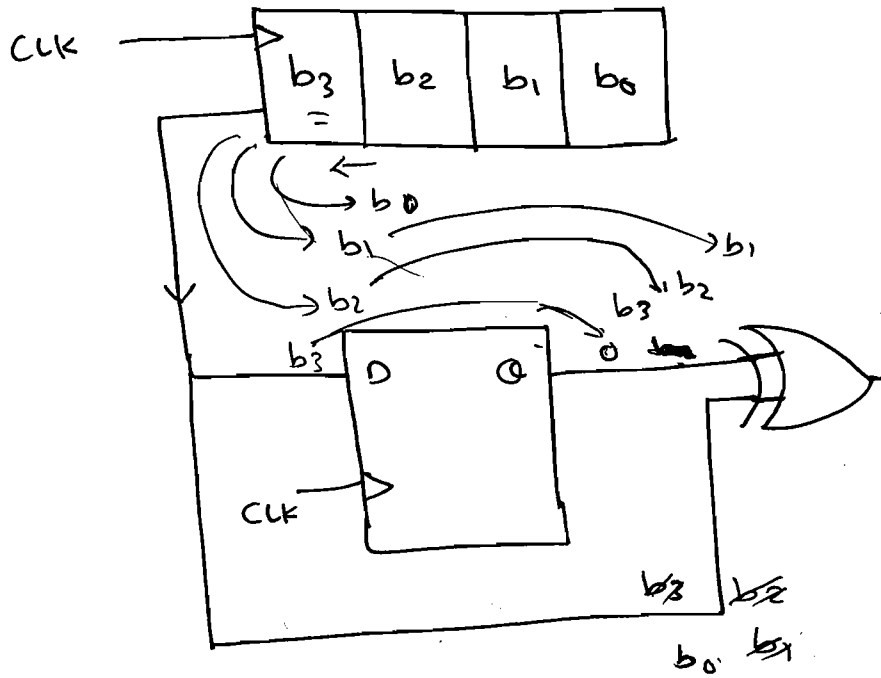


x	Q(t+1)
0	Q(t)
1	$\bar{Q}(t)$

Ex-1 Determine the f^n of the following circuits.

①

Shift left shift Register.



$F_3 = b_3 \oplus 0.$

$F_3 = b_3.$

$F_2 = b_3 \oplus b_2.$

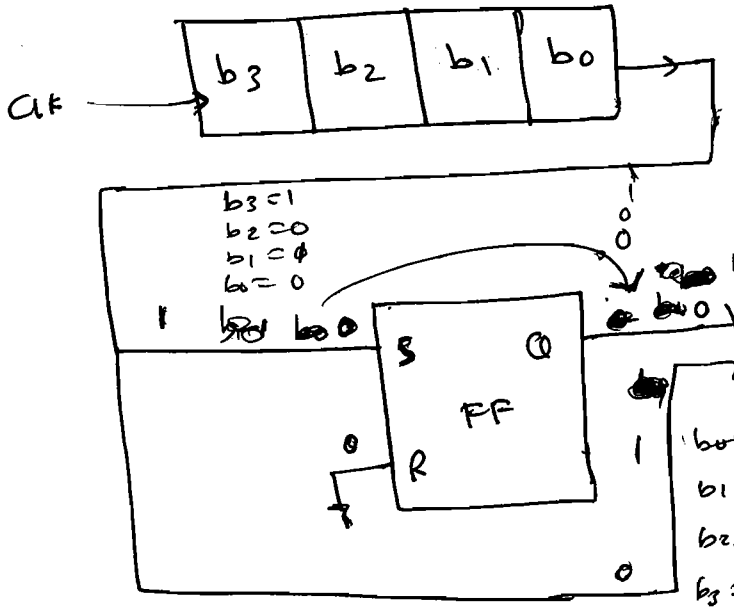
$F_1 = b_2 \oplus b_1$

$F_0 = b_1 \oplus b_0.$

→ Binary to Gray Code Conversion.

②

Shift Right Shift Register



1010
0101
0

$b_0 = 0 \oplus 0 = 0$

$b_1 = 1 \oplus 0 = 1$

$b_2 = 0 \oplus 1 = 1$

$b_3 = 1 \oplus 1 = 0.$

Input = 1 0 1 0

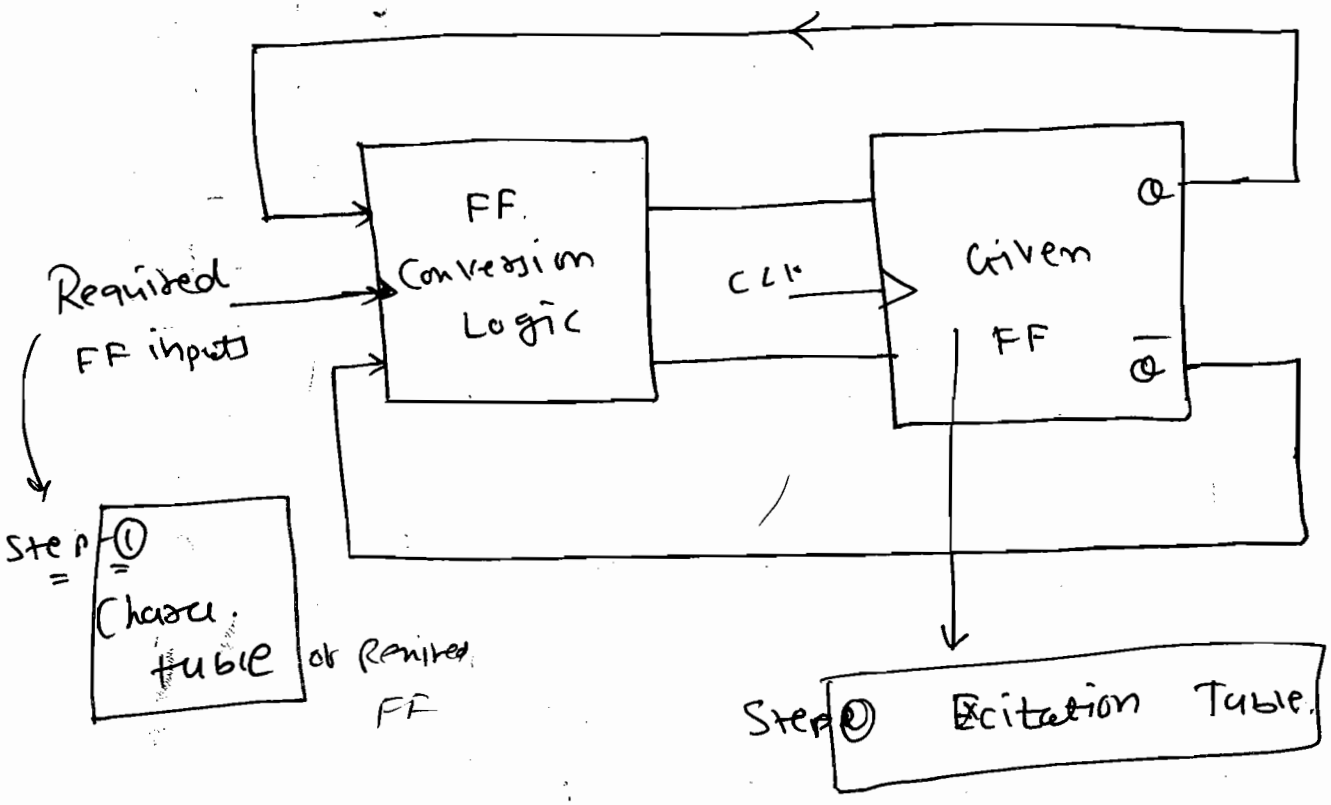
output = 0 1 10

→ It is 2's comp. of binary no.

→ So, it is 2's complement circuit

* Conversion of Flipflops:

⇒ Universal Principle:



Ex-1 Convert S-R FF to T flip flop.

Ans: Step-① → Characteristics table of T-Flip flop.

Step-② → Excitation table of SR flip flop.

T	Q(t)	Q(t+1)	S	R
0	0	0	0	X
0	1	1	X	0
1	0	1	1	0
1	1	0	0	1

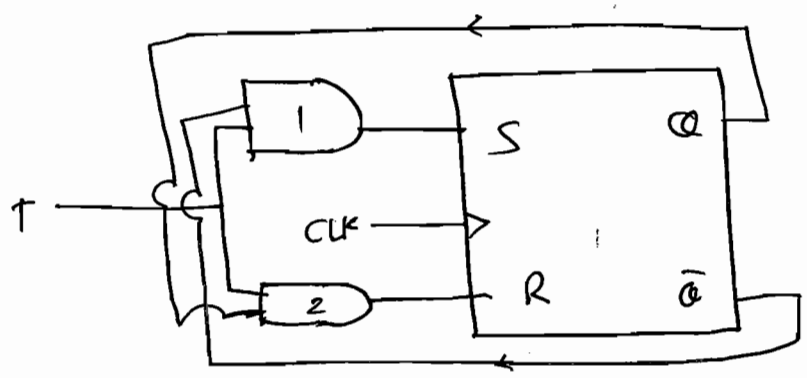
→ ⑤

T \ Q(t)	0	1
0	0	X
1	(1)	0

$S = T\bar{Q}(t)$.

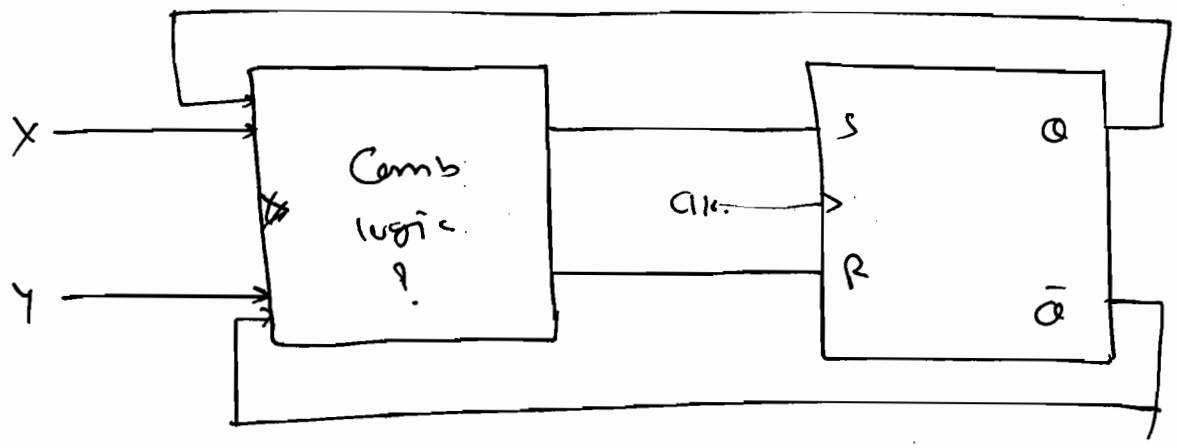
T \ Q(t)	0	1
0	X	0
1	0	(1)

$R = TQ(t)$.



[T- Flip Flop]

Ex. 2 In the following diagram determine the combinational logic to be used.

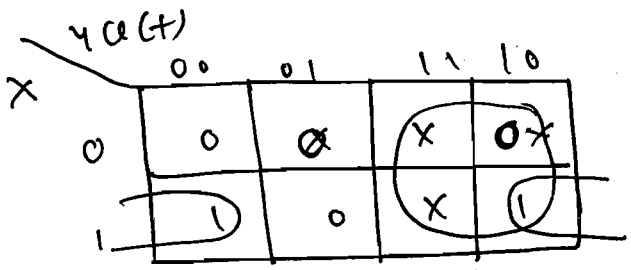


Given:

X Y	Q(t+1)	S R
0 0	0	
0 1	Q(t)	
1 0	$\bar{Q}$(t)	
1 1	1	

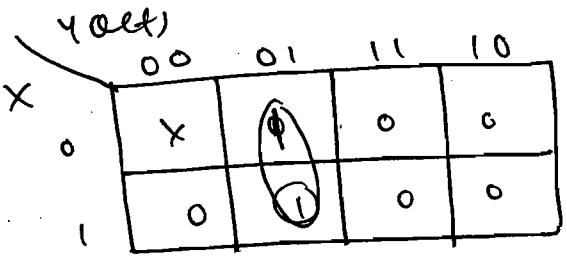
X	Y	Q(t)	Q(t+1)	S	R
0	0	0	0	0	X
0	0	1	0	X 0	0 1
0	1	0	0	0	X
0	1	1	1	X	0
1	0	0	1	1	0
1	0	1	0	0	1
1	1	0	1	1	0
1	1	1	1	X	0

① S



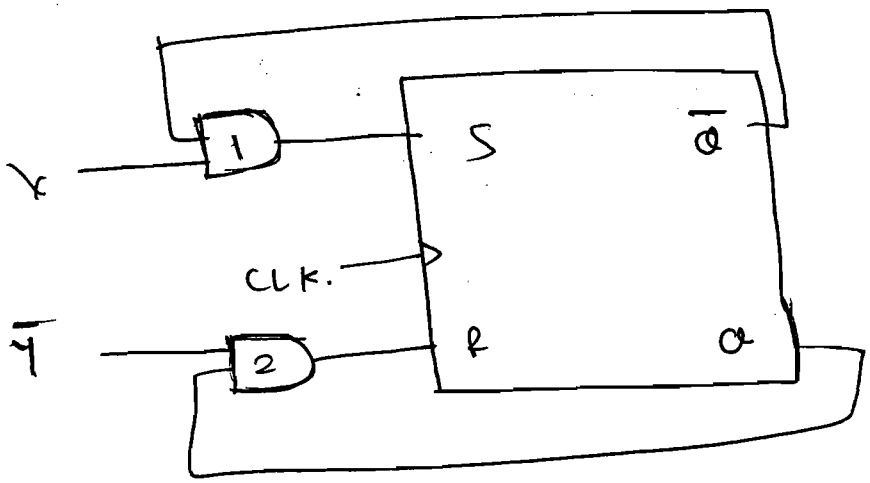
$\therefore \quad S = X\bar{Y}\overline{Q(t)}$

② R

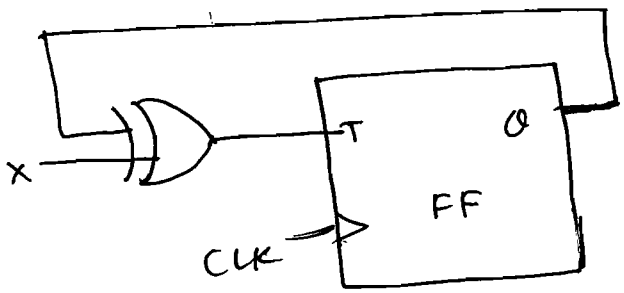


$\therefore \quad R = X\bar{Y}Q(t)$

$R = \bar{Y}Q(t).$



Ex-3 (a) Identify the following flip flop.



$T = x \oplus Q(t) \quad -①.$

For T FF

$T \Rightarrow Q(t+1) = T \oplus Q(t)$

$Q(t+1) = x \oplus Q(t) \oplus Q(t)$

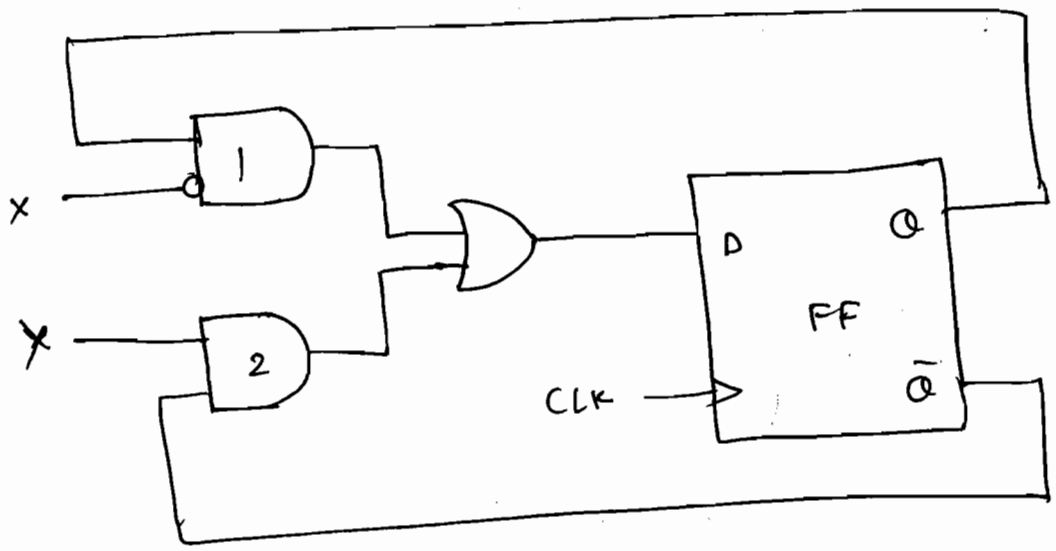
$Q(t+1) = x \oplus 0$

$\boxed{Q(t+1) = x}$

We know ⇒ ③ is similar to D-FF Characteristic equation.

⇒ It is D-Flip Flop.

b)



$D = Q\bar{x} + \bar{Q}y.$

$J\bar{Q}$ $\bar{J}Q(t)$
KQ $K\bar{Q}(t)$.

$\therefore$ $Q(t+1) = Q(t)\bar{x} + \bar{Q}(t)y.$ —③

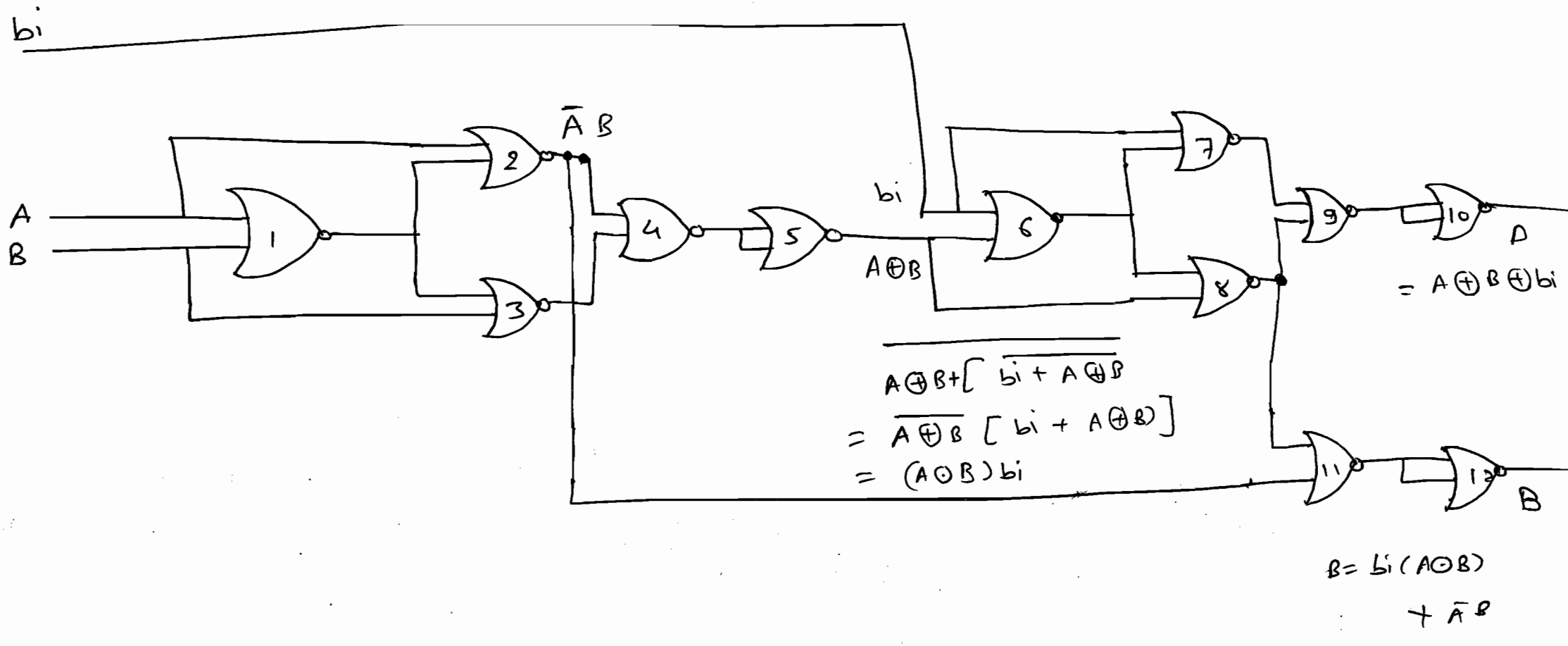
$\therefore$ $Q(t+1) = J\overline{Q(t)} + \bar{K}Q(t).$ —④

So, $\bar{x} = \bar{K}$ $\quad y = KJ$ $\quad X = K$, $Y = J$

$x = J$ $\quad x = k$

So, it is J-K flip flop.

* Full Subtractor using NOR gate only.

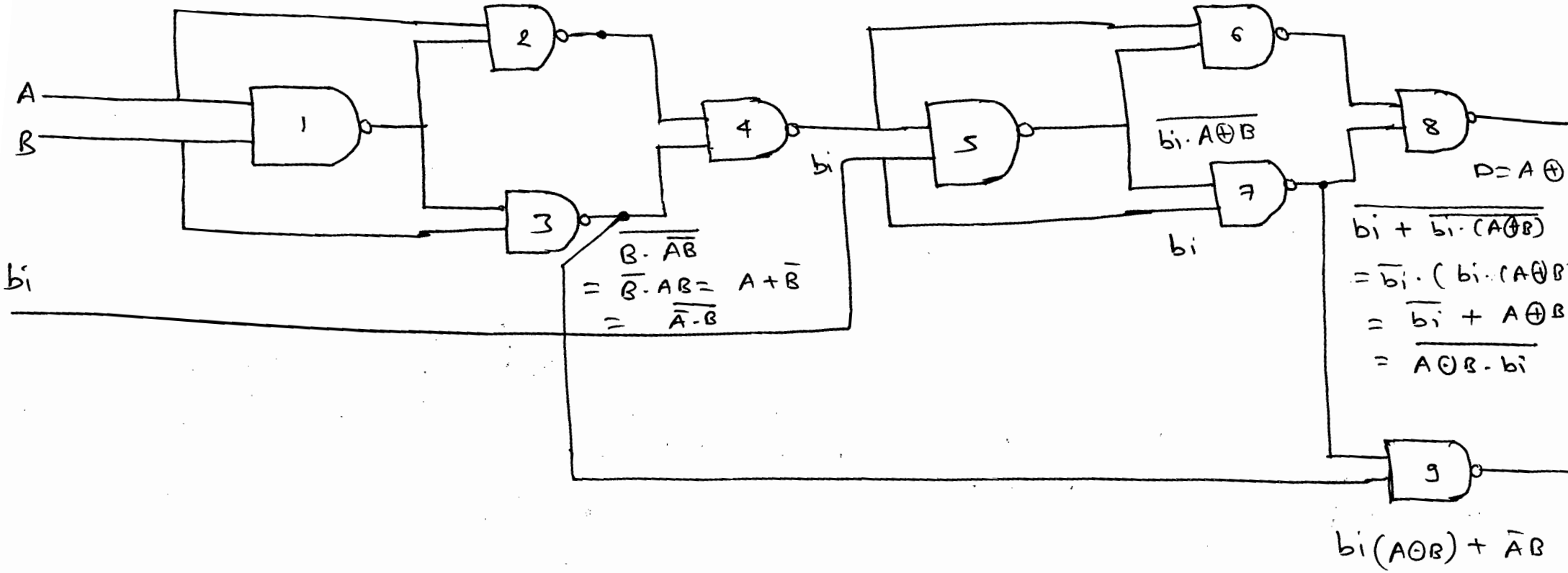


$D = A \oplus B \oplus bi$

$B = bi(A \odot B) + \bar{A}B$

* Full Subtractor using NAND gate only:

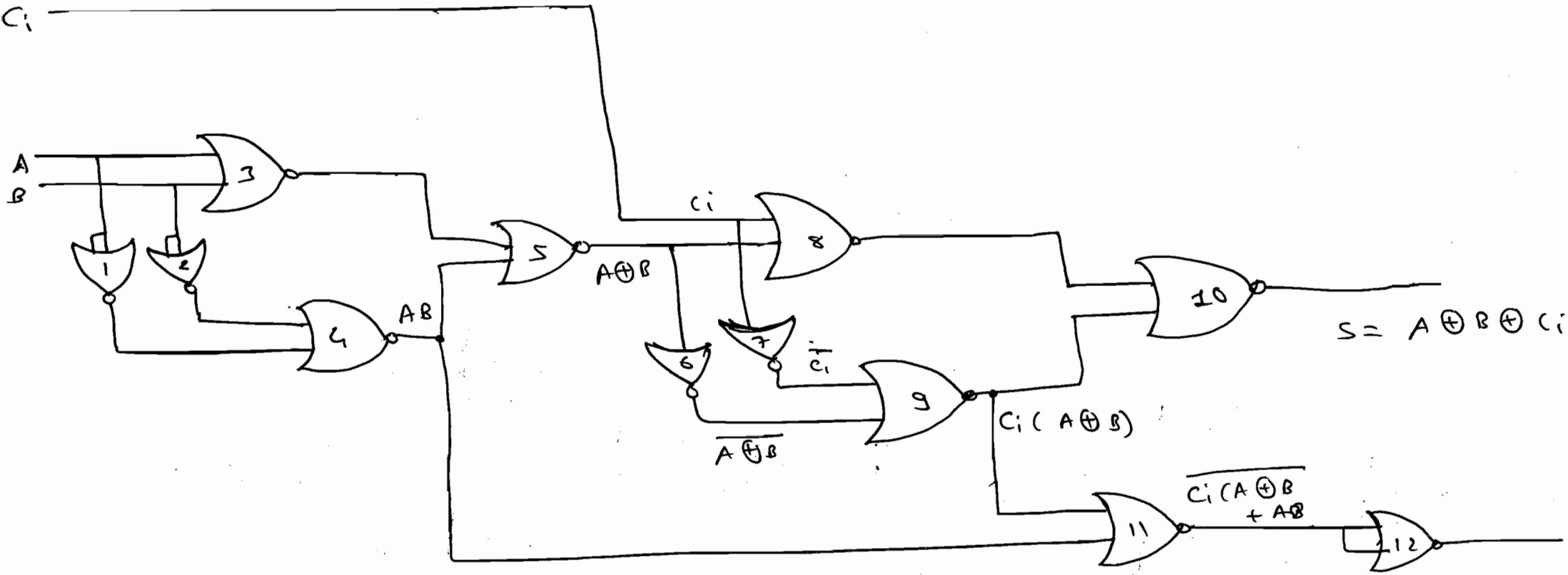
$$\overline{A \cdot \overline{AB}} = \overline{\bar{A} + AB} = \bar{A}B$$
$$= \overline{A\bar{B}}$$



$$D = A \oplus B \oplus bi$$

$$B = bi(A \odot B) + \bar{A}B$$

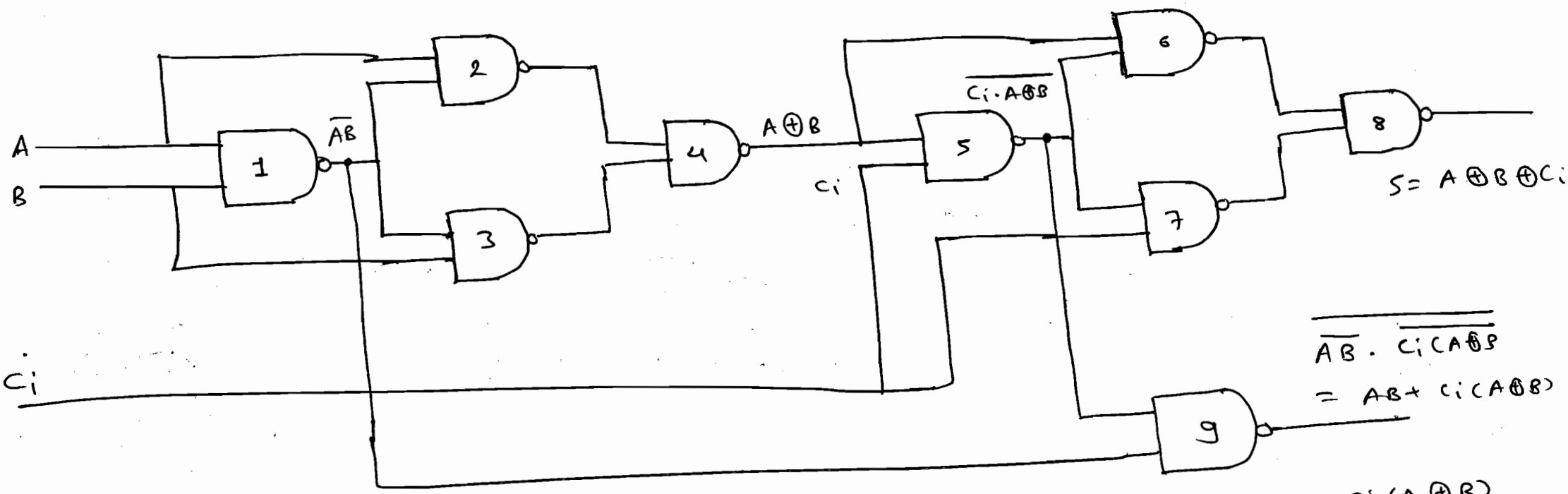
* Full Adder using NOR gate only:



$S = A \oplus B \oplus C_i$

$C_{i+1} = C_i (A \oplus B) + AB$

* Full adder using NAND gate only



$S = A \oplus B \oplus C_i$

$C = C_i \cdot (A \oplus B) + AB$