

# Chapter 6

## Microprocessor 8085

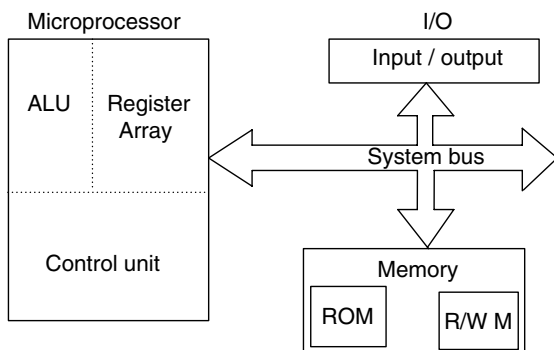
### CHAPTER HIGHLIGHTS

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- ☞ Microprocessor 8085
- ☞ Instructions Classifications
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A microprocessor is a programmable integrated device that has computing and decision-making capability similar to that of the central processing unit (CPU) of the computer.

The microprocessor communicates and operates in the binary numbers 0 and 1 called bits. Each microprocessor has a fixed set of instruction in the form of binary patterns called machine language to make it easier to understand the binary instructions that are given abbreviated names called mnemonics, which form the assembly language for a given microprocessor.

### ORGANIZATION OF MICROPROCESSOR-BASED SYSTEM



Microprocessor-based systems include three components: microprocessor, input/output (I/O), and memory. These components are organized around a common communication path called bus.

### Microprocessor

The microprocessor is a clock-driven semiconductor device consisting of electric logic circuits manufactured by using either LSI or VLSI technique.

### Arithmetic Logic Unit

The ALU unit performs arithmetic operations as addition, subtraction, and logic operations such as AND, OR, and exclusive OR.

### Register Array

Microprocessor consists of various registers identified by B, C, D, E, H, and L. These registers are primarily used to store data temporarily during the execution of a program.

### Control Unit

The control unit provides the necessary timing and control signals to all the operations in the micro-computer.

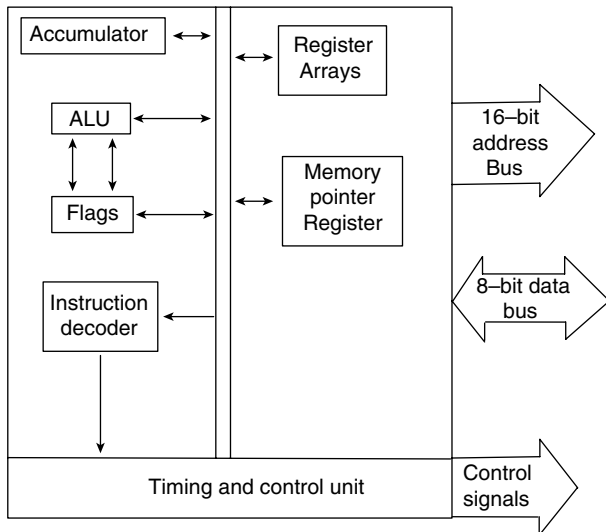
## MICROPROCESSOR 8085

### Registers

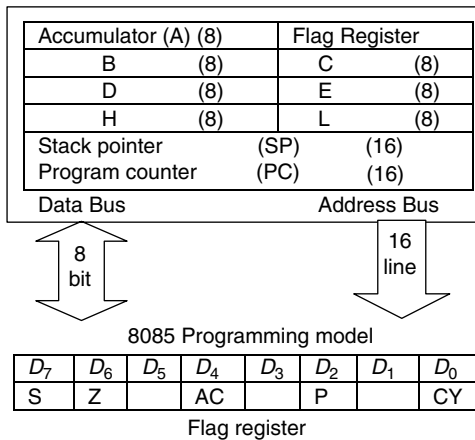
The 8085 has six general purpose registers to store 8-bit data; these are identified as B, C, D, E, H, and L, and they can be combined as register pairs BC, DE, and HL to perform some 16-bit operations.

### Accumulator

It is an 8-bit register, part of ALU, and the result of an operation is stored in the accumulator. It is also identified as register A.



8085 hardware model



## Flags

The ALU includes five flip-flops; these flags are set or reset after the execution of an arithmetic or logic operation.

1. Z – zero flag is set to 1 when result is zero, otherwise it is reset.
2. CY – carry flag is set if an arithmetic operation results in carry or borrow, otherwise reset.

3. S – sign flag is set if bit D<sub>7</sub> (MSB) of the result is 1, otherwise reset.
4. P – parity flag is set, if result has an even number of 1's; for odd number of 1's, the flag is reset.
5. AC – auxiliary carry flag is set, when (in arithmetic operation) a carry is generated by digit D<sub>3</sub> and passed to D<sub>4</sub> (carry transition from lower nibble to higher nibble). This flag is used internally for BCD operations.

## Program Counter (PC) and Stack Pointer (SP)

These are two 16-bit registers used to hold memory addresses.

The function of a program counter is to point to memory address from which the next byte is to be fetched and executed. When a byte (machine code) is being fetched, the program counter is incremented by one to point to the next memory location.

Stack pointer points to a memory location in R/W memory called stack. The beginning of the stack is defined by loading a 16-bit address in the stack pointer.

## INSTRUCTIONS CLASSIFICATIONS

An instruction is a binary pattern designed inside a microprocessor to perform a specific function. The entire group of instructions, called instructions set, determines what functions the microprocessor can perform.

## Data Transfer (Copy) Operations

These instructions perform the following six operations:

1. Load an 8-bit number in a register
2. Load 16-bit number in a register pair
3. Copy from register to register
4. Copy between register and memory
5. Copy between I/O and accumulator
6. Copy between registers and stack memory

Mnemonics	Operations
MVI Reg., 8 bit	Load 8-bit data in a register
MOV Rd, Rs	Copy data from source (Rs) to destination (Rd) register
LXI Rp, 16 bit	Load 16-bit num in a register pair (Rp)
OUT 8 bit (port addr)	Send data byte from accumulator
IN 8 bit (port Addr)	Accept data byte from Input device into accumulator
LDA 16 bit	Load accumulator with data from 16-bit memory address
STA 16 bit	Store contents of A in 16-bit memory address
LDAX Rp	Load 'A' with data from memory address specified by (Rp) register pair
STAX Rp	Store data in A into the memory location specified by (Rp)
MOV R, M	Copy the data byte into register (R) from the memory specified by the address by HL pair
MOV M, R	Copy data byte into memory specified by HL pair from the register (R)

## Arithmetic Instructions

The frequently used arithmetic operations are add, subtract, increment, and decrement; the result will be stored in accumulator.

Mnemonics	Operation
ADD R	Add contents of Reg to contents of A
ADI 8 bit	Add 8-bit data to contents of A
ADD M	Add the contents of memory (in HL reg) to A
SUB R	Subtract the contents of Reg from contents of A
SUI 8 bit	Subtract 8-bit data from contents of A
SUB M	Subtract the contents of memory HL from A
INR R/M	Increment Reg/contents in memory (specified in HL) by 1
DCR R/M	Decrement Reg/contents in memory (specified in HL) by 1
INX Rp	Increment the contents of register pair by 1
DCX Rp	Decrement the contents of register pair by 1

## Logic and Bit Manipulation Instructions

These instructions include the following operations AND, OR, EX-OR, and compare rotate bits and the result will be stored in accumulator.

Mnemonic	Operations
ANA R/M	Logically AND the contents of Reg/memory with contents of A
ANI 8 bit	Logically AND 8-bit data with A
ORA R/M	Logically OR the contents of Reg/memory with contents of A
ORI 8 bit	Logically OR 8-bit data with A
XRA R/M	Ex-OR The contents of a register/memory with A
XRI 8 bit	Ex-OR The contents of 8-bit data with A
CMP R	Compare the contents of R with A
CPI 8 bit	Compare 8-bit data with A
CMA	Complement accumulator

## Branch Instructions

The following instructions change the program sequence

Mnemonics	Operation
JMP 16-bit address	unconditional change the program sequence to specified address
JZ 16-bit address	change the program sequence to specific address if zero flag is set
JNZ 16-bit address	if zero flag is reset change program sequence
JC 16-bit address	if carry flag is set change the program sequence
JNC 16-bit address	change program sequence if carry flag is reset

(Continued)

Mnemonics	Operation
CALL 16-bit address	change the program sequence to the location of a subroutine specified
RET	return to the called program after subroutine sequence

## Machine Control Instructions

These instructions affect the operation of the processor:

HLT – stop processing and wait

NOP – do not perform any operation

In data transfer, the contents of the source are not destroyed, only the contents of the destination are changed. However, the data copy instructions do not affect the flags.

Arithmetic and logical operations are performed with the contents of accumulator and results are stored in the accumulator

## Instruction Word Size

### One-byte Instructions

These include OP code and operand in the same byte; each instruction requires one- byte memory space

For example, MOV C, A; ADD B; CMA

Mnemonic followed by letters representing register or memory.

### Two-byte Instructions

The first byte specifies the operation code and the second byte specifies operand. A mnemonic is followed by 8 bit. For example, MVI A, 32H; MVI B, F2H;

These instructions would require two memory locations.

### Three-byte Instructions

These instructions would require three memory locations, each to store the binary codes. The first byte specifies the op code, and the following two bytes specify the 16-bit address, the second byte is the low order address, and third byte is the high order address.

These instructions have mnemonic followed by 16 bit:

Ex:

LDA 2050H	3A first byte (op code) 50 second byte 20 third byte
JMP 2085H	C3 first byte (op code) 85 second byte 20 third byte

An instructions has two parts: OP code (operation to be performed) and operand (data to be operated on).

The operand can be data (8- or 16-bit), address or register or it can be implicit.

The method of specifying an operand (directly or indirectly, etc.) is called the addressing mode.

## Operations in Microprocessor

The microprocessor (MPU) primarily performs four operations

1. memory read
2. Memory write
3. I/O read
4. I/O write

For each operation, it generates the appropriate control signals. To communicate with a peripheral (and memory), the MPU identifies the location by its address, transfers data, and provides timing signals.

The 8085 microprocessor has 16 address lines, 8 data lines, and control bus to provide timing of various operations. The 8085 can respond to four externally initiated operations: reset, interrupt, ready, and hold.

Memory is a group of registers arranged in a sequence to store bits. The 8085 MPU requires an 8-bit wide memory word and uses 16-bit address to select a memory location. The memory addressing assigned to a memory chip in a system is called the memory mapping.

The assignment of memory address is done through the chip select logic.

Memory can be classified into two groups:

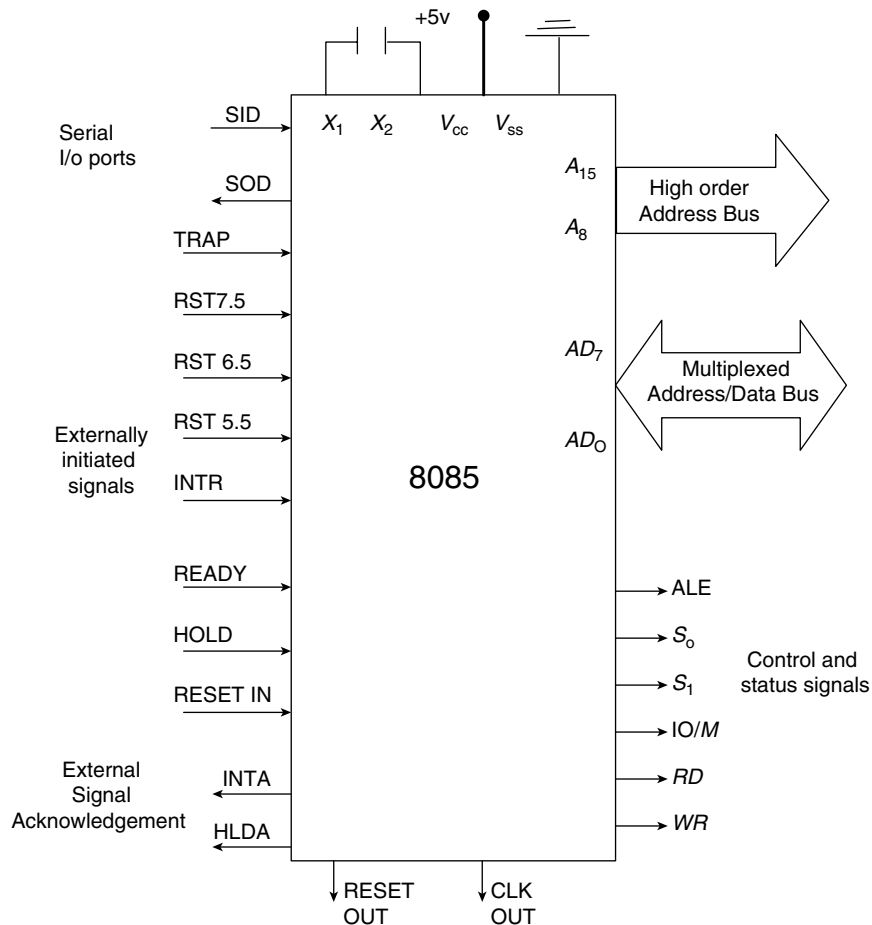
1. Read/write memory is volatile and can be used to read and write information; this is also called user memory.
2. The ROM is a non-volatile memory and the information written into this memory is permanent.

Input/output devices or peripherals can be interfaced with 8085 in two ways.

## Peripheral I/O and Memory-mapped I/O

In peripheral I/O, the MPU uses an 8-bit address to identify an I/O, and IN and OUT instructions for data transfer. In memory-mapped I/O, the MPU uses a 16-bit address to identify an I/O and memory related instructions for data transfer.

To execute an instruction, the MPU places the 16-bit address on the address bus, sends the control signal to enable the memory chip, and fetches the instruction. The instruction is then decoded and executed.



The 8085 microprocessor signals

## 8085 SIGNALS

8085 is an 8-bit general purpose microprocessor. Addressing capacity is 64 kB. It is an integrated circuit with 40 pins and uses a +5 V power supply. It operates at 3 MHz single-phase clock. (8085 A-2 version can operate at the maximum frequency of 5 MHz.)

The signals of 8085 microprocessor, classified into six groups:

- Address bus:** The 8085 has 16 lines ( $A_{15}$  to  $A_8$ ) and ( $AD_7$  to  $AD_0$ ) as address bus. High order address lines are unidirectional, and low order address lines ( $AD_7$  to  $AD_0$ ) are used for data and low order address bus.
- Data bus:** The signal lines ( $AD_7$  to  $AD_0$ ) are bidirectional. In executing an instruction, during earlier part of the cycle, these lines are used as the lower address bus. During the latter part of the cycle, these lines are used as data bus.
- Control and status signals:**
  - ALE:** Address latch enable is active high signal generated every time the 8085 begins an operation. Machine Cycle: It indicates the bits  $AD_7$  to  $AD_0$  are address bits.
  - $\overline{RD}$ :** Read is the active low signal indicating the selected IO/memory device to be read and data are available on data bus.
  - $\overline{WR}$ :** Write is the active low signal indicating the data available on data bus, which are to be written into a selected memory or I/O.
  - $IO/\overline{M}$ :** This signal used to indicate IO (1) or memory (0) operation.
  - $S_1$  and  $S_0$ :** These status signals can identify various operations as per the following table.

Machine cycle	$IO/\overline{M}$	$S_1$	$S_0$	Control signals
op code fetch	0	1	1	$\overline{RD}=0$
Memory read	0	1	0	$\overline{RD}=0$
Memory write	0	0	1	$\overline{WR}=0$
I/O read	1	1	0	$\overline{RD}=0$
I/O write	1	0	1	$\overline{WR}=0$
Interrupt acknowledge	1	1	1	$\overline{INTA}=0$
Halt	Z	0	0	$\overline{RD}, \overline{WR}=Z, \overline{INTA}=1$
Hold	Z	X	X	$\overline{RD}, \overline{WR}=Z$
Reset	Z	X	X	$\overline{INTA}=1$

### 4. Power supply and clock frequency:

- $V_{CC}$ : +5 V power supply,  $V_{SS}$ : ground
- $X_1, X_2$ : A crystal (RL or RC) is connected between these two pins, and the frequency is internally divided by two.
- Clk (out): This is the system clock for other devices.

### 5. Externally initiated signals:

$\overline{INTR}$  (input): general purpose interrupt request.

$\overline{INTA}$  (output): interrupt acknowledgement

$RST\ 7.5$ :- Restart interrupts, vectored interrupts,  
 $RST\ 6.5$ :- That transfer the program control to  
 $RST\ 5.5$ :- Specific memory location (8x)

TRAP (input): non-maskable interrupt with the the highest priority.

HOLD (input): This signal indicates that a peripheral like DMA is requesting the use of address/data bus.

HLDA (output): Hold request acknowledgement.

READY (input):- When this signal goes low, microprocessor waits for an integral number of clock cycles until it goes high.

$\overline{RESET\ IN}$ : When the signals goes low, PC is set to zero, the buses are tri-stated, and microprocessor is reset.

RESET OUT: This signal indicates that MPU is being rest and used to rest other devices.

### 6. Serial IO ports:

SID – serial input data,

SOD – serial output data.

The 8085 microprocessor has a multiplexed bus  $AD_7$  to  $AD_0$  used as low order address bus and the data bus.

The bus  $AD_7$  to  $AD_0$  can be demultiplexed by using a latch and the ALE signal. The 8085 has a status signal  $IO/\overline{M}$  and two control signals  $\overline{RD}, \overline{WR}$ ; by ANDing these signals, four control signals can be generated  $\overline{MEMR}, \overline{MEMW}, \overline{IOR}, \overline{IOW}$

To execute an instruction, the MPU

- places the memory address of instruction on address bus.
- indicates the operation status on the status lines.
- sends  $\overline{MEMR}$  control signal to enable the memory, fetches the instruction byte, and places it in the instruction decoder.
- executes the instruction.
- each instruction of 8085 microprocessor can be divided into a few basic operations called machine cycles, and each machine cycle can be divided into T-states.

The frequently used machine cycles are Opcode fetch, memory read and write, and I/O read and write. When 8085

performs any of the operations, it asserts the appropriate control signal and status signal.

The Opcode fetch and the memory read are operationally similar, and the 8085 reads from memory in both machine cycles. However, the 8085 reads Opcode during the Opcode fetch cycle, and it reads 8-bit data during the memory read cycle. In the memory write cycle, the processor writes data into memory.

The 8085 performs three basic steps in any of these machine cycles: it places the address on address bus, sends appropriate control signals, and transfers data via data bus.

## 8085 Machine Cycles and Bus Timings

1. **Instruction cycle:** It is the time required to complete the execution of an instruction; one instruction cycle consists of 1 to 6 machine cycles.
2. **Machine cycle:** It is the time required to complete one operation like accessing memory or IO or acknowledging external request. This cycle may consist of 3 to 6 T-states.
3. **T-states:** It is the part of the operation performed in one clock period. Each T-state is exactly equal to one clock period.

In each instruction cycle, the first operation is always opcode fetch, and this cycle can be of four to six T-states duration.

Memory read is similar to opcode fetch but requires 3 T-states, and these two are differentiated by the status signals.

Memory write cycle consists of 3 T-states, I/O read or I/O write consists of 3 T-states, and interrupt acknowledgement machine cycle consists of 6 T-states.

Consider instruction STA 2016H → store accumulator contents in memory location 2016H.

This instruction includes the op code fetch and memory read machine cycles to read address 2016H, and then memory write machine cycle. A total of four machine cycles, and it is a 3-byte instruction.

Total T-states = opcode fetch + memory read + memory read + memory write =  $4 + 3 + 3 + 3 = 13$  T-states.

Consider another instruction OUT 20H → transfer the data from accumulator to output device at 20H.

This instruction consists of op code fetch, memory read (reading 20H), and I/O write.

Total T-states =  $4 + 3 + 3 = 10$  T-states

Consider CALL 2006H instruction. This instruction is a 3-byte instruction, which takes the program control to the address specified 2006H and it stores the address of next instruction on the top of stack, so that RET instruction can take execution to previous program.

Therefore, call instruction consists of five machine cycles. Op code fetch + Memory read + Memory read + Memory write + Memory write (storing program counter) =  $4 + 3 + 3 + 3 + 3 = 18$  T-states

To interface a memory chip with 8085, the necessary low order address lines of the 8085 address bus are connected to the address lines of the memory chip.

The high order address lines are decoded to generate  $\overline{CS}$  signals to enable the chip. In the absolute decoding technique, all the address lines that are not used for the memory chip to identify a memory register must be decoded. Thus, the chip select can be asserted by only one address. In the particular decoding technique, same address lines are left don't care. This technique reduces hardware. However, it generates multiple address resulting in foldback memory space.

## Peripheral-mapped I/O

A latch is commonly used to interface output devices. A tristate buffer is commonly used to interface input devices. To interface an output or an input device, the low order address bus  $A_7$  to  $A_0$  (or high order bus) needs to be coded to generate the device address pulse, which must be combined with the control signal ( $IOR$  or  $IOW$ ) to select the device.

## Memory-mapped I/O

Memory related instructions are used to transfer data. To interface I/O device, the entire bus must be decoded to generate the device address pulse, which must be combined with the control signal  $MEMR$  or  $MEMW$  to generate the I/O select pulse. This pulse is used to enable the I/O device and transfer the data.

## Memory Interfacing

The primary function of memory interfacing is that the microprocessor should be able to read and write into a given register of a memory element. To perform read/write operation with memory, the microprocessor should.

1. be able to select the chip (through  $\overline{CS}$ )
2. identify the register (using address bus)
3. enable read/write operation (using  $\overline{RD}$  or  $\overline{WR}$  signals)

## Address Decoding and Memory Addresses

The process of address decoding should result in identifying a register for a given address. We should be able to generate a unique pulse for a given address.

Let us consider  $4\text{ k} \times 8$  R/W memory has to interface with 8085 microprocessor.

Microprocessor uses 16-bit address, but  $4\text{ k} \times 8 = 2^{12} \times 8$  memory uses 12-bit address ( $A_{11}$  to  $A_0$ ).

To interface with microprocessor, lower order address ( $A_{11}$  to  $A_0$ ) are connected to memory chip and remaining four address lines ( $A_{15}$  to  $A_{12}$ ) of 8085 microprocessor must be decoded, and this can be done by a gate/decoder/demultiplexer.



Therefore, the range of address for the R/W memory is

$$\begin{array}{cccccccccccccccccccccccc}
 A_{15} & A_{14} & A_{13} & A_{12} & A_{11} & A_{10} & A_9 & A_8 & A_7 & A_6 & A_5 & A_4 & A_3 & A_2 & A_1 & A_0 \\
 1 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 & & & & & & & & & & & & & & & = 8C00H \\
 1 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
 \underbrace{\hspace{1.5cm}} & \underbrace{\hspace{1.5cm}} & & & & & \underbrace{\hspace{4.5cm}} \\
 \text{Decoder 1} & \text{Decoder 1} & & & & & \text{Address lines of } 1k \times 8
 \end{array}$$

Range of address for ROM1 = 2000 H – 3FFFH

Range of address for ROM2 = C000H – DFFFH

Range of address for R/w M1 = 8C00H – 8FFFH

## Peripheral I/O Instructions

The I/O devices such as key boards and displays can be interfaced with 8085 microprocessor with 8-bit addresses in peripheral-mapped I/O. In memory-mapped I/O, 16-bit address will be used and memory related instructions for peripheral-mapped I/O 8-bit address will be used.

IN 8 bit Port Adder → This is 2-byte instruction, which transfers the data from input port to accumulator.

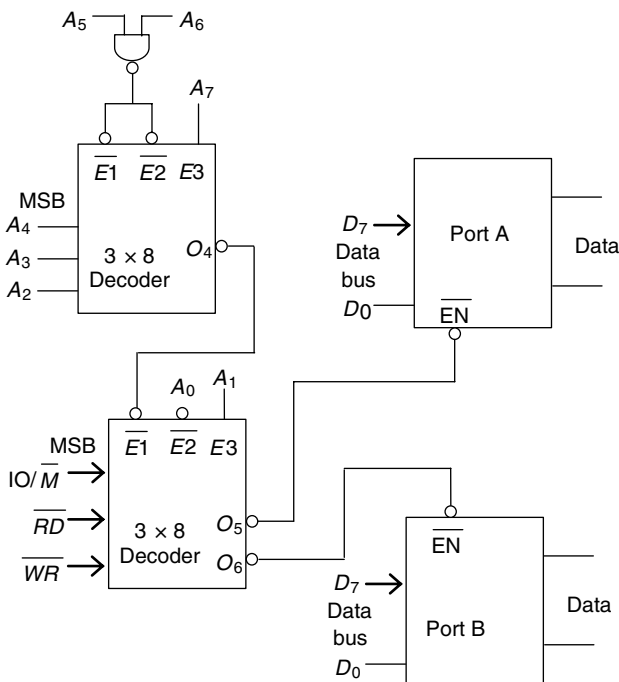
OUT 8 bit Port Adder → This is a 2-byte instruction, which transfers the data from accumulator to output port.

When an I/O instruction is executed, the 8085 micro-processor places the device address (port number) on the demultiplexed low order as well as high order address bus.

Address can be decoded to generate the pulse corresponding to the device address on the bus, and it will be added with appropriate signal  $\overline{IOR}$  or  $\overline{IOW}$ . Further, when both signals asserted, the I/O port is selected.

## Example 2

In the following I/O interfacing circuit, identify ports A and B as input or output ports and addresses of the ports? Further, find the instruction to be used.



## Solution

Two ports port A and port B are connected in the abovementioned figure with two decoders.

First decoder  $O_4$  is used to enable  $(\overline{E1})$  second decoder, and therefore,  $A_4 A_3 A_2 = 100$ . — —

First decoder will be enabled if  $\overline{E1} \overline{E2} E3 = 001$ , and therefore  $A_5 A_6 = 11$  (NAND output = 0),  $A_7 = 1$ .

Second decoder will be enabled  $\overline{E2} \ E3 = 01$ .

Therefore,  $A_1 = 1, A_0 = 0$

The address of the port is

$$\begin{array}{cccccccc} A_7 & A_6 & A_5 & A_4 & A_3 & A_2 & A_1 & A_0 \\ 1 & 1 & 1 & 1 & 0 & 0 & 1 & 0 \end{array} = \text{F2H}$$

Therefore, both port A and port B will have same address F2H. However, if we select IO Read operation,

IO/ $\overline{M}$  = 1,  $\overline{RD}$  = 0, and  $\overline{WR}$  = 1 are the inputs for the second decoder. Therefore,  $O_5$  will be selected, and port A is used for IO Read operation. IN F2H is the instruction for port A (input).

For IO write operation,  $\overline{IO/M} = 1$ ,  $\overline{RD} = 1$ , and  $\overline{WR} = 0$ , that is, 110, are the inputs for decoder. Therefore,  $O_6$  will be selected output, and hence, port B will be enabled for write operation.

OUT F2H is the instruction for output port B.

### Comparison between memory mapped I/O and peripheral I/O

Memory-mapped I/O		Peripheral I/O	
(1)	Device address is 16 bit.	(1)	Device address is 8 bit.
(2)	$\overline{MEMR}/\overline{MEMW}$ control signals for input/output.	(2)	$\overline{IOR}/\overline{IOW}$ control signals for input/output.
(3)	The memory map (64k) is shared between I/Os and system memory.	(3)	I/O map is independent of the memory map, 256 input devices and 256 output devices can be connected.
(4)	More hardware needed to decode 16-bit memory address; however, arithmetic/logical operations can be performed.	(4)	Less hardware needed to decode 8-bit address; however, arithmetic and logical operations not available.

## ADDITIONAL INSTRUCTIONS

## Additional Jump Instructions

JP 16 bit	Jump on plus (if D7 = 0 and S = 0)
JM 16 bit	jump on minus (if D7 = 1 and S = 1)
JPE 16 bit	jump on even parity ( $p = 1$ )
JPO 16 bit	jump on odd parity ( $p = 0$ )

### Additional data transfer and 16-bit arithmetic instructions

LXI, Rp, 16 bit	load reg. pair immediate
LDAX B/D	load accumulator indirect

(Continued)

LDA 16 bit	load accumulator direct
STAX B/D	store accumulator indirect
STA 16 bit	store accumulator direct
INX Rp,	increment register pair
DCX RP,	decrement register pair.

Logic operation: Rotate

RLC:	Rotate accumulator left
RAL:	Rotate accumulator left through carry
RRC:	Rotate accumulator right
RAR:	Rotate accumulator right through carry

Logic operations: Compare

CMP R/M: Compare register/memory with accumulator

CPI 8 bit: Compare immediate with accumulator

If A < R/M, CY = 1, Z = 0

If A > R/M CY = 0, Z = 0

If A = R/M CY = 0, Z = 1

Remaining flags effected according to the result of subtraction.

16-bit data transfer and data exchange instructions

LHLD 16 bit	load HL registers direct
SHLD 16 bit	store HL registers direct
XCHG 16bit	exchange the contents of HL with DE
XTHL	exchange the top of the stack with HL
SPHL	Copy HL reg pair into stack pointer
PCHL	copy HL reg pair into the program counter
ADC R/M	Add Reg/memory contents with carry to accumulator
SBB R/M	Subtract R/memory contents with borrow from accumulator
DAA	Decimal adjust accumulator, it adjusts the 8-bit number in accumulator to form 2BCD numbers. It works with addition when BCD numbers are used
ACI 8 bit	Add immediate to accumulator with carry
CMC	Complement carry
DAD RP:	add register pair to HL registers
DI	disable interrupts
EI	enable interrupts
POP RP	POP off stack to reg pair
PUSH Rp	push register pair on to stack
SBI 8 bit	subtract immediate with borrow
STC	set carry
RIM	read interrupt mask
SIM	set interrupt mark
RST	restart

## STACK

Memory locations in R/W memory can be employed as temporary storage for information by initializing 16-bit address in the stack pointer (SP) register, and these memory locations are called stack.

The stack space grows upward in the numerically decreasing order of memory address.

The contents of the stack pointer can be interpreted as the address of the memory location that is already used for storage. The retrieval of bytes begins at the address in the stack pointer; however, the storage begins at the next memory location (in the decreasing order).

The storage and retrieval of data bytes on the stack should follow the LIFO (last-in first-out sequence) information in stack location and it is not destroyed until new information is stored in those locations.

PUSH Rp: store register pair on stack.

In copies, the contents of the specified register pair on the stack. The stack pointer register is decremented and the contents of high order register (e.g., register B, D/H) are copied in the location shown by stack pointer register. The stack pointer register again decremented and the contents of the low order register (e.g., register C/E/L) are copied in that location.

Operand PSW represents program status word, meaning the contents of the accumulator and the flags.

POP Rp: Retrieve register pair from stock.

It copies the contents of the top two memory locations of stack into specified register pair.

First, the contents of the memory location indicated by the stack pointer register are copied into the low order register (e.g., register C/E/L) and then the stack pointer register incremented by 1. The contents of the next memory location are copied into the high order register (e.g., register H/B/D) and the stack pointer register is again incremented by 1.

## SUBROUTINE

It is a group of instructions written separately from the main program to perform a function that occurs repeatedly in the main program.

8085 has two instructions to implement subroutines:

CALL 16 bit: call subroutine unconditionally.

It transfers the program sequence to a subroutine address specified in instruction.

First, it saves the contents of the program counter (the address of the next instruction) on the stack. However, it decrements the stack pointer by two, jumps unconditionally to the memory location specified by the second, and third bytes in instruction. This instruction is accompanied by a return instruction in the subroutine.

RET: return from subroutine unconditionally

It inserts the two bytes from the top of the stack into the program counter and increments stack pointer by two. Unconditionally, returns from a subroutine.

## Conditional Call and Return Instructions

The conditional call and return instructions are based on four data conditions (flags): carry, zero, sign, and parity.

If the call instruction in the main program is conditional, the return instruction in the subroutine can be conditional or unconditional.

CC 16 bit: call subroutine if carry flag is set ( $CY = 1$ )

CNC 16 bit: call subroutine if carry flag is reset ( $CY = 0$ )

CZ 16 bit: call subroutine if zero flag is set ( $z = 1$ )

CNZ 16 bit: call subroutine if zero flag is reset ( $z = 0$ )

CM 16 bit: call subroutine if sign flag is set ( $S = 1$  negative number)

CP 16 bit: call subroutine if sign flag is reset ( $S = 0$  positive number)

CPE 16 bit: call subroutine if parity flag is set ( $p = 1$  even parity)

CPO 16 bit: call subroutine if parity flag is reset ( $P = 0$ , odd parity)

Conditional RETURN

RC – Return if  $CY = 1$     RM – Return if  $S = 1$

RNC – Return if  $CY = 0$     RP – Return if  $S = 0$

RZ – Return if  $Z = 1$ ,    RPE – Return if  $P = 1$

RNZ – Return if  $Z = 0$ ,    RPO – Return if  $P = 0$

The programming technique of a subroutine calling another subroutine is called nesting, and this process is limited only by the number of available stack locations. When a subroutine calls another subroutine, all return addresses are stored on the stack. One call can have multiple return instructions.

## Restart (RST) Instructions

RST instructions are one-byte call instructions that transfer the program execution to a specific location on page 00H.

RST 0 – Call 0000 H

RST 1 – Call 0008 H

RST 2 – Call 0010 H

RST 3 – Call 0018 H

RST 4 – Call 0020 H

RST 5 – Call 0028 H

RST 6 – Call 0030 H

RST 7 – Call 0038 H

The interrupt is an asynchronous process of communication with the microprocessor initiated by an external peripheral.

The 8085 has a maskable interrupt that can be enabled or disabled using the instructions EI and DI. The 8085 has four additional interrupt inputs: one non-maskable and three maskable interrupt inputs; these three interrupts are implemented without any external hardware and are known as RST 7.5, 6.5, and 5.5.

The instruction SIM is necessary to implement interrupt 7.5, 6.5, and 5.5. The instruction RIM can be used to check whether any interrupt requests are pending.

The direct memory access (DMA) is a process of high-speed data transfer under the control of external devices like a DMA controller.

## Summary of Interrupts in 8085 in the order of their priority.

Interrupts	Type	Trigger
TRAP	Non maskable – vectored (0024H)	Level and edge sensitive
RST 7.5	Maskable vectored (003CH)	Edge sensitive
RST 6.5	Maskable vectored (00034H)	Level sensitive
RST 5.5	Maskable vectored (0002CH)	Level sensitive
INTR	Maskable non-vectored (RST code from external hardware (0000–0038H))	Level sensitive

## Example 3

Consider the following set of instructions:

LXI B, 7E45H

STC

MOV A, B

ORA A

RAL

MOV B, A

This set of instructions

(A) doubles the number in register B.

(B) divides the number in register by 2.

(C) OR contents of B and A.

(D) adds A and B register contents.

## Solution

LXI B, 7E45H – move 7E45H to BC register pair, i.e., B = 7EH, C = 45H.

STC – set carry,  $CY = 1$

MOV A,B – Move contents of B to A.

ORA A – OR content of A with A itself; this makes  $CY = 0$ , and other flags will be effected as per result in A, and contents of A will not be altered as  $A \text{ OR } A = A$  only.

RAL – rotate accumulator left arithmetically, that is, include carry bit in rotation; this instruction moves the contents of accumulator to shift left by 1 bit, and carry bit (= 0) will be added at LSB side. This rotation is equal to multiplication by 2. Left shift by  $n$ -bit = multiplication by  $2^n$ .

MOV B,A – move contents of A to B, that is, store result in B again. Now, the contents of B are doubled.

**Direction for questions 2 to 4:**

Consider the following program of 8085 microprocessor and a subroutine at memory location 1010H.

2020: LXI H, 2020H  
 2023: SPHL  
 2024: MOV A, C  
 2025: XRA C  
 2026: RAL  
 2027: CZ 1010H  
 202A: NOP

1010: PUSH B  
 1011: PUSH D  
 1012: POP B  
 1013: POP D  
 1014: XTHL  
 1015: RET

**Example 4:** What is the operation of subroutine at 1010H?

- (A) Interchanges contents of B and D registers
- (B) Swaps the contents of SP and HL register pair
- (C) Interchanges the contents of B and D register pairs.
- (D) Copies the top of the stack to HL register pair.

**Example 5:** What are the contents of SP when the microprocessor is executing instruction at 1014H?

- (A) 201E H
- (B) 2020 H
- (C) 1015 H
- (D) 202A H

**Example 6:** For how many number of times, the instruction at 202AH will execute?

- (A) Infinite times
- (B) 2
- (C) 1
- (D) Never executes

**Solutions for questions 2 to 4**

2020: LXI H, 2020 H: Load HL register path with 2020H, HL = 2020H  
 2023: SPHL: Move HL register pair to SP stack pointer, SP = 2020H  
 2024: MOV A, C: Move contents of register C to accumulator  
 2025: XRA C: XOR Accumulator with C, Now A = 00H. CY = 0, Z = 1.  
 2026: RAL: rotate accumulator left through carry now CY = 0, A = 00H  
 2027: CZ 1010H: jump to 1010 if zero flag = 1, as Z = 1; now, control execution and go to 1010H

However, to return to main program, CALL instruction stores the present PC = 202AH on top of the stack; therefore, now contents of top of stack are 202A, SP = 201EH and PC will be charged to 1010H.

1010: PUSH B: move contents of BC register pair on top of stack

1011: PUSH D: move contents of DE register pair on top of stack

1012: POP B: retrieve the top of stack contents to BC register pair, that is, BC = DE

1013: POP D: retrieve the top of stack contents to DE register pair, that is, DE = BC

These four instructions will interchange B,D register pairs, as stack works with last-in first-out principle. After these four instructions, the top of stack will have 202AH and SP = 201E H.

1014: XTHL: Exchange top of stack with HL register pair contents;

Now, HL = 202AH, top of stack = 2020H

1015: RET: Return instruction returns to main program by taking the stored address of next instruction of CALL instruction on top of the stack, that is, by retrieving top of the stack to PC.

Now, PC->2020H. Therefore, the execution starts from 2020H and CZ will be always 1 and CALL(CZ) will be executed infinite number of times.

2. (C)                      3. (A)                      4. (D)

**Example 7**

Consider the following program for an 8085 microprocessor

MVI A, 8-bit data  
 ANA A  
 JP SUB1  
 XRA A

SUB1: OUT 8-bit port address  
 HLT

At output port

- (A) only numbers with even number of 1's will appear
- (B) only numbers with odd number of 1's will appear
- (C) no negative numbers will appear
- (D) only negative numbers will appear

**Solution**

MVI A, 8-bit data – move 8-bit data to accumulator  
 ANA A – AND accumulator with accumulator itself.

JP SUB1 – if sign flag is 0, that is, for positive number jump to SUB1, else go to next instruction.

XRA A – XOR A with A, that is, contents of A – 00H

SUB1: OUT 8-bit port address – output the accumulator contents to the 8-bit port address.

HLT – stop execution.

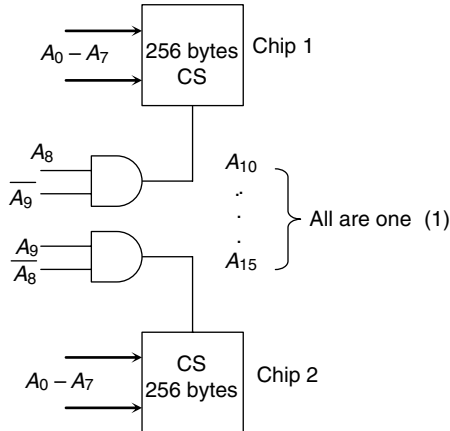
The program outputs only positive numbers, if the jump on positive condition fails, then contents of accumulator will be reset, and 00H will be the output at output port.

## EXERCISES

## Practice Problems I

**Direction for questions 1 to 16: Select the correct alternative from the given choices.**

1. Given two memories, what is the memory address range represented by chip 1 or chip 2. (CS – chip select,  $A_0$ – $A_{15}$  are address lines)



- (A) 0100–02FF (B) F500–F6FF  
(C) F900–FAFF (D) FD00–FEFF
2. If we have an 8085 program, as shown in the figure, such that the program starts at location 0100H, and the content of accumulator when PC reaches 010CH is
- ```

LXI SP, 00EF
LXI H, 0700
MOV A, M
XRA M
MOV M, A
MVI A, 30H
SUB M

```
- (A) 30H (B) 02H  
(C) 00H (D) FFH
3. From the given program, what will be the content of SP on completion of RET execution?
- ```

LXI SP, EFFFH
CALL 2000 H
2000H LXI H, 3CF4 H
      PUSH PSW
      SPHL
      POP PSW
      RET

```
- (A) EFFF (B) EFFF  
(C) 3CF6 (D) 3CF8
4. Given a 8085 program, indicate the status of CY and Z flags after the execution of line 7 in the program.
- ```

Line 1: MVI A, B5H
      2: MVI B, 0EH
      3: XRI 69H

```

- 4: ADD B  
5: ANI FBH  
6: CPI 9F H  
7: STA 3010 H  
8: HLT

- (A) CY = 0, Z = 0 (B) CY = 0, Z = 1  
(C) CY = 1, Z = 0 (D) CY = 1, Z = 1

5. Predict the content of PC and HL after the execution of part of program.

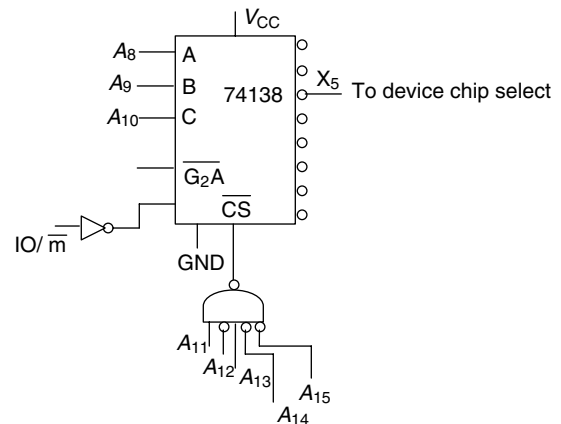
```

2710 LXI H, 30A2H
2713 DAD H
2714 PCHL

```

- (A) PC = 2715 H HL = 30 A2 H  
(B) PC = 30 A2 H HL = 2715 H  
(C) PC = 6144 H HL = 6144 H  
(D) PC = 6144 H, HL = 2715 H

6. Determine the address range for the device connected to  $X_5$ .



- (A) 2D00–2DFF (B) 2E00–2EFF  
(C) FD00–FDFF (D) 2F00–2FFF

7. For the program, find the content of accumulator after its complete execution.

```

MVI A, 40 H
MOV B, A
STC
CMC
RAR
XRA B

```

- (A) 60 H (B) 67 H  
(C) 20 H (D) 40 H

8. Serial input data of 8085 can be loaded into bit 7 of accumulator by

- (A) executing an RIM instruction  
(B) using TRAP  
(C) executing an RST 1  
(D) none of these

9. Consider the program  
 LXI D, 0009 H  
 XRA A

LOOP: DCX D  
 JNZ LOOP

The loop will be executed

- (A) 9 times (B) 8 times  
 (C) 1 time (D) None of these

10. If we have an I/O port having address of 01H, what will be the content of flag register after the execution of instructions? (assume data is 75 H)

IN 01 H  
 ANI 81 H

- (A) 1 0 \* 1 \* 1 \* 0  
 (B) 0 1 \* 1 \* 0 \* 0  
 (C) 0 1 \* 0 \* 0 \* 0  
 (D) 0 1 \* 0 \* 1 \* 0

11. The content of SP and HL after the execution of instruction.

1000 LXI SP, 27FE  
 1003 CALL 1006  
 1006 POP H

- (A) SP = 27FE, HL = 1003  
 (B) SP = 27FD, HL = 1003  
 (C) SP = 27FE, HL = 1006  
 (D) SP = 27FC, HL = 1006

12. In order to design a memory system of size 16 k bytes using chips with 11 address lines and 4 data lines each, how many chips are required?

- (A) 8 (B) 2 (C) 16 (D) 4

13. If A contains 39 BCD, B contains 12 BCD, then what will be the output of instructions?

ADD B  
 DAA

- (A) 4 BH (B) 51 H (C) B1 H (D) 18 H

14. What are events followed by the instruction POP PSW in 8085 microprocessor?

- (A) flag register  $\leftarrow$  [SP] (B) SP  $\leftarrow$  SP + 1  
 SP  $\leftarrow$  SP + 1 flag register  $\leftarrow$  [SP]  
 A  $\leftarrow$  [SP] SP  $\leftarrow$  SP + 1  
 SP  $\leftarrow$  SP + 1 A  $\leftarrow$  [SP]  
 (C) SP  $\leftarrow$  SP - 1 (D) flag register  $\leftarrow$  [SP]  
 flag register  $\leftarrow$  [SP] SP  $\leftarrow$  SP - 1  
 SP  $\leftarrow$  SP - 1 SP  $\leftarrow$  SP - 1  
 A  $\leftarrow$  [SP] [SP]  $\leftarrow$  A

**Direction for questions 15 and 16:**

An 8085 assembly language program is given:

Line 1 : MVI A, B5H  
 2 : MVI B, 0EH  
 3 : XRA A  
 4 : ADD B  
 5 : ANI 8CH  
 6 : CPI 8DH  
 7 : STA 3010H  
 8 : HLT

15. The contents of the accumulator just after execution of the ADD instruction in line 4 will be

- (A) 00H  
 (B) C3H  
 (C) 0CH  
 (D) 0EH

16. After execution of line 7 of the program, the status of the CY and Z flags are

- (A) CY = 0, Z = 0  
 (B) CY = 0, Z = 1  
 (C) CY = 1, Z = 0  
 (D) CY = 1, Z = 1

## Practice Problems 2

**Direction for questions 1 to 15:** Select the correct alternative from the given choices.

1. In an 8085 microprocessor, if we execute the instruction CMP B with content of B less than that of accumulator. As a result,

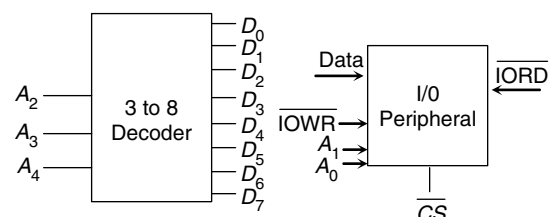
- (A) both carry flag and zero flag are set  
 (B) carry flag is set and zero flag is reset  
 (C) both carry flag and zero flag are reset  
 (D) carry flag is reset and zero flag is set

2. Match the number of machine cycles required to execute the instructions.

- |                    |     |   |
|--------------------|-----|---|
| (i) LHLD 2050H     | (1) | 5 |
| (ii) LDA 2050H     | (2) | 4 |
| (iii) LXI H, 2050H | (3) | 2 |
| (iv) XCHG          | (4) | 3 |
|                    | (5) | 1 |

- (A) i - 1, ii - 2, iii - 4, iv - 5  
 (B) i - 1, ii - 2, iii - 4, iv - 3  
 (C) i - 1, ii - 5, iii - 1, iv - 3  
 (D) i - 2, ii - 1, iii - 1, iv - 5

3. An input/output peripheral is to be interfaced to an 8085 microprocessor. To select the input/output device in address range E1 to E3H, its  $\overline{CS}$  should be connected to which of the decoder output pins?



- (A)  $D_0$  (B)  $D_7$   
(C)  $D_1$  (D)  $D_3$
4. An instruction that can be used so as to select only the higher 4 bits of accumulator in 8085 programming language  
(A) ANI FOH (B) ANI OFH  
(C) XRI OFH (D) XRI FOH
5. It is desired to multiply 0AH by 0BH and store the result in accumulator. The numbers are available in C and D. The steps required are  
(A) MVI A, 00 H (B) MVI A, 00 H  
LOOP: ADD C LOOP: JNZ LOOP  
DCR D ADD C  
JNZ LOOP DCR D  
HLT HLT  
(C) MVI A, 00 (D) None of these  
LOOP: ADD C  
JNZ LOOP  
DCR D  
HLT
6. The content of accumulator after the execution of instruction  
MVI A, 7H  
ORA A  
RLC  
(A) CFH (B) 4FH  
(C) 4EH (D) CEH
7. In the given program, the number of times the first and second JNZ instruction cause the control to be transferred to LOOP are  
MVI H, 02H  
MVI L, 05H  
LOOP: DCR L  
FIRST: JNZ LOOP  
DCR H  
SECOND: JNZ LOOP  
HLT  
(A) 5 and 2 (B) 4 and 1  
(C) 259 and 1 (D) 260 and 2
8. If the accumulator content is 27 H and if carry flag is already set, the instruction ACI 16 H will result in  
(A) 3F H, CY = 1 (B) 39 H, CY = 0  
(C) 3E H, CY = 0 (D) 3E H, CY = 1
9. Match the vectored interrupts with the address  
A. TRAP (1) 002CH  
B. RST 7.5 (2) 003CH  
C. RST 6.5 (3) 0024 H  
D. RST 5.5 (4) 0034 H  
(A) A – 2, B – 3, C – A, D – 1  
(B) A – 3, B – 1, C – 2, D – 4  
(C) A – 4, B – 2, C – 1, D – 3  
(D) A – 3, B – 2, C – 4, D – 1

10. For the given program of 8085  $\mu$ P, what is the time interval between two  $\overline{MEMW}$  signal?

```
START: MOV A, B
      OUT 55
      DCR B
      STA FFF8 H
      JMP START
```

- (A) 5.8  $\mu$ s (B) 6.2  $\mu$ s  
(C) 7.8  $\mu$ s (D) 5.2  $\mu$ s

11. Consider the following microprocessor programming code

```
LXI H, 5050H
MOV A, M
MOV B, 05H
ADD A, B
CMA
MOV M, A
HLT
```

Memory location 5050H is loaded with  $(0A)_{16}$ .

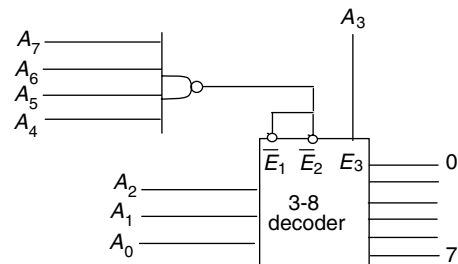
The status of zero flag and carry flag after execution of CMA is

- (A)  $Z = 1, C = 1$   
(B)  $Z = 0, C = 1$   
(C)  $Z = 1, C = 0$   
(D)  $Z = 0, C = 0$

12. The last address location of a 1 kB memory chip is given as F080. The starting address will be

- (A) EC 80H (B) EC 81H  
(C) F000H (D) EC00H

13. A 3-8 decoder is used to decode the addresses and interface it to the microprocessor. Address lines are connected to the decoder, as shown in the figure. The range of address possible to be selected by the given schematic is



- (A) 88H – 8FH (B) F0H – F8H  
(C) F8H – FFH (D) 00H – FFH

14. Consider the following assembly language program.

```
MVI A, B3H
MVI B, 10H
XRI 69H
ADD B
STA 3000H
HLT
```

The content of accumulator after executing ADD instruction will be

- (A) 69H (B) DAH  
(C) EAH (D) CIH

15. The following is the status of control buses of an 8085 program.

$\overline{IO/\overline{M}}$  – HIGH

$\overline{RD}$  – LOW]

$\overline{WR}$  – HIGH

The data in memory location 2500 H is 08H. The output port is 25H and input port is 20H. The assembly language instruction being executed is

- (A) IN 08H (B) OUT 25H  
(C) OUT 08H (D) IN 20H

### PREVIOUS YEARS' QUESTIONS

1. The 8255 programmable peripheral interface is used as

- I. an A/D converter is interfaced to a microprocessor through an 8255. The conversion is initiated by a signal from the 8255 on port C. A signal on port C causes data to be strobed into port A.
- II. two computers exchange data using a pair of 8255s. Port A works as a bi-directional data port supported by appropriate hand shaking signals.

The appropriate modes of operation of the 8255 for I and II would be [2004]

- (A) Mode 0 for I and mode 1 for II  
(B) Mode 1 for I and mode 0 for II  
(C) Mode 2 for I and mode 0 for II  
(D) Mode 2 for I and mode 1 for II

2. The number of memory cycles required to execute the following 8085 instructions

- I. LDA 3000H
- II. LXI D, FOF 1H

would be [2004]

- (A) 2 for I and 2 for II  
(B) 4 for I and 3 for II  
(C) 3 for I and 3 for II  
(D) 3 for I and 4 for II

3. Consider the following sequence of 8085 instructions. LXI H, 9258, MOV A, M, CMA, MOV M, A Which one of the following is performed by this sequence? [2004]

- (A) Contents of location 9258 are moved to the accumulator.  
(B) Contents of location 9258 are compared with the contents of the accumulator.  
(C) Contents of location 9285 are complemented and stored in location 9285  
(D) Contents of location 5892 are complemented and stored in location 5892.

4. It is desired to multiply the numbers 0AH by 0BH and store the result in the accumulator. The numbers are available in registers B and C, respectively. A part of the 8085 program for this purpose is given:  
MVI A, 00 H

Loop; .....

.....

.....

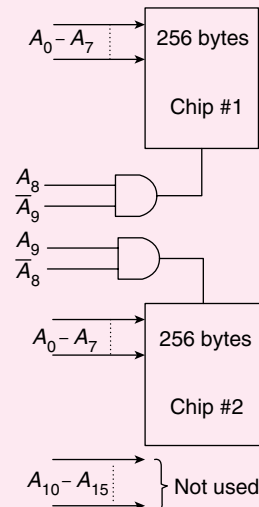
HLT END

The sequence of instructions to complete the program would be [2004]

- (A) JNZ LOOP, ADD B, DCR C  
(B) ADD B, JNZ LOOP, DCR C  
(C) DCR C, JNZ LOOP, ADD B  
(D) ADD B, DCRC, JNZ LOOP

5. What memory address range is NOT represented by chip #1 and chip #2 in figure?  $A_0$  to  $A_{15}$  in this figure are the address lines and CS means chip select. [2005]

- (A) 0100–02FF (B) 1500–16FF  
(C) F900–FAFF (D) F800–F9FF

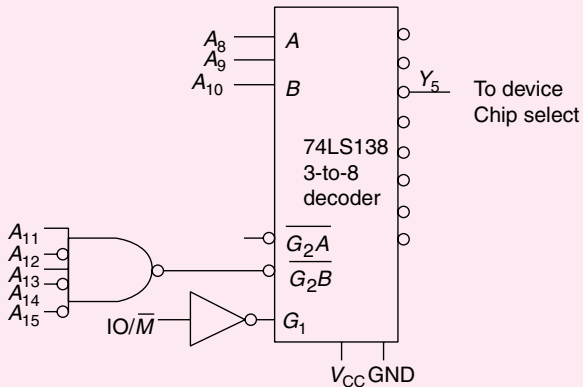


**Direction for questions 6 and 7:**

Consider an 8085 microprocessor system  
The following program starts at location 0100H and contents of 0701H are 20H

```
LXI SP, 00FF
LXI H, 0701
MVI A, 20H
SUB M
```





- (A) 2000–20FF (B) 2D00–2DFF  
(C) 2E00–2EFF (D) FD00–FDFF

16. For the 8085 assembly language program, the content of the accumulator after the execution of the program is [2010]

```

3000 MVI A, 45 H
3002 MOV B, A
3003 STC
3004 CMC
3005 RAR
3006 XRA B

```

- (A) 00H (B) 45H (C) 67H (D) E7H

17. The following is an 8085 assembly language program. Assume that the carry flag is initially unset. The content of the accumulator after the execution of the program is [2011]

```

MVI A, 07H
RLC
MOV B, A
RLC
RLC
ADD B
RRC

```

- (A) 8CH (B) 64H  
(C) 23H (D) 15H

18. For 8085 microprocessor, the following program is executed

```

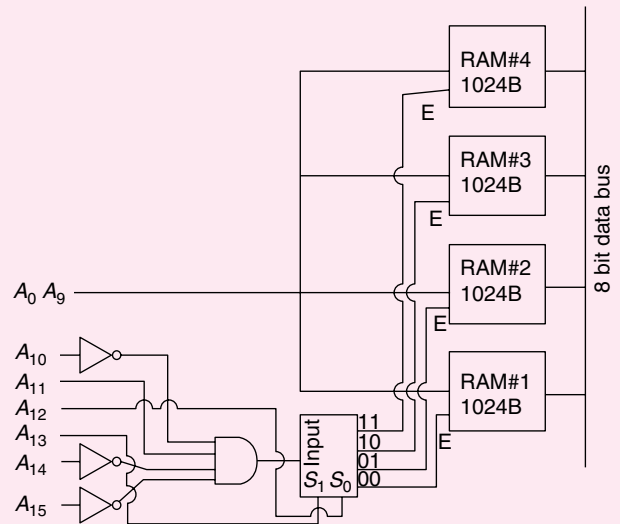
MVI A, 05H,
MVI B, 05H,
PTR ADD B,
DCR B,
JNZ PTR,
ADI 03H,
HLT,

```

At the end of program, accumulator contains [2013]

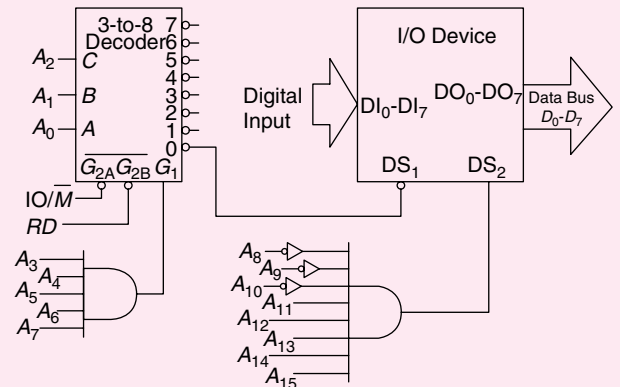
- (A) 17H (B) 20H  
(C) 23H (D) 05H

19. There are four chips each of 1024 bytes connected to a 16-bit address bus, as shown in the figure, RAMs 1, 2, 3, and 4, respectively, are mapped to addresses [2013]



- (A) 0C00H–0FFFH, 1C00H–1FFFH, 2C00H–2FFFH, 3C00H–3FFFH  
(B) 1800H–1FFFH, 2800H–2FFFH, 3800H–3FFFH, 4800H–4FFFH  
(C) 0500H–08FFFH, 1500H–18FFFH, 3500H–38FFFH, 5500H–58FFFH  
(D) 0800H–0BFFFH, 1800H–1BFFFH, 2800H–2BFFFH, 3800H–3BFFFH

20. For the 8085 microprocessor, the interfacing circuit to input 8-bit digital data ( $DI_0$ – $DI_7$ ) from an external device is shown in the figure. The instruction for correct data transfer is [2014]



- (A) MVI A, F8H (B) IN F8H  
(C) OUT F8H (D) LDA F8FH

21. An 8085 microprocessor executes 'STA 1234H' with starting address location 1FFEh (STA copies the contents of the accumulator to the 16-bit address location). While the instruction is fetched and executed, the sequence of values written at the address pins  $A_{15}$  to  $A_8$  is [2014]

- (A) 1FH, 1FH, 20H, 12H  
(B) 1FH, FEH, 1FH, FFH, 12H  
(C) 1FH, 1FH, 12H, 12H  
(D) 1FH, 1FH, 12H, 20H, 12H

22. In an 8085 microprocessor, the shift register that stores the result of an addition and the overflow bit are, respectively [2015]  
 (A) B and F (B) A and F  
 (C) H and F (D) A and C
23. In an 8085 microprocessor, which one of the following instructions changes the content of the accumulator? [2015]  
 (A) MOV B, M (B) PCHL  
 (C) RNZ (D) SBI BEH
24. Which one of the following 8085 microprocessor programs correctly calculates the product of two 8-bit numbers stored in registers B and C? [2015]
- (A) MVI A, 00H  
 JNZ LOOP  
 CMP C  
 LOOP DCR B  
 HLT
- (B) MVI A, 00H  
 CMP C  
 LOOP DCR B  
 JNZ LOOP  
 HLT
- (C) MVI A, 00H  
 LOOP ADD C  
 DCR B  
 JNZ LOOP  
 HLT
- (D) MVI A, 00H  
 ADC C  
 JNZ LOOP  
 LOOP INR B  
 HLT
25. In an 8085 system, a PUSH operation requires more clock cycles than a POP operation. Which one of the following options is the correct reason for this? [2016]  
 (A) For POP, the data transceivers remain in the same direction as for instruction fetch (memory to processor), whereas for PUSH their direction has to be reversed.  
 (B) Memory write operations are slower than memory read operations in an 8085 based system.  
 (C) The stack pointer needs to be pre-decremented before writing registers in a PUSH, whereas a POP operation uses the address already in the stack pointer.  
 (D) Order of registers has to be interchanged for a PUSH operation, whereas POP uses their natural order.
26. In an 8085 microprocessor, the contents of the accumulator and the carry flag are A7 (in hex) are 0, respectively. If the instruction RLC is executed, then the contents of the accumulator (in hex) and the carry flag, respectively, will be: [2016]  
 (A) 4E and 0 (B) 4E and 1  
 (C) 4F and 0 (D) 4F and 1

## ANSWER KEYS

### EXERCISES

#### Practice Problems 1

1. D    2. A    3. D    4. A    5. C    6. A    7. A    8. A    9. C    10. B  
 11. C    12. C    13. B    14. A    15. D    16. C

#### Practice Problems 2

1. C    2. A    3. A    4. A    5. A    6. B    7. C    8. C    9. D    10. C  
 11. D    12. B    13. C    14. C    15. D

#### Previous Years' Questions

1. D    2. B    3. C    4. D    5. D    6. C    7. C    8. B    9. B    10. C  
 11. B    12. C    13. C    14. D    15. B    16. C    17. C    18. A    19. D    20. D  
 21. A    22. B    23. D    24. C    25. C    26. D

## DIGITAL CIRCUITS

Time: 60 Minutes

**Direction for questions 1 to 30:** Select the correct alternative from the given choices.

- What is the range of signed decimal numbers that can be represented by 4 bit 1's complement number  
(A)  $-7$  to  $+7$  (B)  $-16$  to  $+16$   
(C)  $-7$  to  $+8$  (D)  $-15$  to  $+16$
- Which of the following have a unique representation of 0?  
(A) Sign magnitude (B) 1's complement  
(C) 9's complement (D) 2's complement
- Find the odd one among the following  
(A) EBCDIC (B) GRAY  
(C) Hamming (D) ASCII
- Gray code for number 8 is  
(A) 1100 (B) 1111 (C) 1000 (D) 1101
- Find the equivalent logical expression for  $z = x + \bar{x}y$   
(A)  $z = \bar{X}y$  (B)  $Z = \bar{x}Y$   
(C)  $Z = \bar{x} + Y$  (D)  $Z = X + Y$
- The number of distinct Boolean expressions of 3 variables is  
(A) 256 (B) 16 (C) 1024 (D) 65536
- The Boolean expression for the truth table shown is

| X | Y | Z | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

- $Y(X+Z)(\bar{X}+\bar{Z})$  (B)  $Y(X+\bar{Z})(\bar{x}+Z)$   
(C)  $\bar{Y}(X+\bar{Z})(\bar{x}+Z)$  (D)  $\bar{Y}(X+Z)(\bar{X}+\bar{Z})$
- The number of essential prime implicants for the Boolean functions shown in the given K-map.

| WZ | 00 | 01 | 11 | 10 |
|----|----|----|----|----|
| XY |    |    |    |    |
| 00 | 1  | 1  | 0  | 1  |
| 01 | 1  | 0  | 0  | 1  |
| 11 | 1  | 0  | 0  | 0  |
| 10 | 1  | 0  | 0  | 1  |

- (A) 4 (B) 5 (C) 6 (D) 8

- The no. of product terms in the minimized SOP from is

|   |   |   |   |
|---|---|---|---|
| 1 | 0 | 0 | 1 |
| 0 | D | 0 | 0 |
| 0 | 0 | D | 1 |
| 1 | 0 | 0 | 1 |

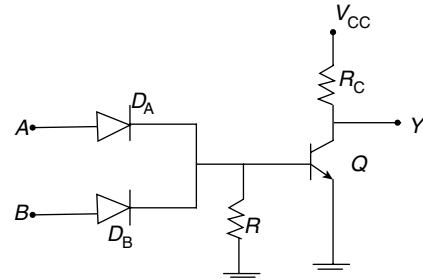
- 2 (B) 4 (C) 5 (D) 3
- The minimum number of 2 input NAND gates needed to implement  $Z = XY + VW$  is  
(A) 2 (B) 3 (C) 4 (D) 5
- The operation  $\bar{a} \oplus \bar{b}$  represent  
(A)  $ab + \bar{a}\bar{b}$  (B)  $\bar{a}b + a\bar{b}$  (C)  $a\bar{b} + \bar{a}b$  (D)  $a - b$
- Find the dual of  
 $X + [Y + XZ] + U$   
(A)  $X + [Y(x+z)] + U$  (B)  $X(Y+xz)U$   
(C)  $X + [Y(X+Z)]U$  (D)  $X[Y(x+z)]U$
- The simplified form of given function  $AB + BC + A\bar{C}$  is equal to  
(A)  $AB + A\bar{C}$  (B)  $A\bar{C} + BC$   
(C)  $\bar{A}C + BC$  (D)  $A\bar{B} + A\bar{C}$
- Simplify the following

| WX | YZ |   |   |  |  |
|----|----|---|---|--|--|
| 1  | 1  | 0 | 1 |  |  |
| 1  | 1  | 0 | 1 |  |  |
| 0  | 0  | 1 | 1 |  |  |
| 0  | 0  | 0 | 0 |  |  |

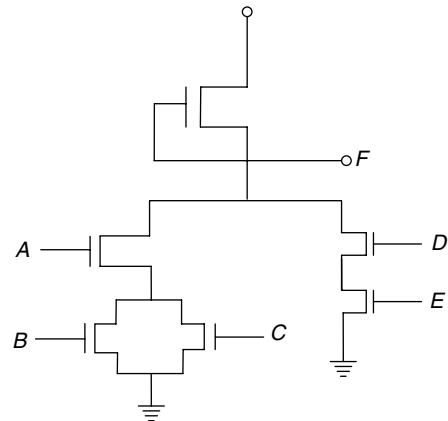
- $\bar{W}\bar{Y} + \bar{W}\bar{Z} + WXY$   
(B)  $\bar{W}\bar{X} + \bar{W}\bar{Z} + WXY$   
(C)  $WY + WYZ + WXY + XY\bar{Z}$   
(D)  $\bar{W}\bar{X} + \bar{Y}\bar{Z} + \bar{W}\bar{Z}$
- Simplify the following  
 $F = ABCD + \bar{A}\bar{B}CD + \bar{A}C\bar{B}D + \bar{A}BCD$   
(A)  $CD$  (B)  $BC$  (C)  $AB$  (D)  $\bar{C} + \bar{D}$
- Find the equivalent Boolean expression for  $AC + \bar{B}\bar{C}$   
(A)  $\bar{A}C + \bar{B}\bar{C} + AC$   
(B)  $ABC + \bar{A}\bar{B}C + \bar{A}BC + \bar{A}\bar{B}\bar{C}$   
(C)  $ABC + \bar{A}\bar{B}C + \bar{A}BC + \bar{A}\bar{B}\bar{C}$   
(D)  $\bar{A}C + \bar{B}\bar{C} + \bar{A}\bar{C}$
- Simplify the following expression  
 $\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + \bar{A}\bar{B}C$   
(A)  $\bar{A}\bar{C} + \bar{B}\bar{C} + \bar{A}B$   
(B)  $\bar{A}\bar{C} + \bar{B}\bar{C} + \bar{A}B$

- (C)  $\overline{A}\overline{C} + \overline{B}C + \overline{A}B$   
 (D)  $\overline{A}\overline{C} + \overline{B}C + \overline{A}B$
18. If  $A = 1$  in the logic equation  $\left[ A + C \left\{ \overline{B} + (\overline{C} + AB) \right\} \right] \left[ \overline{A} + \overline{C} (A + B) \right] = 1$ ; then  
 (A)  $B = C$  (B)  $B = \overline{C}$   
 (C)  $C = 1$  (D)  $C = 0$
19. Which is the odd function with 3 Boolean variables in it  
 (A)  $\Sigma(0, 3, 5, 6)$  (B)  $\Sigma(0, 2, 4, 6)$   
 (C)  $\Sigma(1, 2, 4, 7)$  (D)  $\Sigma(1, 3, 5, 7)$
20. Which of the following expressions is/are incorrect?  
 (A)  $\overline{a+b} = \overline{a} \overline{b}$  (B)  $\overline{\overline{a+b}} = \overline{a} \overline{b}$   
 (C)  $\overline{\overline{a} \overline{b}} = \overline{a} + \overline{b}$  (D)  $\overline{\overline{a} + \overline{b}} = \overline{a} \overline{b}$
21. Which of the following is true?  
 (A) TTL has lowest power consumption  
 (B) ECL has the least propagation delay  
 (C) TTL has the largest fan out  
 (D) CMOS has the lowest noise margin
22. The noise margin of TTL gate is  
 (A) 0.2V (B) 0.8V (C) 0.4V (D) 1.2V
23. Which of the following has lowest power dissipation?  
 (A) Schottky TTL (B) TTL  
 (C) ECL (D) CMOS
24. The totempole in standard TTL refers to  
 (A) Phase splitter  
 (B) Open collector O/P state  
 (C) Input emitter stage  
 (D) Output buffer
25. Which of the following is the suitable condition for interfacing two logic gates?  
 (A)  $V_{OH} > V_{IH}$ ,  $V_{IL} > V_{OL}$   
 (B)  $V_{OH} < V_{IH}$ ,  $V_{IL} < V_{OL}$   
 (C)  $V_{OH} > V_{IH}$ ,  $V_{IL} < V_{OL}$   
 (D)  $V_{OH} = V_{IH}$ ,  $V_{IL} = V_{OL}$

26. Which gate does the following figure represent?



- (A) NAND (B) NOR (C) AND (D) OR
27. Full form of I<sup>2</sup>L is  
 (A) inter integrated logic  
 (B) Inter injection logic  
 (C) Integrated injection logic  
 (D) Injection injection logic
28. The basic TTL gate is  
 (A) NAND (B) NOR (C) AND (D) OR
29. The logic function implemented by the following fig is



- (A)  $\overline{ABCDE}$  (B)  $(AB + \overline{C})(\overline{D} + \overline{E})$   
 (C)  $\overline{A.(B + C) + DE}$  (D)  $(\overline{A} + \overline{B})C + \overline{D} \overline{E}$
30. The fan out of basic TTL gate is  
 (A) 10–100 (B) 100–1000  
 (C) 1000–0000 (D) < 10

### ANSWER KEYS

- |       |       |       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 1. A  | 2. D  | 3. C  | 4. A  | 5. D  | 6. A  | 7. A  | 8. A  | 9. A  | 10. B |
| 11. C | 12. D | 13. B | 14. A | 15. A | 16. B | 17. A | 18. D | 19. C | 20. D |
| 21. B | 22. C | 23. D | 24. D | 25. A | 26. B | 27. C | 28. C | 29. C | 30. A |