Chapter 5

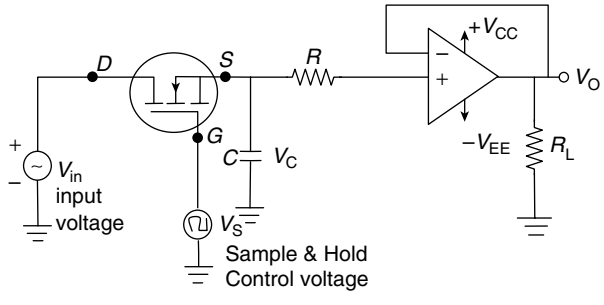
A/D and D/A Circuits and Semiconductor Memories

CHAPTER HIGHLIGHTS

- *Sample and Hold Circuit*
- *Digital to Analog Converter*
- *Analog to Digital Converters*
- *The Counter Type A/D Converter*
- *Servo Tracking A/D Converter*
- *Successive Approximation Converter*
- *Charge Balancing ADC*
- *Memory Classification*
- *Memory Architecture*
- *Static Memory (SRAM)*
- *Dynamic RAM (DRAM)*

Sample-and-Hold Circuit

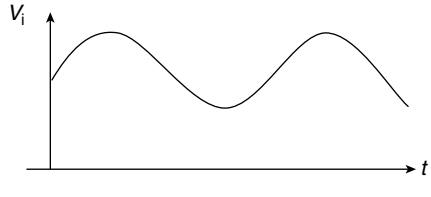
The sample-and-hold circuit as its name implies, samples an input signal and holds onto its last sampled value until the input is sample again.

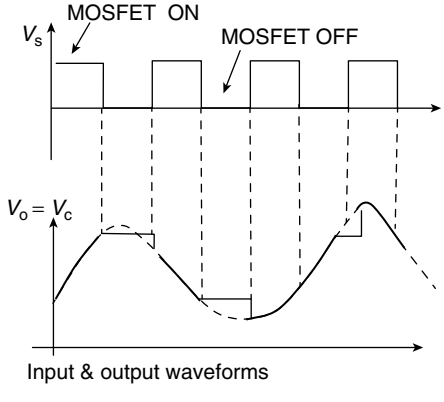


The analog signal V_{in} to be sampled is applied to the drain, and sample-and-hold control voltage (V_s) is applied to the gate of E-MOSFET.

During the positive portion of V_s, the MOSFET conducts and acts as a closed switch. This allows the input voltage to charge capacitor C, i.e., input voltage appears across C and in turn at the output.

When V_s is zero, the E-MOSFET is off (non-conductive) and acts as an open switch, the only discharge path for C is through op amp. However, the input resistance of op amp is very high, and hence voltage across C is retained.

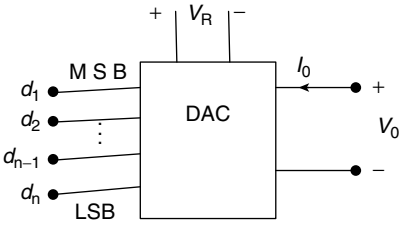




To obtain close approximation of the input waveform, the frequency of the sample-and-hold control voltage must be significantly higher than that of the input. The sample-and-hold circuit is commonly used in digital interfacing and communications.

Digital to Analog Converter

The input is an n-bit binary word D and is combined with a reference voltage V_R to give an analog output signal.



For a voltage output (DAC), the D/A converter is mathematically described as

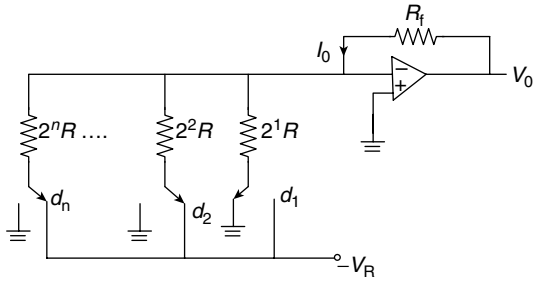
$$V_0 = KV_{FS}\,(d_1\,2^{-1} + d_2\,2^{-2} + \ldots. + d_n\,2^{-n})$$

where V_0 is the output voltage; V_{FS} is the full-scale output voltage; and K is the scaling factor.

Binary word $D = d_1\, d_2 \ldots d_n$

Weighted Resistor DAC

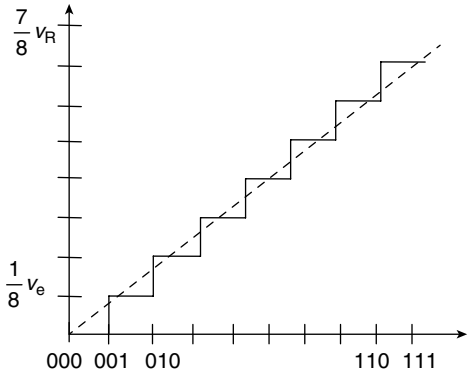
It uses a summing amplifier with a binary-weighted resistor network.



$$V_0 = I_0 R_f$$

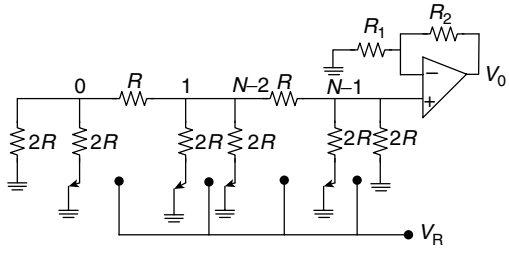
$$= V_R \frac{R_f}{R}(d_1 2^{-1} + d_2 2^{-2} \cdots + d_n 2^{-n})$$

The op amp can be connected either in inverting or non-inverting mode. The op amp is simply working as a current to voltage converter.



This DAC uses wide range of resistances. $2R - 2^nR$, and therefore, it is not suitable for integrated circuits.

R-2R Ladder DAC



This circuit utilizes twice the number of resistors as in binary weighted DAC, for the same number of bits (N) but of values R and $2R$ only.

The ladder used in this circuit is a current-splitting device. At any of the ladder nodes, the resistance is $2R$ looking to the left or the right or towards the switch.

Solved Examples

Example 1

The basic step of a 8-bit DAC is 12 mV. If 00000000 represents 0 V. What is the output for input 10110101?

Solution

Output is = 12 mV $(1 \times 2^7 + 1 \times 2^5 + 1 \times 2^4 + 1 \times 2^2 + 1 \times 2^0) = 2.172$ V

Example 2

Find the values of LSB, MSB, and full-scale output for an 8-bit DAC for 0–10 V. range are?

Solution

$$\text{LSB} = \frac{1}{2^8} = \frac{1}{256}^{\text{th}} \text{ of full-scale voltage}$$

$$\text{LSB} = \frac{10}{256} = 39 \text{ mV}$$

$$\text{MSB} = \left(\frac{1}{2}\right) \text{full-scale voltage} = 5 \text{ V}$$

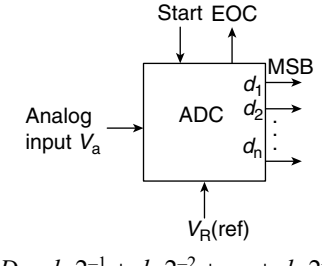
Full-scale output = full-scale reading = (full-scale voltage – 1LSB) = 10 v – 0.039 V = 9.961 V

1. Resolution $= \dfrac{F.S.V}{2^n} = \dfrac{F.S.R}{2^n - 1}$
2. MSB $= \dfrac{F.S.V}{2}$

Analog to Digital Converter

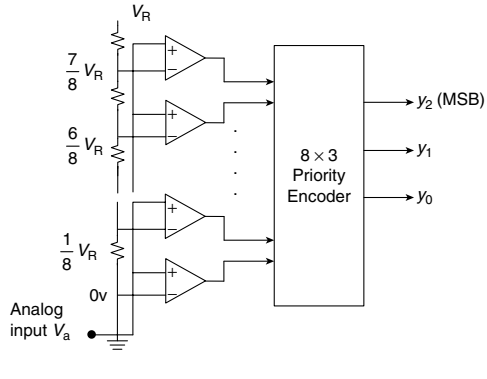
The block schematic of analog to digital converter (ADC) is shown in the figure.

It provides the function just opposite to that of a DAC. It accepts an analog input voltage V_a and produces an output binary word $d_1\, d_2 \ldots d_n$ of functional value D, so that

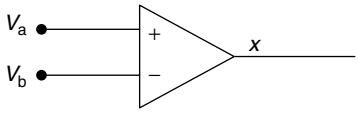


$$D = d_1\, 2^{-1} + d_2\, 2^{-2} + \ldots + d_n\, 2^{-n}$$

Parallel Comparator (Flash) A/D Converter



Basic circuit of a flash-type A/D converter.



Comparator and its truth table

Voltage input	Logic output
$V_a > V_b$	$X = 1$
$V_a < V_b$	$X = 0$
$V_a = V_d$	Previous value

This is the simplest possible ADC and at the same time, the fastest and the most expensive technique. At each node of the resistor divider, a comparison voltage is available, and the purpose of this circuit is to compare the analog, input voltage V_a with each of the node voltages. In general, the number of comparators required are $2^n - 1$ for n-bit ADC. Hence, the number of comparators doubles for each added bit.

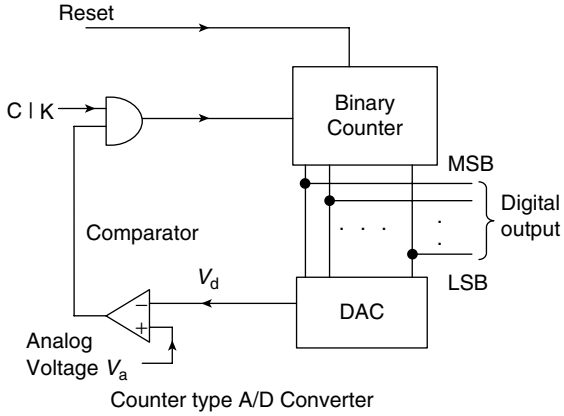
The Counter-type A/D Converter

The clear pulse resets the counter to zero count, and the counter then records in binary form and the number of pulses form the clock line.

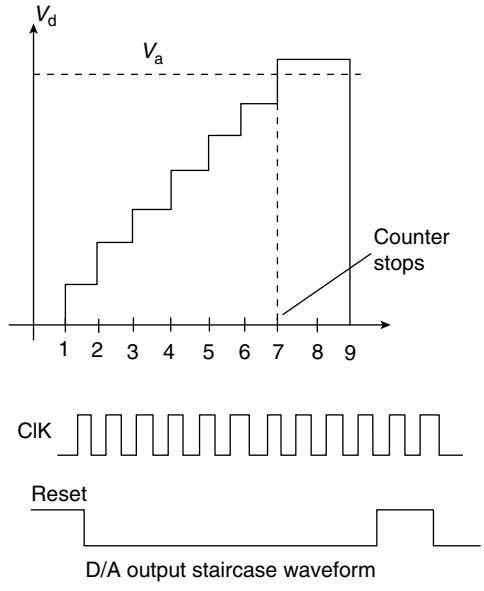
The principle is to adjust the DAC's input code until the DAC's output comes within $\pm\frac{1}{2}$ LSB to the analog input V_a, which is to be converted to binary digital form.

The counter frequency must be low enough to give sufficient time for DAC to settle and for the comparator to respond; further, low speed is the major drawback in this method.

The conversion time can be as long as $(2^n - 1)$ clock periods depending upon the magnitude of input V_a. For example, 12-bit system with 1 MHz clock frequency, the counter will take $(2^{12} - 1)$ μs = 4.095 ms to convert a full-scale input.



Counter type A/D Converter



D/A output staircase waveform

If the input signal is a sampled signal, the minimum interval between samples must be nT seconds for T-clock period and maximum value of input voltage is represented by n-pulses.

Servo Tracking A/D Converter

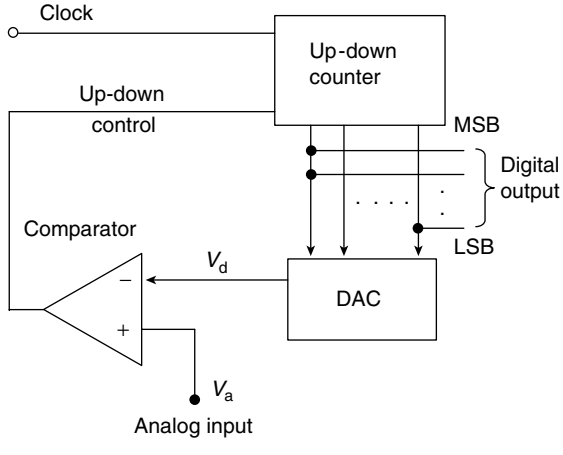
An improved version of counting ADC is the tracking or a servo converter shown in the figure.

The circuit consists of an up/down counter with the comparator controlling the direction of the count.

The analog output of the DAC is V_d and it is compared with the analog input V_a.

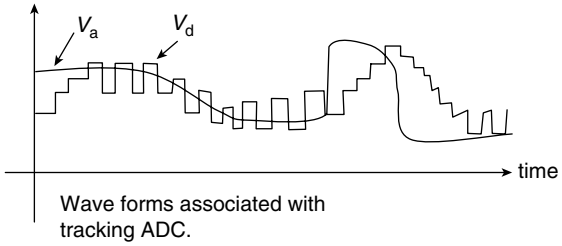
If input $V_a > V_d$, the output of the comparator goes high and the counter is caused to count up.

The DAC output increases with each incoming clock pulse and when it becomes more than V_a, the counter reverses the direction and counts down.



The process goes on being repeated and digital output changes back and forth by ±1 LSB around the correct value. However, the disadvantage is the time needed to stabilize as

a new conversion value is directly proportional to the rate at which the analog signal changes.

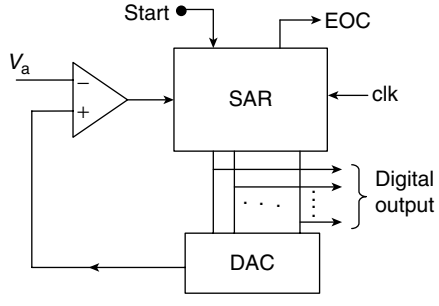


Wave forms associated with tracking ADC.

Successive Approximation Converter

The successive approximation technique uses a very efficient code search strategy to complete *n*-bit conversion in just *n* clock periods.

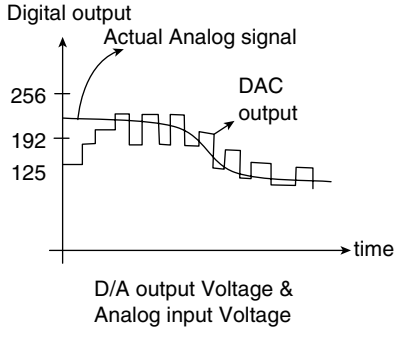
This circuit uses a successive approximation register (SAR) to find the required value of each bit by trial and error method.



Functional diagram of successive approximation ADC.

It can be seen that the D/A output voltage becomes successively closer to the actual analog input voltage. In general, the successive approximation ADC technique is more versatile and superior to all other circuits.

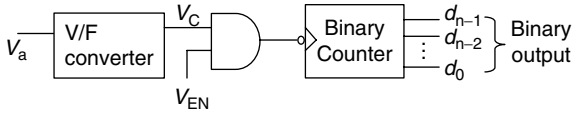
For all the ADCs that use DAC as one of their components, the major drawback is the resolution of ADC will depend upon resolution of DAC.



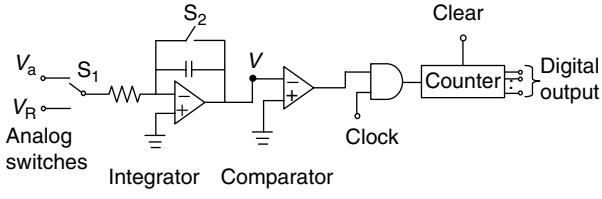
D/A output Voltage & Analog input Voltage

Charge-balancing ADC

The principle of charge-balancing ADC is to first convert the input signal to a frequency using a voltage to frequency (*V*/*F*) converter. This frequency is then measured by a counter and converted to an output code proportional to the analog input.

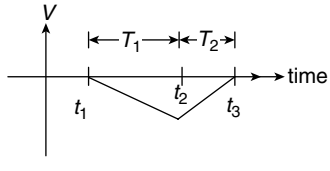


Dual-scope A/D Converter



$$V_a = V_R \cdot \frac{T_2}{T_1} = \frac{n_2 |V_R|}{n_1}$$

$$= n_2 \frac{|V_R|}{2^N}$$



This is a widely used system with $V_a > 0$ and $V_R < 0$. Initially, counter is cleared and at $t = t_1$, S_1 connects V_a and sampled for $n_1 = 2^N$ clock pulses. At time t_2 (at the end of the integration of v_a), all flip flops in the counter read 0.

Now, the reference voltage V_R is automatically connected to the input reference voltage V_R. When it is automatically connected to the input of the integrator at $t = t_2$, we have assumed that $|V_R| > V_a$, so that the integration time T_2 is less than T_1, as indicated. As long as V is negative, the output of the comparator is positive and the AND gate allows clock pulses to be counted. When V falls to zero at $t = t_3$, the AND gate is inhibited and no further clock pulses enter the counter.

$$V_a = n_2 \frac{|V_R|}{2^N},$$

V_a is proportional to counter reading n_2.

This technique can be very accurate; six-digit digital voltmeters employ such signal processing and the dual-scope system is inherently noise immune because of input signal integration.

Conversion time = 2^{N+1} clock cycles

Resolution

The resolution of a converter is the smallest change in voltage, which may be produced at the output or input of converter.

$$\text{Resolution} = \frac{V_{FS}}{2^N - 1} = 1 \text{ LSB increment}$$

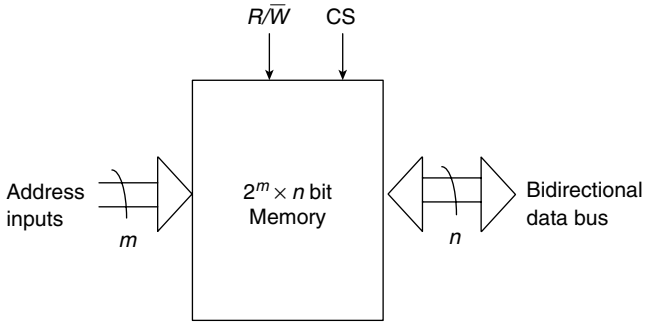
Semiconductor Memories

The advancement in the semiconductor technology resulted sophisticated microprocessors and semiconductor memories.

Garden Moore predicted that number of transistors nearly get doubled every couple of years per IC. As per this law, the semiconductor memory capacity also increases every year.

Any digital system requires facility for storing binary information given by the subsystem called memory.

The basic element of semiconductor memory is a flip-flop. The size of the memory chip, which consists of number of locations, is specified by $2^m \times n$, where m is the number of address bits, and n is the number of data bits. m-Bit address (in binary) can able to represent 2^m locations. The capacity of each location is 'n' bit. Therefore, the total capacity of memory = $2^m \times n$ bits.



To read data from memory: (1) chip-select signal should be applied to CS, (2) address of desired memory location has to be applied, (3) $R/\overline{W}$ input should be made 1, and (4) then the data in the location (specified by the address) appear on data output lines.

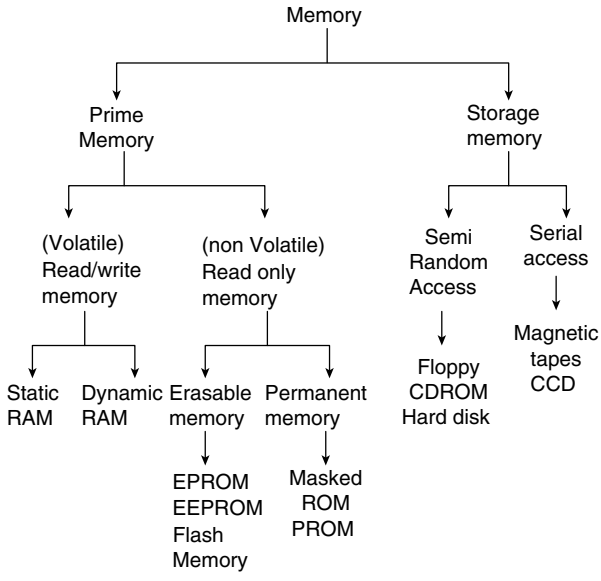
To write data into memory: (1) chip-select signal has to be enabled, (2) data to be written has to be applied to data inputs, (3) address of required memory location has to be applied, and (4) then write signal has to be applied by making $R/\overline{W} = 0$.

Memory Classification

Memory can be classified into two groups: prime (system or main) memory and storage memory. Main memory is the memory the microprocessor uses in executing and storing instructions. Therefore, it should able to respond as fast as execution speed of microprocessor and it should be random access memory so that microprocessor can be able to access any memory location with same speed.

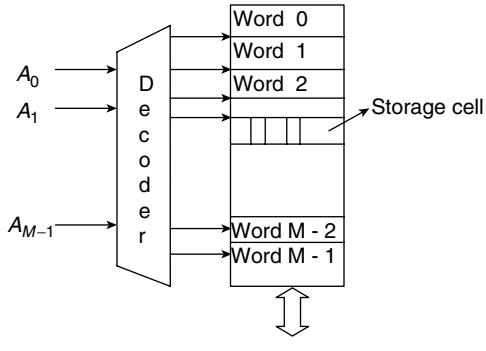
Storage memory is used to store result after execution. Generally, these memories are non-volatile, which means information remains intact even after power off.

Serial access memories such as FIFO (First In and First Out) and LIFO (Last In and First Out) access the data in serial order.



1. **Read/write memory:** It is also known as random access memory. This memory is volatile, meaning that when the power is turned off, all the contents are lost. This memory is used for data that need to be altered such as programs and data.
2. **Read only memory:** ROM is a non-volatile memory that retains the data even if the power is turned off. ROM is used for the programs or data that need not be altered.

Memory Architecture



'n'-bit data input/output

Consider M word memory, which uses m to 2^m decoder and ($M = 2^m$) words, each of size n bit. Therefore, total capacity is $2^m \times n$ bit. A decoder is used to decode the addresses and make the appropriate select line high for the M words.

For an M-word memory with a word length of 'n' bit, the aspect ratio (number of rows:number of columns) is M:n, which is very difficult to implement for large values of M. Such sort of a design slows down the circuit very much.

To overcome this problem, memory arrays are organized so that the vertical and horizontal dimensions are of the same order. Making the aspect ratio close to unity. The address word is divided into column address (A_0 to A_{k-1}) and row address (A_k to A_{m-1}). The row address enables one row of memory for read/write, while the column address

picks one particular word from the selected row. Here, two decoders are required: row decoder and column decoder.

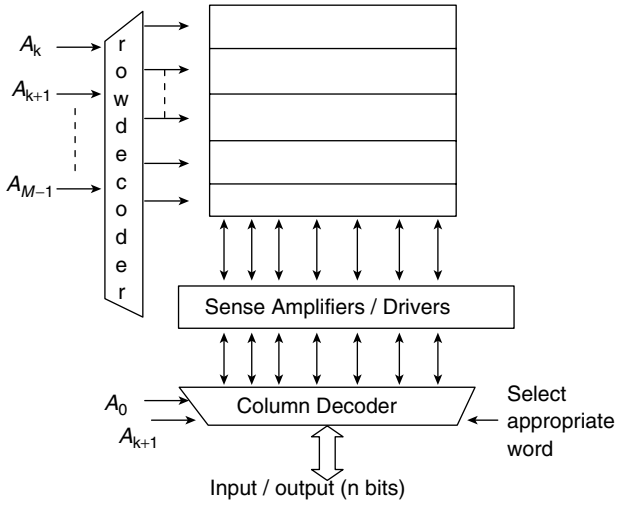


Figure 5.1 Memory with row and column decoders

Example 3

A 16 kb (= 16,384 bit) memory array is designed as a square with an aspect ratio of 1. Find the minimum number of address lines needed for the row decoder is.

Solution

16 kb memory array = 16 kb

$= 2^4 \times 2^{10} = 2^{14}$ bit

To make aspect ratio 1, number of rows = number of columns.

$2^{14} = 2^7 \times 2^7$

Therefore, we can make 7-bit row address and 7-bit column address.

Static Memory (SRAM)

SRAM is made up of flip-flops. It stores the bit as a voltage. Each memory cell requires six transistors. Therefore, the memory chip has low density (number of bits per chip) but high speed and consumes more power than DRAM. SRAMs are much faster having typical access times in the order of a few nanoseconds. Hence, SRAMS are used as cache memory for processors.

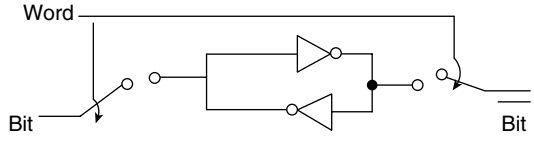


Figure 5.2 SRAM cell

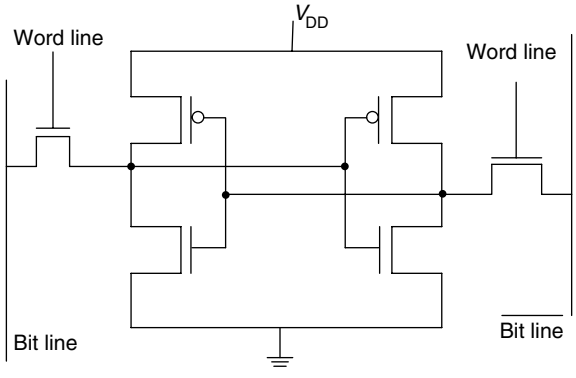
The memory said to be static as it retains the data as long as the power supply is on without any need of periodic refresh. The one-bit cell in static RAM array consists of simple latch circuit (inverters connected in regenerative feedback).

A low-power SRAM cell may be designed by using cross-coupled CMOS inverters.

The advantages of CMOS SRAM cell are as follows:

1. Least static power dissipation
2. Small leakage current
3. High noise immunity
4. Operated at lower power supply

The disadvantage is that it has large cell size consisting of six transistors.



CMOS SRAM Cell

The memory cell consists of two CMOS inverters connected back to back and two transistors with word line access. When the word line is active, the access transistors are turned on and the data can be read/written from the complementary bit-line columns.

Dynamic RAM (DRAM)

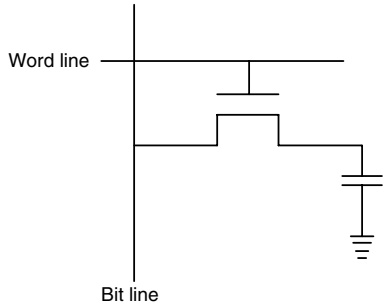
DRAM is made up of MOS transistor gates. Further, it stores the bit as a charge. DRAMs do not use flip-flops, but instead they are an array of cell, each containing an MOS transistor and capacitor. Logic 1 or logic 0 is stored on the capacitor by charging and discharging it. The electrical charge (bit information) on capacitor tends to leak out, and hence, each bit in DRAM must be refreshed every few milliseconds to prevent loss of data.

Advantages of DRAM

1. High density
2. Low power consumption
3. Cheaper than SRAM

Disadvantages of DRAM

1. It requires external circuit to refresh charge (bit information).



1 bit DRAM cell

The capacitor stores the charge (bit information) for the cell. The transistor gives the *R*/*W* access to the cell. When the word line is active, the transistor is ON and the bit line is connected to the capacitor to read/write data. Dynamic RAM has to be dynamically refreshed all the time or it forgets, what it is holding. This refreshing takes time and slows down the memory. The access time for DRAM is in order of tens of nanoseconds.

Types of ROM

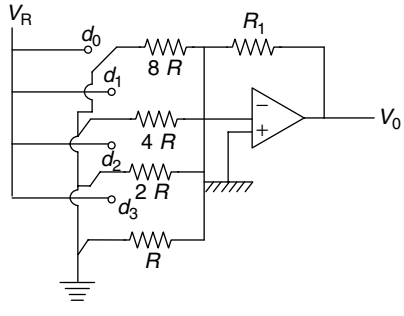
1. **Masked ROM:** In this ROM, a bit pattern is permanently recorded by the masking and metallization process. As per our requirement, memory manufacturer fabricates the masked ROM.
2. **PROM:** Programmable read only memory has Nichrome or polysilicon wires arranged in a matrix. The user can selectively burn the fuses by PROM programmer according to the bit pattern to be stored.
3. **EPROM:** Erasable programmable read only memory stores a bit by charging the floating gate of an FET. The information can be erased by exposing the chip to UV light, but erasing process takes 15–20 min.
4. **EEPROM:** Electrically erasable PROM same as EPROM; however, the information can be altered by using electrical signals. Memory can be erased in order of million seconds.
5. **Flash memory:** This is a variation of EEPROM; however, the difference is EEPROM can be erased at register level and the flash memory can be erased at block level.

Exercises

Practice Problems I

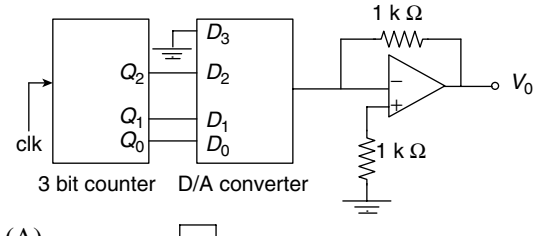
Direction for questions 1 to 10: Select the correct alternative from the given choices.

1. A 4-bit weighted DAC has $V_R = 2$ V and $\frac{R_1}{R} = 2$. For an input of 1,000, the output will be

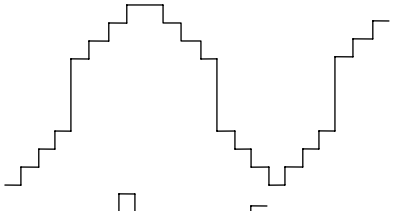


(A) −2 V (B) −4 V (C) −8 V (D) 8 V

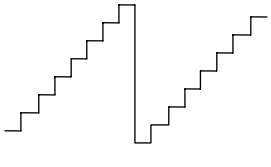
2. A 4-bit D/A converter is connected to free running 3-bit UP counter as shown in the following figure. What will be the waveform obtained at V_0?



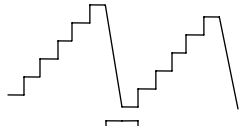
(A)



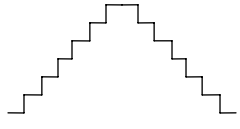
(B)



(C)



(D)



3. A 10-bit ADC is used to digitize an analog signal in the range 0–10 V. The maximum peak-to-peak ripple voltage that can be allowed in the DC supply voltage is

(A) nearly 100 mV (B) nearly 10 mV
(C) nearly 25 mV (D) nearly 5 mV

4. For a dual ADC-type 3 ½ DVM, reference voltage is 200 mV and first integration time is 400 ms. For the same input voltage, deintegration is 470.2 ms. The DVM will indicate

(A) 200 mV (B) 235.1 mV
(C) 199.9 mV (D) 1.818 mV

5. In the case of a dual-slope integrating-type ADC, if the output of 10-bit counter is clocked at 1 MHz, maximum frequency of analog signal that can be converted using ADC is

(A) 3 kHz (B) 2 kHz (C) 20 kHz (D) 1 kHz

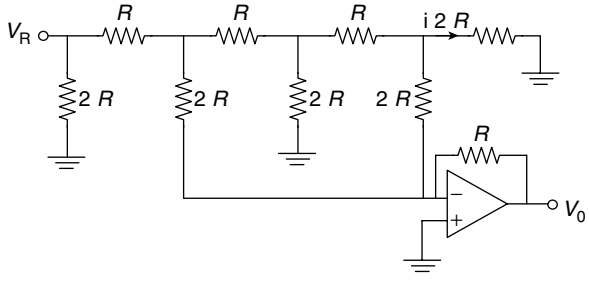
6. An 8-bit digital ramp ADC with a 50 mV resolution uses a clock frequency of 2.5 MHz and a comparator with $V_T = 1$ mV. The digital output for $V_A = 6$ V is

(A) 01111000 (B) 10010110
(C) 01011110 (D) 01011111

7. A sample-and-hold circuit having a holding capacitor of 0.1 nF is used at the input of an ADC. The conversion time is 1 μs and during this time, the capacitor should not lose more than 0.1% of charge put across it during the sampling time. The maximum value of the input signal to the *S*/*H* circuit is 5 V. The leakage current of *S*/*H* circuit is less than

(A) 2.5 mA (B) 0.25 mA (C) 5 μA (D) 0.5 μA

8. In the *D/A* converter, $V_R = 10$ V and $R = 10$ kΩ. Voltage V_0 is

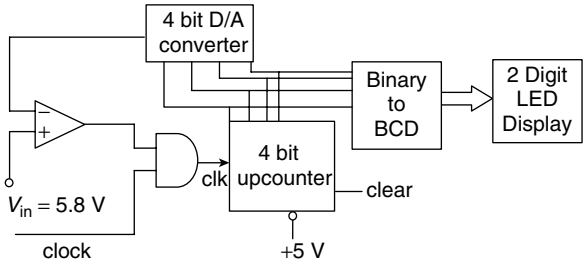


(A) −0.781 V (B) −1.562 V
(C) −3.125 V (D) −6.250 V

Direction for questions 9 and 10:

In the circuit comparator, output is logic '1'; if $V_1 > V_2$, the output is logic '0', otherwise. The D/A conversion is done as per the relation.

$V_{DAC} = \sum_{n=0}^{3} 2^{n-1}\ b_n$ volts, where b_3 (MSB), b_2, b_1, and b_0 are counter outputs. The counter starts from clear state.



9. The stable state of LED displays is
(A) 06 (B) 07 (C) 10 (D) 13

10. The magnitude of error between V_{DAC} and V_{in} at steady state in volts.
(A) 0.2 V (B) 0.7 V (C) 0.5 V (D) 0.1 V

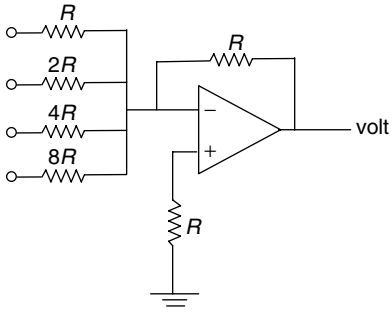
Practice Problems 2

Direction for questions 1 to 10: Select the correct alternative from the given choices.

1. The minimum number of comparators required to build *n* bit flash ADC is
(A) 2^{n-1} (B) $2n$ (C) 2^n (D) $2^n - 1$

2. If the resolution of D/A converter is approximately 5% of its full-scale range, then it is an
(A) 8-bit converter (B) 10-bit converter
(C) 12-bit converter (D) 16-bit converter

3. The circuit shown is a 4-bit DAC. The inputs 0 correspond to 0 V and 1 to 5 V. The op amp is ideal, but all the resistances and 5 V input have a tolerance of ±10%. The specification of tolerance for the ADC is



(A) ±35% (B) ±20% (C) ±10% (D) ±5%

4. A digital to analog converter with a full-scale output voltage of 3.5 V has a resolution close to 20 mV. Its bit size is
(A) 4 (B) 8 (C) 16 (D) 32

5. An 8-bit DAC has a full-scale output voltage of 15 V. The output voltage when the input is 10111010 is _____.
(A) 10.89 mV (B) 12 mV
(C) 12 V (D) 10.89 V

6. A 12-bit ADC is employed to convert an analog voltage 0 to 12 V, and the resolution of the ADC is
(A) 2.44 mV (B) 83.3 mV
(C) 2.92 mV (D) 1.0 mV

7. In a 4-bit weighted-resistor D/A converter, the resistor value corresponding to LSB is 4 kΩ, then the resistor value corresponding to the MSB will be?
(A) 32 kΩ (B) 16 kΩ (C) 1/4 kΩ (D) 1/2 kΩ

8. A 6-bit DAC is having output voltage of 4.2 V for input 101010. The full-scale reading of the DAC is
(A) 6.4 V (B) 6.3 V (C) 7.2 V (D) 8 V

9. Resolution of 4-bit ADC is 0.2 V for the input of 2.55 V. Therefore, the output stable state will be ?
(A) 1101 (B) 1011
(C) 1100 (D) 1110

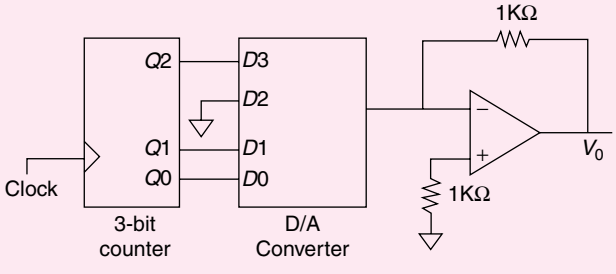
10. The correct order for most accurate, fastest, simplest design of ADCs, respectively,
(A) dual-scope ADC, flash-type ADC, SAR-type ADC
(B) SAR-type ADC, dual-scope ADC, flash-type ADC
(C) flash-type ADC, SAR-type ADC, counter-type ADC
(D) dual-scope ADC, flash-type ADC, counter-type ADC

Previous Years' Questions

1. A digital system is required to amplify binary-encoded audio signal. The user should be able to control the gain of the amplifier from a minimum to a maximum in 100 increments. The minimum number of bits required to encode in straight binary is **[2004]**

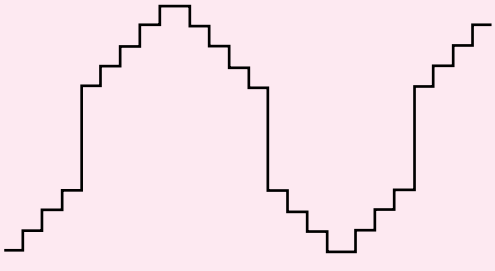
(A) 8 (B) 6 (C) 5 (D) 7

2. A 4-bit D/A converter is connected to a free-running 3-bit UP counter as shown in the following figure. Which of the following waveforms will be observed at V_0? **[2006]**

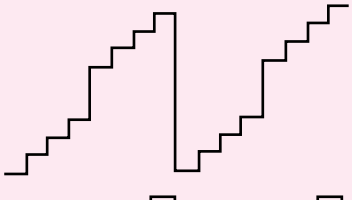


In the abovementioned figure, the ground has been shown by symbol ∇.

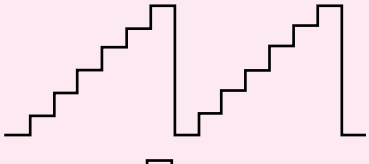
(A)



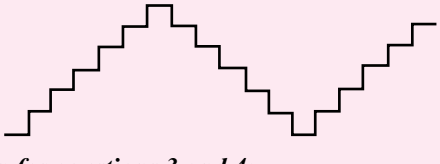
(B)



(C)

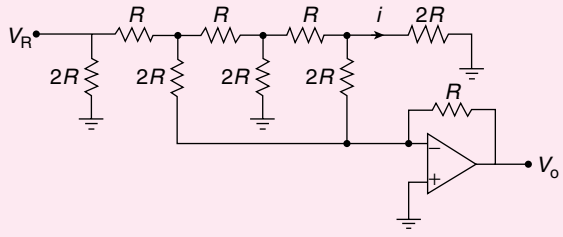


(D)



Direction for questions 3 and 4:

In the digital – to – analog converter circuit shown in the following figure, $V_R = 10$ V and $R = 10$ kΩ



3. The current I is **[2007]**

(A) 31.25 μA (B) 62.5 μA

(C) 125 μA (D) 250 μA

4. The voltage V_0 is **[2007]**

(A) –0.781 V (B) –1.562 V

(C) –3.125 V (D) –6.250 V

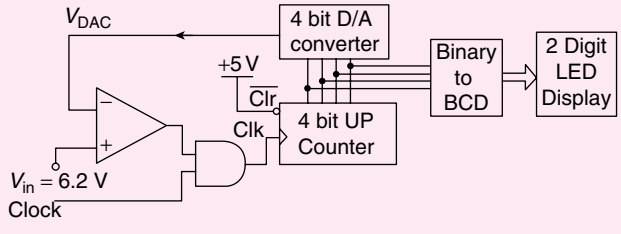
Direction for questions 5 and 6:

In the following circuit, the comparator output is logic '1' if $V_1 > V_2$ and the output is logic '0' otherwise. The D/A conversion is done as per the relations.

$$V_{DAC} = \sum_{n=0}^{3} 2^{n-1} b_n \text{ volts, where } b_3 \text{ (MSB)}, b_2, b_1, \text{and } b_0 \text{ (LSB)}$$

are the counter outputs.

The counter starts from the clear state.



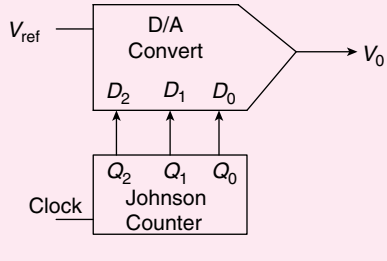
5. The stable reading of the LED display is **[2008]**

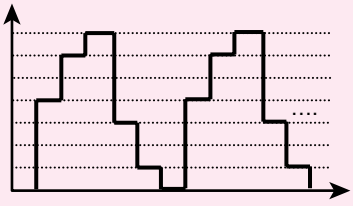
(A) 06 (B) 07 (C) 12 (D) 13

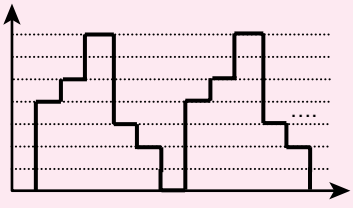
6. The magnitude of the error between V_{DAC} and V_{in} steady state in volts is **[2008]**

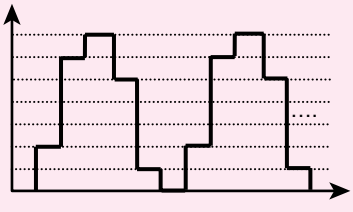
(A) 0.2 (B) 0.3 (C) 0.5 (D) 1.0

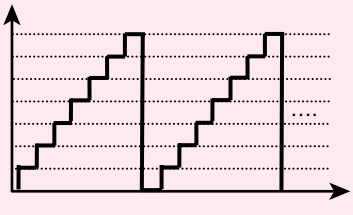
7. The output of a three-stage Johnson (twisted ring) counter is fed to digital–to–analog (D/A) converter, as shown in the following figure. Assume all states of the counter to be unset initially. The waveform that represents the D/A converter output V_0 is **[2011]**



(A) 

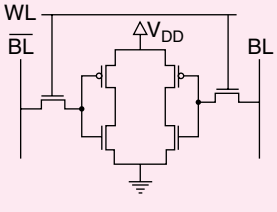
(B) 

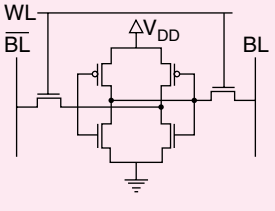
(C) 

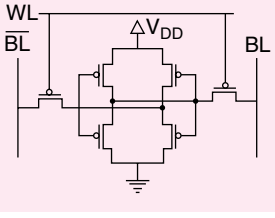
(D) 

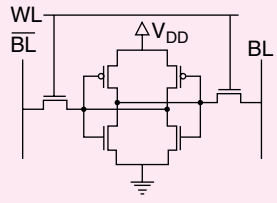
8. An analog voltage in the range 0–8 V is divided in 16 equal intervals for conversion to 4-bit digital output. The maximum quantization error (in volts) is _____ **[2014]**

9. If WL is the Word Line and BL the Bit Line, an SRAM cell is shown in **[2014]**

(A) 

(B) 

(C) 

(D) 

10. For a given sample-and-hold circuit, if the value of the hold capacitor is increased, then **[2014]**

(A) droop rate decreases and acquisition time decreases

(B) droop rate decreases and acquisition time increases

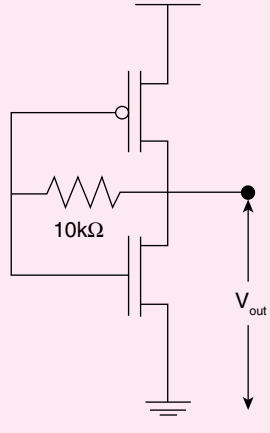
(C) droop rate increases and acquisition time decreases

(D) droop rate increases and acquisition time increases

11. A 16 Kb (=16,384 bit) memory array is designed as a square with an aspect ratio of one (number of rows is equal to the number of columns). The minimum number of address lines needed for the row decoder is _____. **[2015]**

12. Consider a four-bit D to A converter. The analogue value corresponding to digital signals of values 0000 and 0001 are 0 V and 0.0625 V, respectively. The analogue value (in volts) corresponding to the digital signal 1111 is _____. **[2015]**

13. What is the voltage V_{out} in the following circuit? **[2016]**



(A) 0V

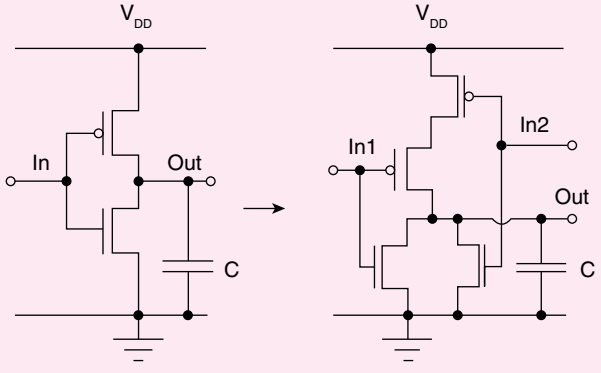
(B) V_T of PMOS + V_T of NMOS)/2

(C) Switching threshold of inverter

(D) V_{DD}

14. Transistor geometries in a CMOS inverter have been adjusted to meet the requirement for worst case charge and discharge times for driving a load capacitor C. This design is to be converted to that of a NOR circuit in the same technology, so that its worst case charge and discharge times while driving the same capacitor

are similar. The channel lengths of all transistors are to be kept unchanged. Which one of the following statements is correct? **[2016]**



(A) Widths of PMOS transistors should be doubled, while widths of NMOS transistors should be halved.

(B) Widths of PMOS transistors should be doubled, while widths of NMOS transistors should not be changed.

(C) Widths of PMOS transistors should be halved, while widths of NMOS transistors should not be changed.

(D) Widths of PMOS transistors should be unchanged, while widths of NMOS transistors should be halved.

15. An 8k Byte ROM with an active low Chip Select input $(\overline{CS})$ is to be used in an 8085 microprocessor based system. The ROM should occupy the address range 1000H to 2FFFH. The address lines are designated as A_{15} to A_0, where A_{15} is the most significant address bit.

Which one of the following logic expressions will generate the correct $\overline{CS}$ signal for this ROM? **[2016]**

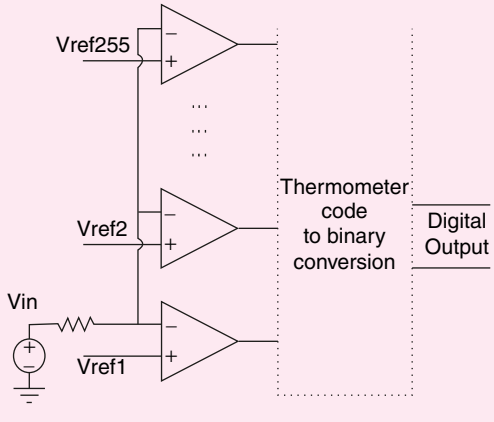
(A) $A_{15} + A_{14} + (A_{13}A_{12} + \overline{A_{13}}\ \overline{A_{12}})$

(B) $A_{15}A_{14}(A_{13} + A_{12})$

(C) $\overline{A_{15}}\ \overline{A_{14}}\left(A_{13}\overline{A_{12}} + \overline{A_{13}}A_{12}\right)$

(D) $\overline{A_{15}} + \overline{A_{14}} + A_{13}A_{12}$

16. In an N bit flash ADC, the analog voltage is fed simultaneously to $2^N - 1$ comparators. The output of the comparators is then encoded to a binary format using digital circuits. Assume that the analog voltage source V_{in} (whose output is being converted to digital format) has a source resistance of 75Ω as shown in the circuit diagram below and the input capacitance of each comparator is 8pF. The input must settle to an accuracy of $\frac{1}{2}$LSB even for a full scale input change for proper conversion. Assume that the time taken by the thermometer to binary encoder is negligible. **[2016]**



If the flash ADC has 8 bit resolution, which one of the following alternatives is closest to the maximum sampling rate?

(A) 1 megasamples per second

(B) 6 megasamples per second

(C) 64 megasamples per second

(D) 256 megasamples per second

Answer Keys

Exercises

Practice Problems 1

1. B	**2.** B	**3.** B	**4.** B	**5.** D	**6.** A	**7.** D	**8.** C	**9.** D	**10.** B

Practice Problems 2

1. D	**2.** A	**3.** A	**4.** B	**5.** D	**6.** C	**7.** D	**8.** B	**9.** A	**10.** D

Previous Years' Questions

1. D	**2.** B	**3.** B	**4.** C	**5.** D	**6.** B	**7.** A	**8.** 0.25 V	**9.** B	**10.** B
11. 7	**12.** 0.93 to 0.94		**13.** C	**14.** B	**15.** A	**16.** A			