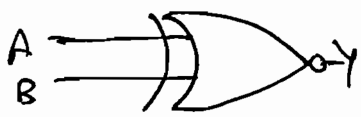
☆ Logic Gate:

→ AND, OR, NAND, NOR, EX-OR, EX-NOR gates.

→ NAND & NOR are Universal gates.

① Equavalance | coincidence gate
⇒ ExNOR gate

→ 

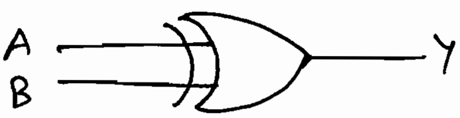
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

$$\boxed{Y = A \odot B}$$

$$\therefore \boxed{Y = \bar{A}\cdot\bar{B} + A\cdot B}$$

② Staircase Connection :-
⇒ Ex-OR gate Logic

→

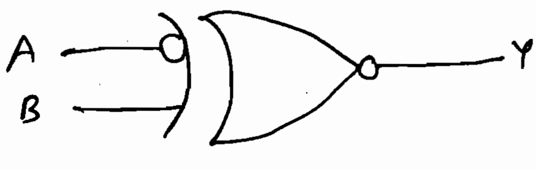


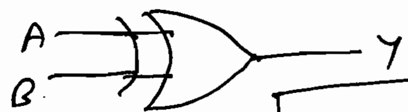
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

$$\boxed{Y = A \oplus B}$$

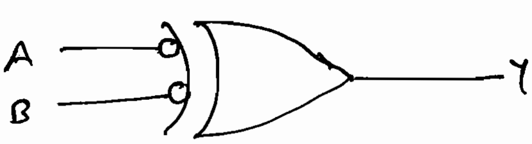
$$\boxed{Y = \bar{A}\cdot B + \bar{B}\cdot A}$$

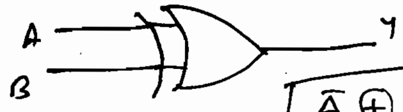
③

ⓐ 

= 

$$\boxed{\bar{A}\odot B = A \oplus B}$$

ⓑ 

= 

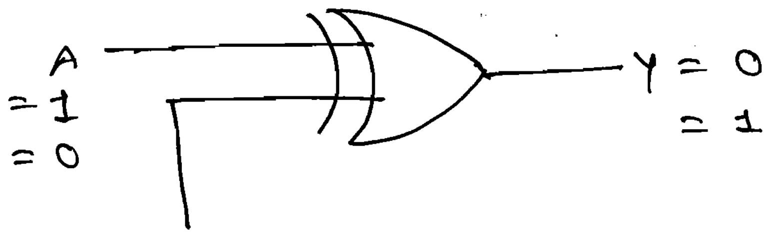
$$\boxed{\bar{A}\oplus\bar{B} = A \oplus B}$$

→ $\boxed{A \oplus \bar{B} = A \odot B}$

④ Min no. of gates

	NAND	NOR
Ex-OR	4	5
EX-NOR	5	4

⑤



Control

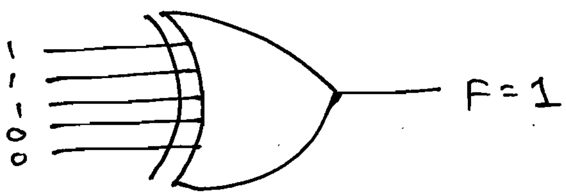
'x' = 1

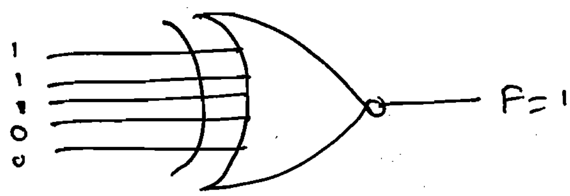
If $x = 1 \rightarrow Y = \bar{A}$ (Inverter)

$x = 0 \rightarrow Y = A$ (Buffer).

NOTE: For X-NOR it reverse.

⑥





$1 \oplus 1 \oplus 1 \oplus 0 \oplus 0 = 1$

↓

$1 \odot 1 \odot 1 \odot 0 \odot 0 = 1.$

NOTE:

→ Ex-OR output = 1 if Input has odd no of 1's

→ Ex-NOR Output = 1 if Input has Even no. of 0's.

→ $\boxed{\text{Ex-NOR} = \text{EX-OR}}$ if no. of Input Variables are odd.

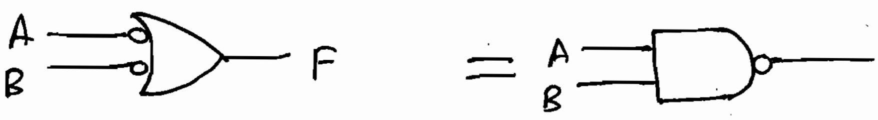
E.g. = $A \oplus B \oplus C = A \odot B \odot C$.

→ $\boxed{\text{Ex-NOR} = \overline{\text{EX-OR}}}$ if no. of Input Variables are even.

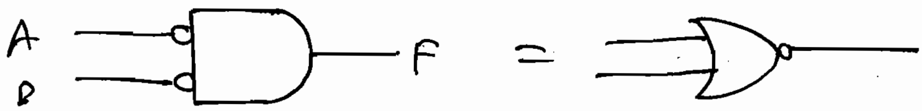
E.g. = $A \odot B \odot C \odot D = \overline{A \oplus B \oplus C \oplus D}$

7 Bubbled gates (Negative gates)

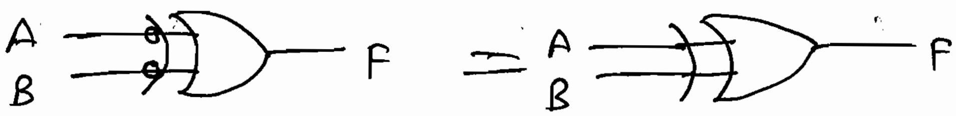
a Bubbled OR gate = NAND gate



b Bubbled AND gate = NOR gate

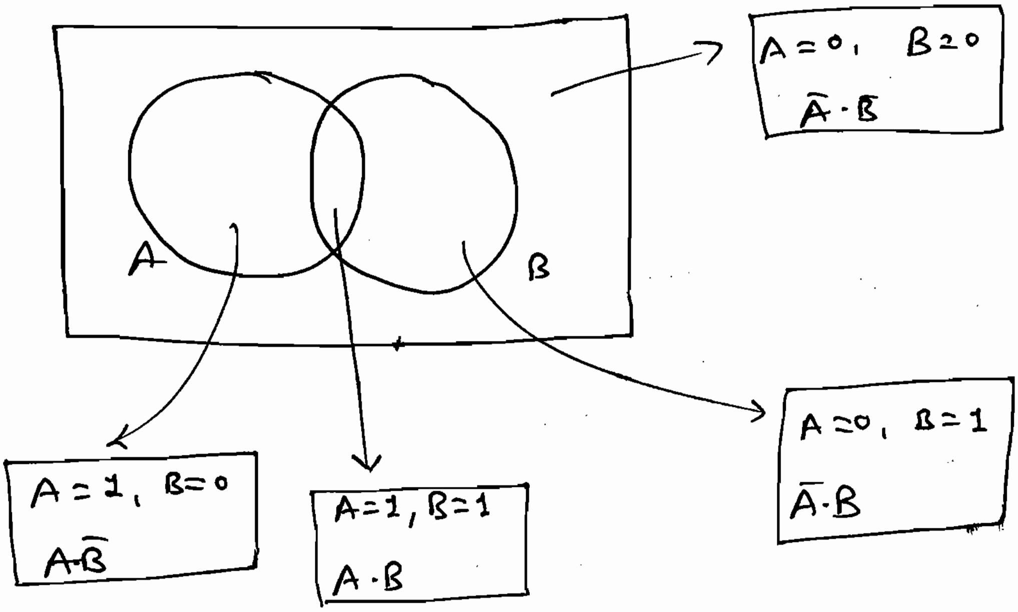


c Bubbled Ex-OR = Ex-OR gate

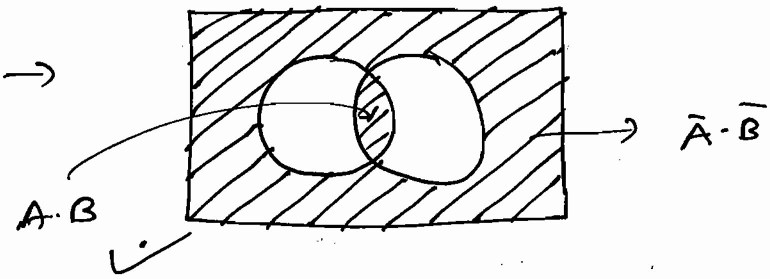


⑧ Venn diagrams:

→ NOTE:



→

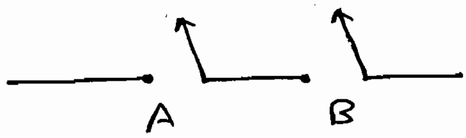


$F = \bar{A}\cdot\bar{B} + A\cdot B$

$F = A \odot B$ → Ex-NOR gate

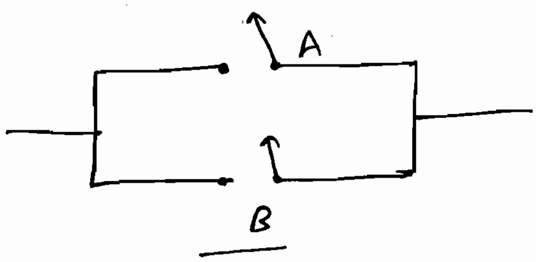
⑨

ⓐ



⇒ $F = A\cdot B$. AND

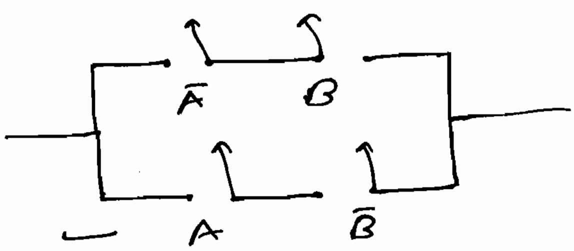
ⓑ



⇒ $F = A + B$. OR

*

ⓒ



⇒ $F = \bar{A}B + A\bar{B}$

Ex-OR

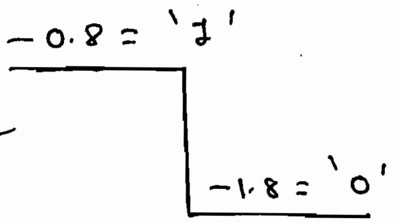
F = Ex-OR gate.

(10) Positive Logic   Negative Logic

e.g. ECL Logic

$\Rightarrow$ '0' = −1.8

'1' = −0.8



$\rightarrow$ Positive Logic.

NOTE: In negative logic, more negative value treated as logic '1' state. ~~ex~~ for e.g. −1.8 → Logic '1', −0.8 → as logic '0'.

Ex-1 (a) If $A \cdot B = 0$; EX-OR gate behaves ______ logic gates?

$\rightarrow$ $A \cdot B = 0$ $A \cdot B = 1$

$\Rightarrow$ $A = 0,\ B = 1$ $A = 1,\ B = 1$

$A = 1,\ B = 0$

$A = 0,\ B = 0$

$$\therefore\ A \oplus B = A\bar{B} + \bar{A}B = \overline{AB + \bar{A}\bar{B}}$$

$$= \overline{0 + \bar{A}\bar{B}}$$

$$= A + B$$

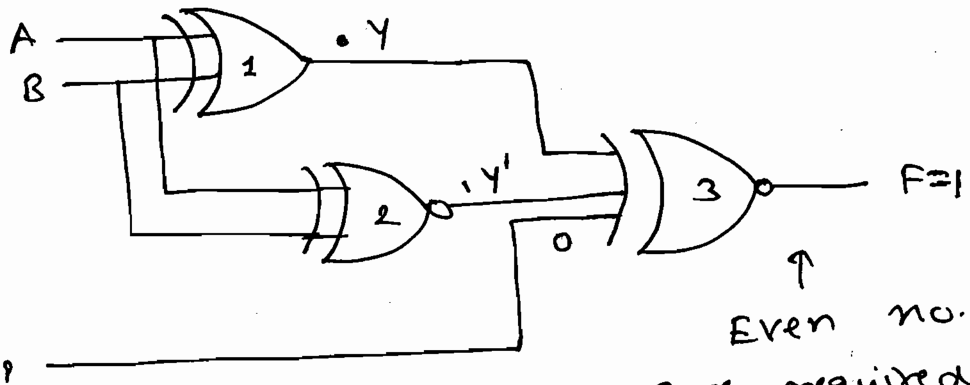
$$= \text{OR gate}$$

Imp NOTE:

In TTL Logic family open input is accepted by the logic gate as '1'

see: Page-133, Q-30 of IES '13 Book ACE Academy.

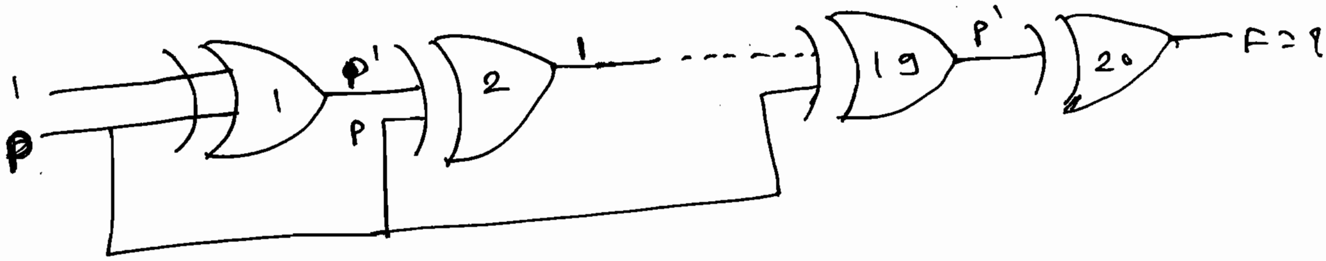
(b) Find the value of $C = ?$



$C = 0$.

↑ Even no. of zeros are required at gate-3 to get $F = 1$.

(c) Find output $F = ?$



~~for~~ P' $F = 1$.

→ output at even gate is 1 and at odd gate is P'

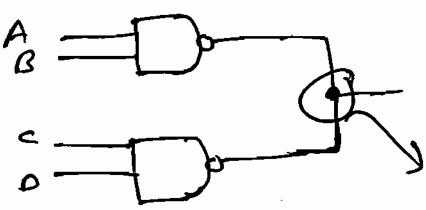
→ After even no. gates → O/P ⇒ 1 } → if IP = 1.

After 20 gates → O/P = 1.

if initial condition is reverse that 1 become 0 then it act as a buffer.

NOTE: Open collector TTL will provide wired-AND operation.

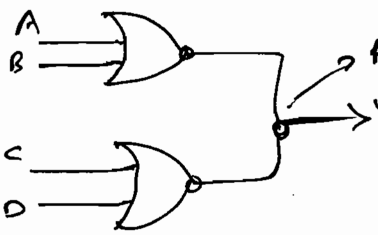
for eg.



$F = \overline{A \cdot B} \cdot \overline{C \cdot D}$

AND operation.

(2)



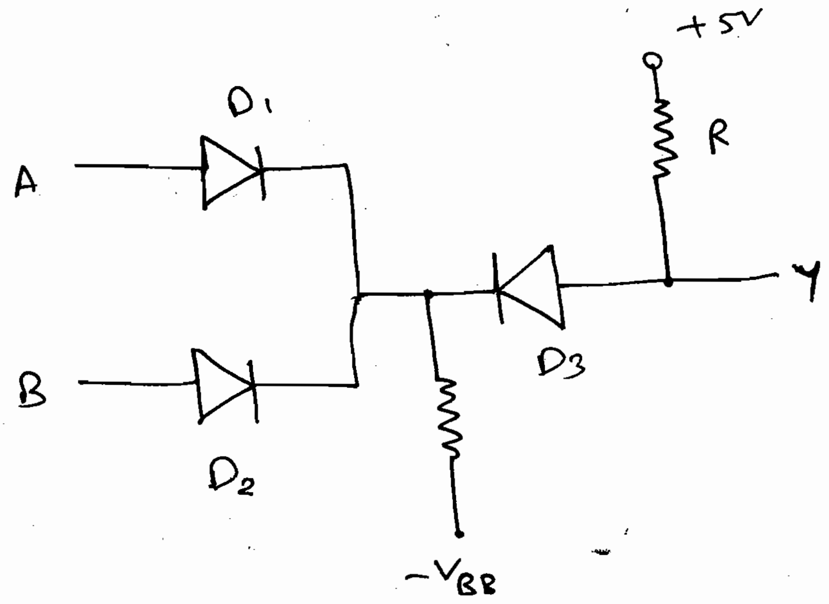
$Y = \overline{A+B} \cdot \overline{C+D}$

Ex - 2 Determine the Logic represented by the following ckt.

(a) in +ve Logic.

(b) in -ve logic.

→



A	B	Y	
0	0	0 V	D_1, D_2, D_3 are ON.
+0	+5	+5 V	D_2 ON, D_1 & D_3 are OFF
+5	0	+5 V	D_1 ON, D_2 & D_3 are OFF
+5	+5	+5 V	D_1, D_2 ON, D_3 OFF.

$Y = A + B$ = OR gate.

(a) Positive logic.

+5 V → '1'

0 V → '0'

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

⇒ OR gate.

(b) Negative Logic

$+5 \rightarrow$ '0'

$0 \rightarrow$ '1'

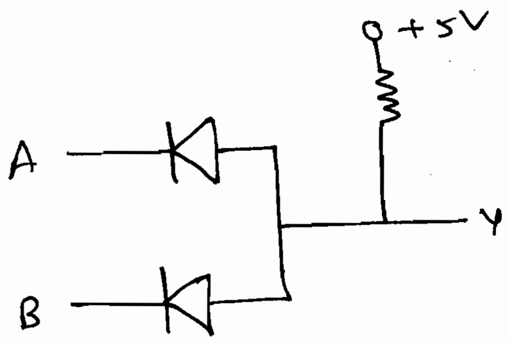
A	B	F
1	1	1
1	0	0
0	1	0
0	0	0

$\Rightarrow$ AND gate.

NOTE: (i) $\boxed{\text{+ve logic OR gate = -ve logic AND gate}}$

+ve logic		-ve logic
AND	$\longrightarrow$	OR
OR	$\longrightarrow$	AND
NAND	$\longrightarrow$	NOR
NOR	$\longrightarrow$	NAND
EX-OR	$\longrightarrow$	EX-NOR
EX-NOR	$\longrightarrow$	EX-OR.

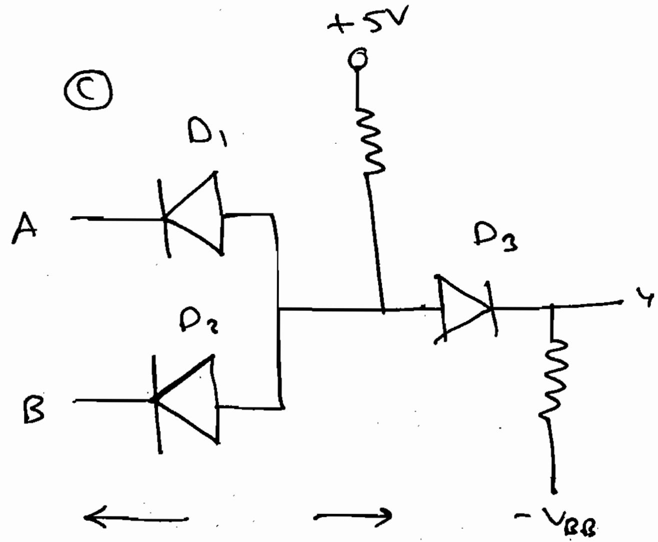
(b)



$\leftarrow$

AND gate

(c)



AND gate

NOTE:

a) Diode pointing $\boxed{\text{outwards}}$ $\Rightarrow$ $\boxed{\text{AND gate.}}$

b) Diodes pointing $\boxed{\text{Inwards}}$ $\Rightarrow$ $\boxed{\text{OR gate.}}$