# Test

## Computer Organization and Architecture

**Time: 60 min.**

***Directions for questions 1 to 30:*** Select the correct alternative from the given choices.

**1.** Which of the following register keeps track of instruction execution sequence?
(A) Accumulator (B) Program counter
(C) Stack pointer (D) Instruction register

**2.** Consider the following Register Transfer Language:

$$R_1 \leftarrow R_1 + M[R_2 + R_3]$$

Where $R_1$, $R_2$ and $R_3$ are the CPU registers and '$M$' is a memory location in primary memory, which addressing mode is suitable for above register transfer language?
(A) Indirect (B) Direct
(C) Indexed (D) Displacement

**3.** Which of the following is/are advantage(s) of using a multiple-bus architecture over a single-bus architecture?
(i) Multiple-bus architecture reduces propagation delay.
(ii) Multiple-bus architecture reduces bottleneck effects.
(A) (i) only (B) (ii) only
(C) Both (i) and (ii) (D) Neither (i) nor (ii)

**4.** Which of the following statement is false with respect to Booth's Multiplication Algorithm?
(i) Corrections required for the final result.
(ii) Sign bit is protected due to internal arithmetic shift.
(iii) More space required to maintain the sum.
(A) (i), (ii) only (B) (ii), (iii) only
(C) (i), (iii) only (D) (i), (ii), (iii)

**5.** After selective complement of $A = 1100$ with $B = 0101$, the resultant $A$ will be
(A) 0000 (B) 1100
(C) 0101 (D) 1001

**6.** Which type of shift operation always keeps the sign bit unchanged?
(A) Logical shift (B) Arithmetic shift
(C) Circular shift (D) Any right shift

**7.** Consider the register transfer language instructions:

$AC \leftarrow M[R_1]$;

$R_1 \leftarrow R_1 + 1$;

Which addressing mode is specified by the instructions?
(A) Register addressing mode
(B) Register indirect mode
(C) Auto-increment mode
(D) Relative mode

**8.** Which of the following statement is true?
(A) Floating point representation is better than fixed point representation.
(B) Fixed point representation is better than floating point representation.
(C) Datapath is same as ALU.
(D) Both (A) and (C)

**9.** Which of the following statements correctly specifies about overflow?
(i) When adding two unsigned numbers the carry-out, from the MSB position serves as the overflow indicator.
(ii) Overflow can occur only by adding two signed numbers that have the same sign.
(A) (i) only (B) (ii) only
(C) Both (i) and (ii) (D) Neither (i) nor (ii)

**10.** A certain processor supports only the immediate and direct addressing modes. Which of the following programming language features cannot be implemented on this processor?
(A) Pointers (B) Arrays
(C) Records (D) All of these

**11.** The special purpose storage location(s) used by both ALU and CU are
(A) Decoders (B) Demultiplexers
(C) Registers (D) Buffers

**12.** Which of the following is a component of the datapath of Von Neumann machine?
(i) Registers
(ii) ALU input bus
(iii) ALU I/O registers
(A) (i), (ii) only (B) (ii), (iii) only
(C) (i), (ii), (iii) (D) None of these

**13.** Which of the following is/are false with respect to single-bus datapath?
(i) It is simplest and least expensive.
(ii) No limit on the amount of data transfer in a single clock cycle.
(A) (i) only (B) (ii) only
(C) Both (i) and (ii) (D) Neither (i) nor (ii)

**14.** If we have shifted the significant to the right by a single position, then
(A) Add one to the exponent
(B) Subtract one from the exponent
(C) Don't change the exponent
(D) Data insufficient

**15.** In which addressing mode, the effective address of the operand is generated by adding a constant value to the content of a register?
(A) Absolute mode (B) Indirect mode
(C) Immediate mode (D) Index mode

**16.** What is the number of instructions required to add '$n$' numbers and store the result in memory using only one-address instructions?
(A) $n$ (B) $n-1$
(C) $n+1$ (D) independent of $n$

**17.** Which unit of a computer system executes program, communicates with and often controls the operation of other subsystems?
(A) CPU (B) ALU
(C) I/O module (D) DMA

**18.** The multiplicand register and multiplier register of a hardware circuit implementing booth's algorithm have 1001 and 1100 respectively. The resultant will be
(A) 10011100 (B) 00011100
(C) 01101100 (D) 00010010

**19.** A floating point number has sign bit 0, Excess-64 exponent is 1010100 and fractional part is 0000000000011011. After converting this number to normalized form, the exponent (in decimal) will be
(A) 20 (B) 9
(C) 31 (D) 0

**20.** In IEEE floating point single precision representation, the number of bits in the fractional part is
(A) 24
(B) 23
(C) 32
(D) Depends on the architecture

**21.** After multiplying the binary numbers 010111 and 110110 using booth's multiplication algorithm, the resultant will be
(A) –1242 (B) 1242
(C) 230 (D) –230

**22.** The IEEE standard 754 single precision floating point representation of $(0.000001101101001 01)_2$ is.
(A) 0 10000111 11011010010100000000000
(B) 0 01111001 11011010010100000000000
(C) 0 10000110 10110100110100000000000
(D) 0 01111000 10110100101000000000000

**23.** How many clock cycles are required to perform two-operand operations using one bus datapath?
(A) 1 (B) 2
(C) 3 (D) Can't be determined

**24.** Which of the following is a rounding mode in IEEE754 standard?
(i) round to 0
(ii) round towards $+\infty$
(iii) round towards $-\infty$
(iv) round to nearest representable number
(A) (i), (iv) only (B) (ii), (iii) only
(C) (i), (ii) only (D) (i), (ii), (iii), (iv)

**25.** What is the normalized form of $0.00000110 \times 16^{101}$?
(A) $1.10 \times 16^{107}$ (B) $1.10 \times 16^{95}$
(C) $0.110 \times 16^{94}$ (D) $0.110 \times 16^{106}$

**26.** What is the biased representation of –7, using 4-bits for the bias?
(A) 0111 (B) 1111
(C) 0000 (D) 1001

**27.** What is the total resultant after adding $A = -7$ and $B = -6$ using signed two's complement representation?
(A) 0100 (B) 11101
(C) 1101 (D) Overflow occurs

**28.** What is the total number of additions and subtractions required using Booths multiplication algorithm for the multiplier 00011110?
(A) 1 (B) 2
(C) 30 (D) Can't be determined

**Common data questions 29 and 30:** Consider a 12-bit floating point format in which base $b = 2$, a 5-bit exponent $e$ with $a$ bias = 16 and 6-bit normalized mantissa $m$. Given two floating point numbers:

$A = 0\ 10001\ 011011$
$B = 1\ 01111\ 101010$

**29.** After adding $A$ and $B$, the resultant will be
(A) 1 10001 000000
(B) 1 10001 000001
(C) 0 10001 000000
(D) 0 10001 000001

**30.** After subtracting $B$ from $A$, the resultant will be
(A) 1 10001 110101 (B) 0 10001 110101
(C) 1 10001 110110 (D) 0 10001 110110

## Answers Keys

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|---|---|---|---|---|---|---|---|---|---|
| **1.** B | **2.** C | **3.** C | **4.** C | **5.** D | **6.** B | **7.** C | **8.** A | **9.** C | **10.** D |
| **11.** C | **12.** C | **13.** B | **14.** A | **15.** D | **16.** C | **17.** A | **18.** B | **19.** B | **20.** B |
| **21.** D | **22.** D | **23.** B | **24.** D | **25.** B | **26.** C | **27.** D | **28.** B | **29.** C | **30.** D |