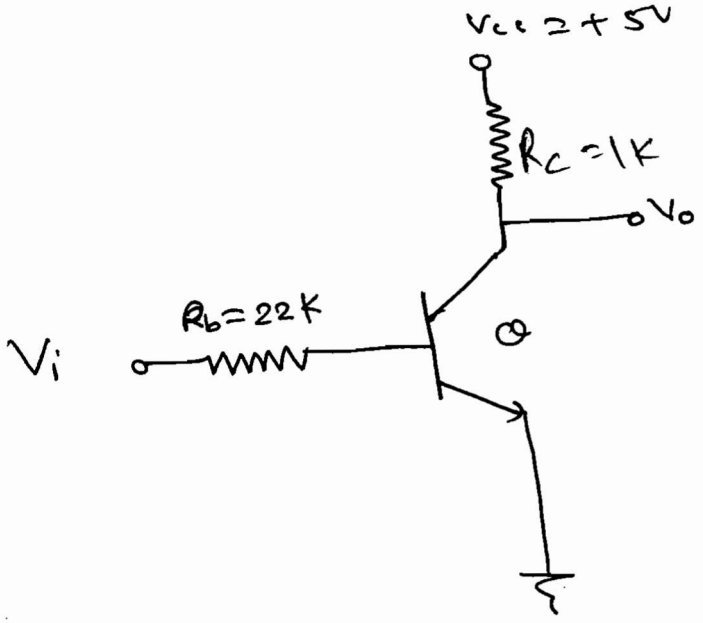
✡ Logic Families:

* Transistor as an Inverter:



$V_{BE,cutoff} = 0.8V$

$V_{BE,active} = 0.7V$

$V_{BE,sat} = 0.8V$

(i) $V_i = 0V$; Q is OFF $\Rightarrow$ $V_o = +5V$.

(ii) $V_i = +5V$; Q is ON $\Rightarrow$ $V_o = V_{CE,sat} = 0.2$.

$\rightarrow$ $I_B \geq I_{B,min}$. where $I_{B,min} = \frac{I_{C,sat}}{h_{FE}}$.

$\therefore$ $I_B \geq \frac{I_{C,sat}}{h_{FE}}$.

$\therefore$ $\boxed{h_{FE} I_B \geq I_{C,sat}}$ $\rightarrow$ For Q to be in Saturation.

$\rightarrow$ $I_{C,sat} = \frac{V_{CC} - V_{CE,sat}}{R_C} = \frac{5 - 0.2}{1K} = 4.8\ mA.$

$\therefore$ $I_B = \frac{V_i - V_{BE,sat}}{R_b} = \frac{5 - 0.8}{22} = \frac{4.2}{22} = 0.19\ mA$

$\therefore$ $h_{FE} I_B = (20)(0.19) = \boxed{3.8\ mA.}$

because

NOTE: In the above circuits If $h_{FE} = 30$ then

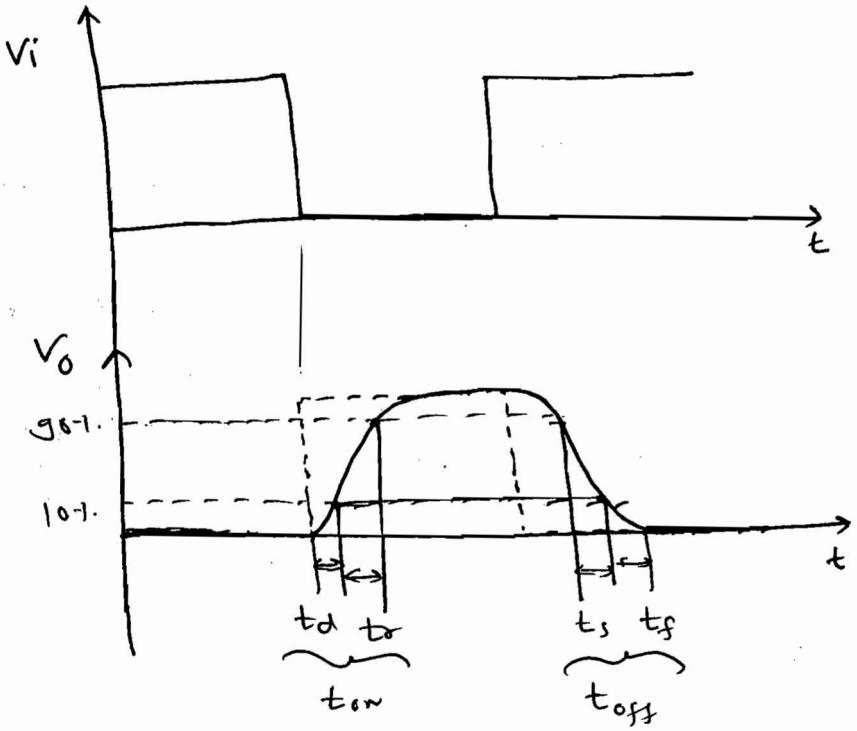
then $h_{FE} I_B = (30)(0.19) = 5.7\,mA.$

$\therefore \boxed{I_{C\,sat} = 4.8\,mA.}$

So, Transistor is in saturation, because

$h_{FE} I_B > I_{C\,sat}.$

* Transistor switching time:



t_d = delay time.

t_r = Rise time.

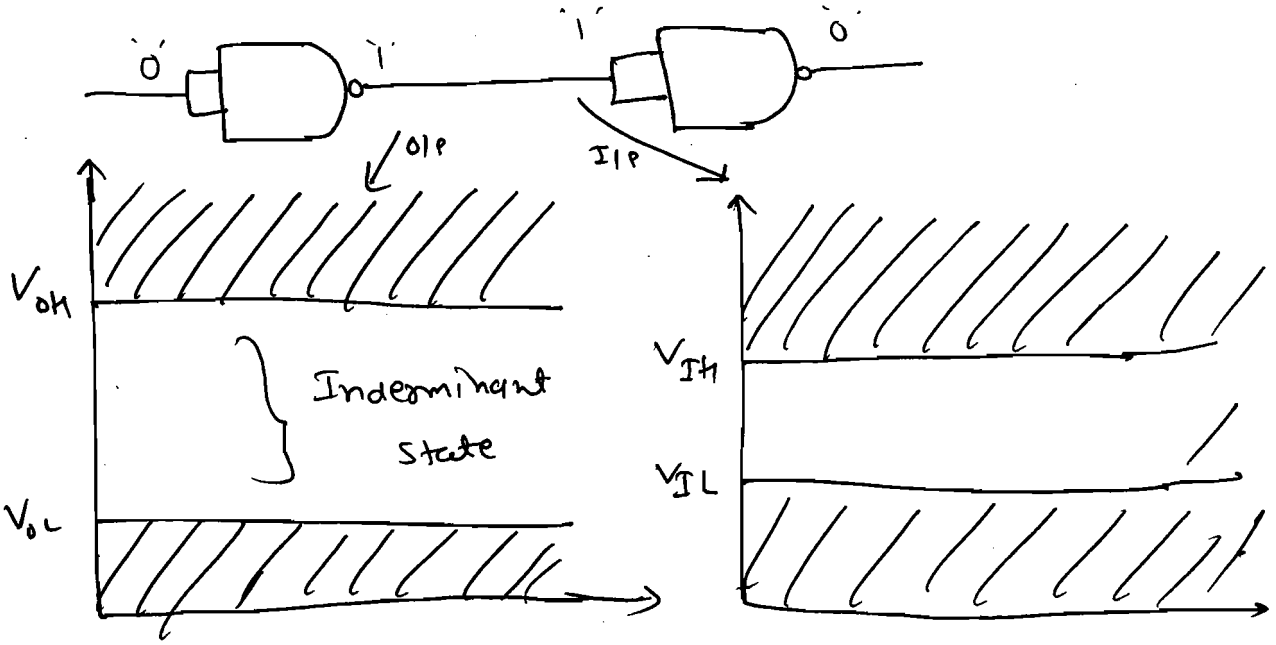
t_s = Storage time.

t_f = fall time.

→ $t_{ON} = t_d + t_r$.

$t_{OFF} = t_s + t_f$.

* Parameter of Logic gates:



$$V_{OH} > V_{IH} > V_{IL} > V_{OL}.$$

2) Noise margin:

→ It is the amount of noise that can be allowed without disturbing the normal operation of logic gates.

$$NM_H = V_{OH} - V_{IH} = 2.4 - 2.0 = \boxed{0.4V}$$ ↑ (-ve noise)

$$NM_L = V_{IL} - V_{OL} = 0.9 - 0.4 = \boxed{0.5V}$$ → (+ve noise)

$$\therefore N.M. = \min(NM_H, NM_L).$$

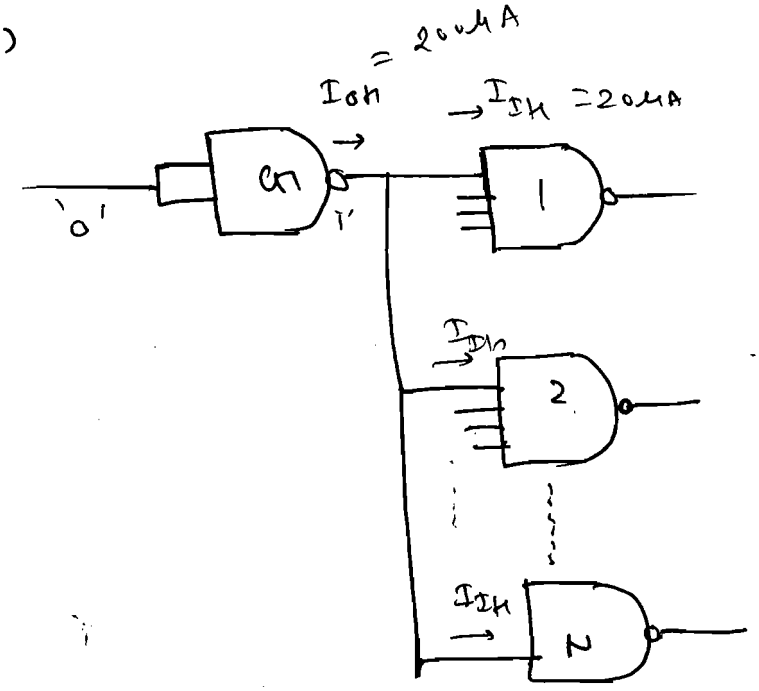
$$= \min(0.5, 0.4).$$

$$\therefore \boxed{NM = 0.4V}$$

③ Fanout:

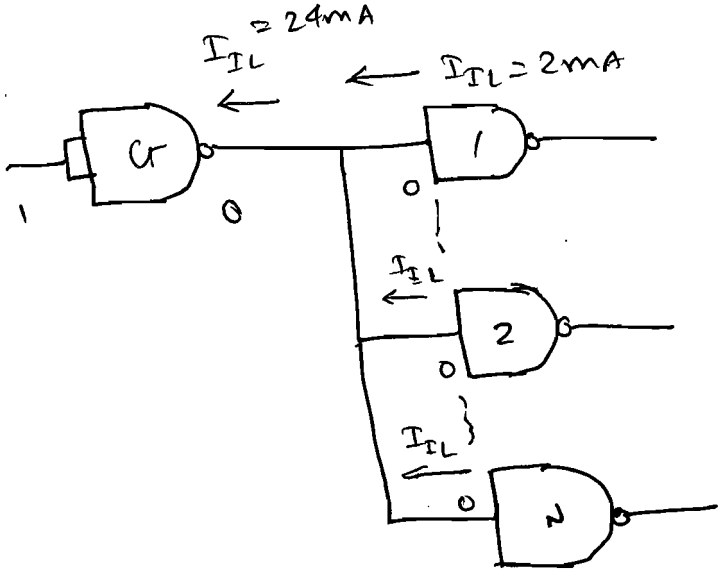
→ It is the no. of standard load o/p of gate can drive without impairing its normal operation. The standard load is input current of a logic gate which belongs to the the family of driving gate.

(a)



$$\text{Fan out}_H = \frac{I_{OH}}{I_{IH}} = 10.$$

(b)



$$\text{Fan out}_L = \frac{I_{OL}}{I_{IL}}$$

$$= \frac{24}{2}$$

$$\text{Fan out}_L = 12$$

→ Fanout = min (Fanout$_H$, Fanout$_L$).

= min (10, 12)

∴ **Fanout = 10**

(4) FOM (figure of Merit).

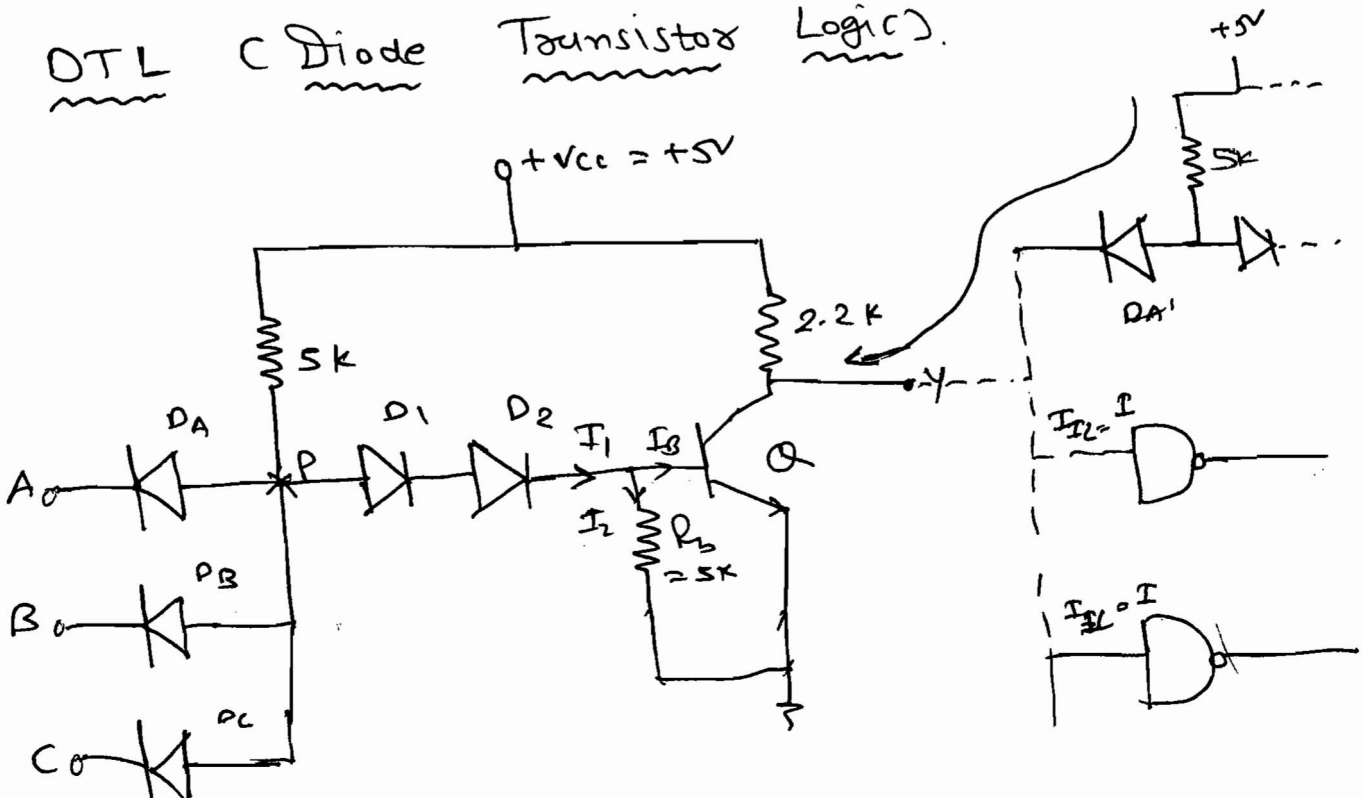
→ Prop. delay (ns) X power dissipation (mW)

=> picojoules (PJ).

→ It is used to compare two gates in terms of its performance.

→ (1) DTL
(2) modified DTL
(3) TTL
(4) ECL.

(1) DTL (Diode Transistor Logic).



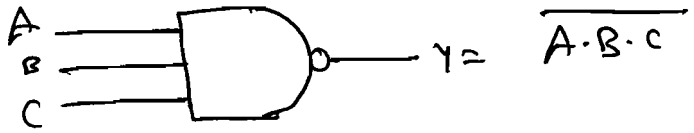
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

D_A, D_B, D_C are ON
D_1, D_2, Q are OFF $\Rightarrow Y = +5V$.

D_1, D_2, Q are OFF $\Rightarrow Y = +5V$

D_A, D_B, D_C are OFF
D_1, D_2 & Q are ON,
$Y = V_{CE,sat} = 0.2V$.

So, it is NAND gate.



→ (i) when Q is on the voltage at P

$V_P = 0.7 + 0.7 + 0.8 = \boxed{2.2\ V.}$

(ii) when Q is OFF $\Rightarrow V_P = 0.7 + 0.2 = \boxed{0.9V}$

→ For 'Q' to be in saturation.

$h_{FE} I_B \geq I_{C,sat} + N.I.$

$I_{C,sat} = \dfrac{5 - V_{CE,sat}}{2.2} = \dfrac{4.8}{2.2} = \boxed{2.18\ mA.}$

$$I = \frac{5 - V_A' - V_{CE,sat}}{5} = \frac{5 - 0.7 - 0.2}{5}.$$

$$\therefore \quad I = \frac{4.1}{5} = \boxed{0.82\,mA}$$

$$\rightarrow \quad I_1 = \frac{5 - V_P}{5} = \frac{5 - 2.2}{5}.$$

$$\therefore \quad I_1 = \frac{2.8}{5} = \boxed{0.56\,mA}$$

$$\rightarrow \quad I_2 = \frac{V_{BE,sat}}{R_b} = \frac{0.8}{5} = \boxed{0.16\,mA}$$

$$\therefore \quad I_B = I_1 - I_2 = 0.56 - 0.16$$

$$\therefore \quad \boxed{I_B = 0.4\,mA}$$

Let, $h_{FE} = 30$.

$$\therefore \quad 30 \times 0.4m \geq 2.18m \times N + N.(0.82)m$$

$$\therefore \quad 12 + 2 \geq 2.18 + (0.82 \times N)$$

$$\therefore \quad 9.82 \geq 0.82 \times N$$

$$\therefore \quad N \leq \frac{9.82}{0.82}.$$

$$\therefore \quad N = 11.97$$

$$\therefore \quad \boxed{N = 11}$$

$$\therefore \quad \boxed{\text{Fanout} = 11}$$

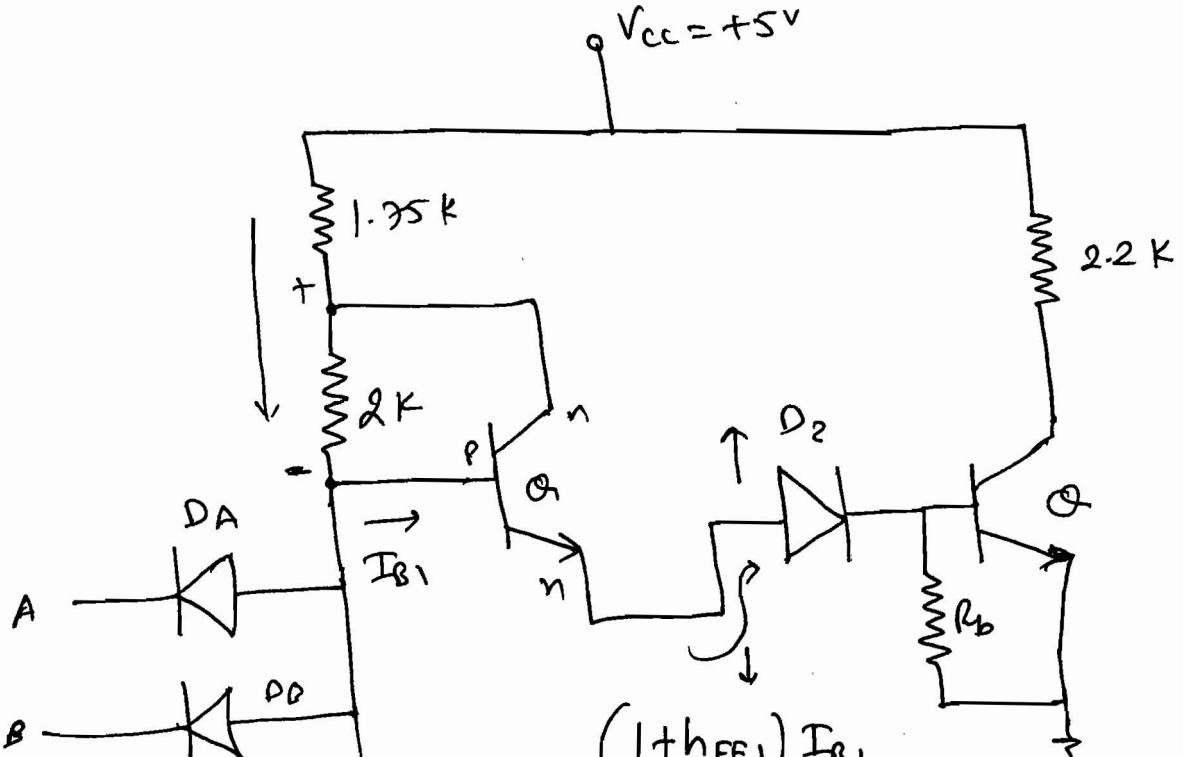
→ In OTL two Diodes D_1 & D_2 are used to increase the noise margin of the logic gates.

→ ~~At~~ In OTL, the R_b resistor is used to reduce the Storage time of the transistor which in turn reduces the switch off time of the transistor.

(2) Modified OTL Gate:

→ In modified DTL the Diode D_1 is replaced by a transistor in active region which increases the base current of Q. hence the fanout of the Logic increases

→

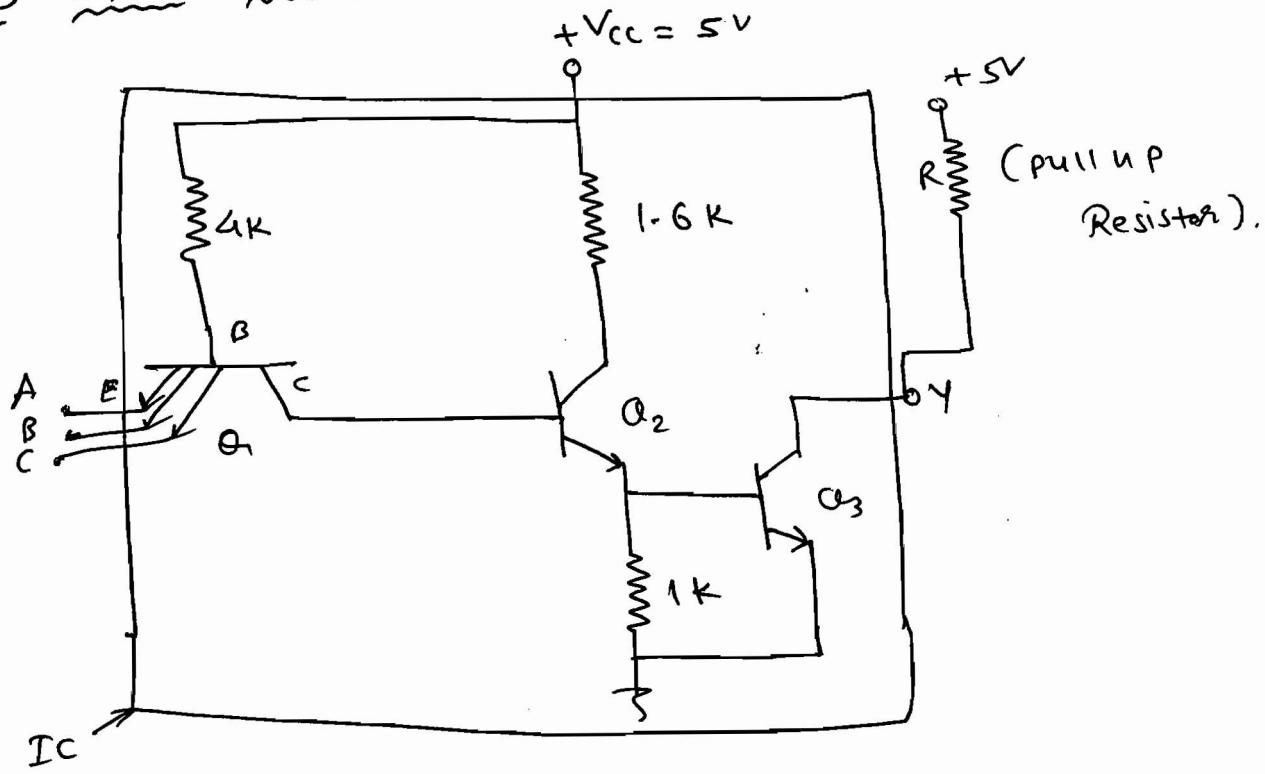


→ 'Q' is in Active region.

(3) TTL : (Transistor Transistor Logic). (saturated).

→ (a) open Collector.
(b) Totempole.
(c) Tri-state.

→ (a) open collector.

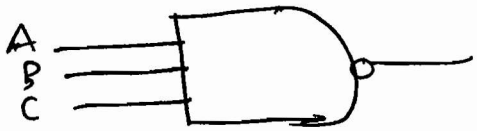


A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

→ Q1 is in forward Active region mode
Q2 and Q3 are OFF ⇒ Y = +5V

→ Q1 is in Reverse active

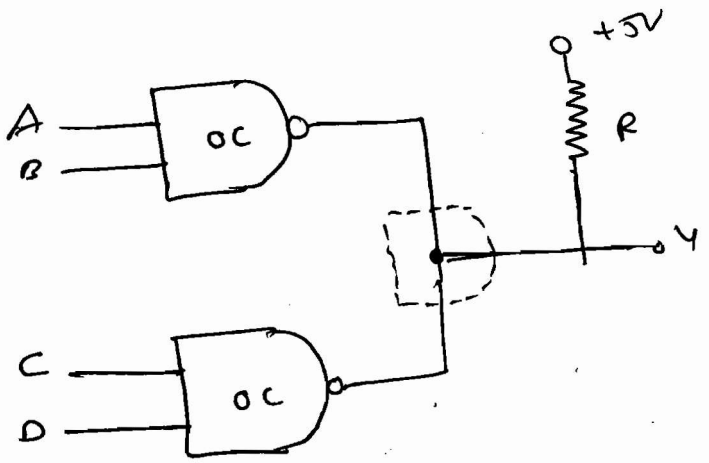
→ So, it is NAND gate.

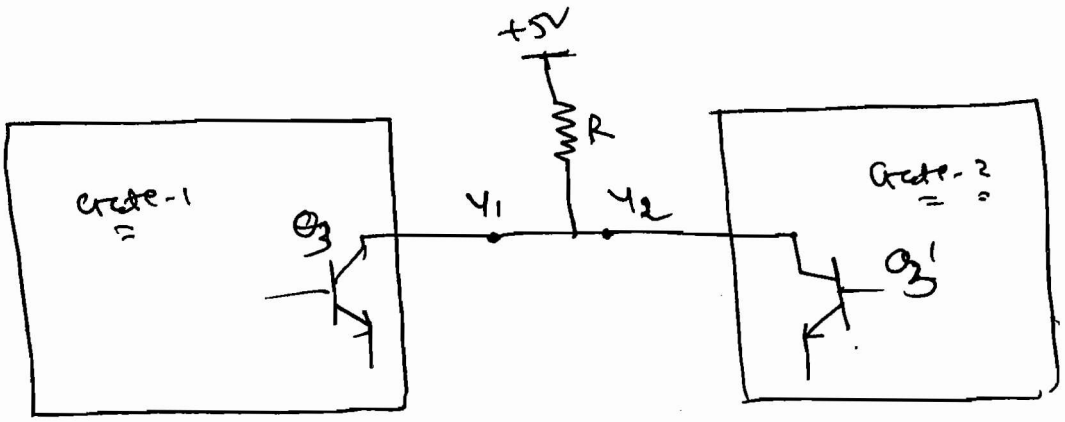


* Advantages:

→ (1) Open Collector TTL

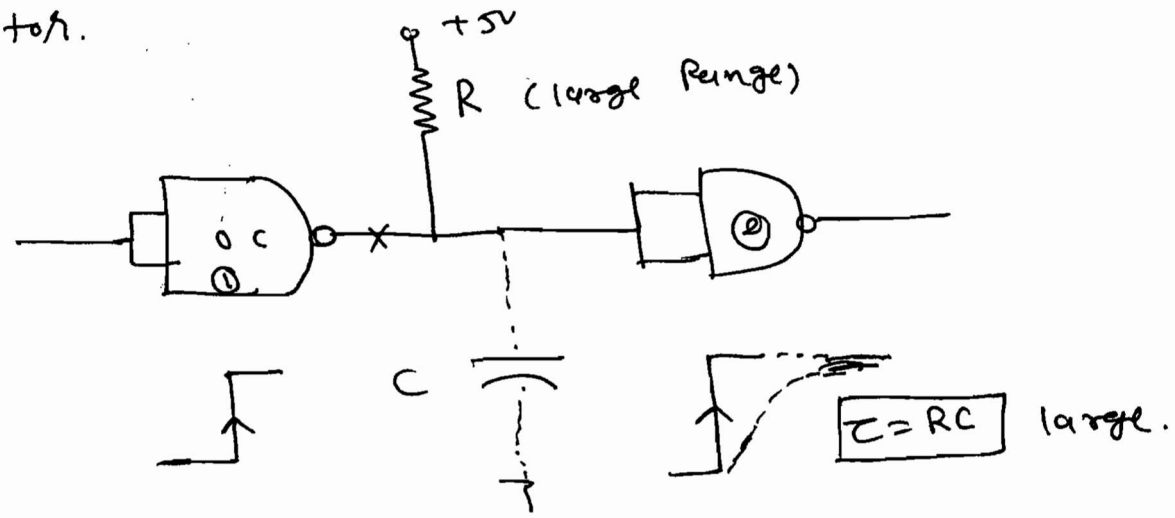
→ Wired - AND Logic. ✓





* Disadvantage:

→ In open collector TTL the stray capacitance at the i/p of the driven gate takes more time to change the voltage levels. because of high time constant $\tau = RC$, where R = pull up Resistor.



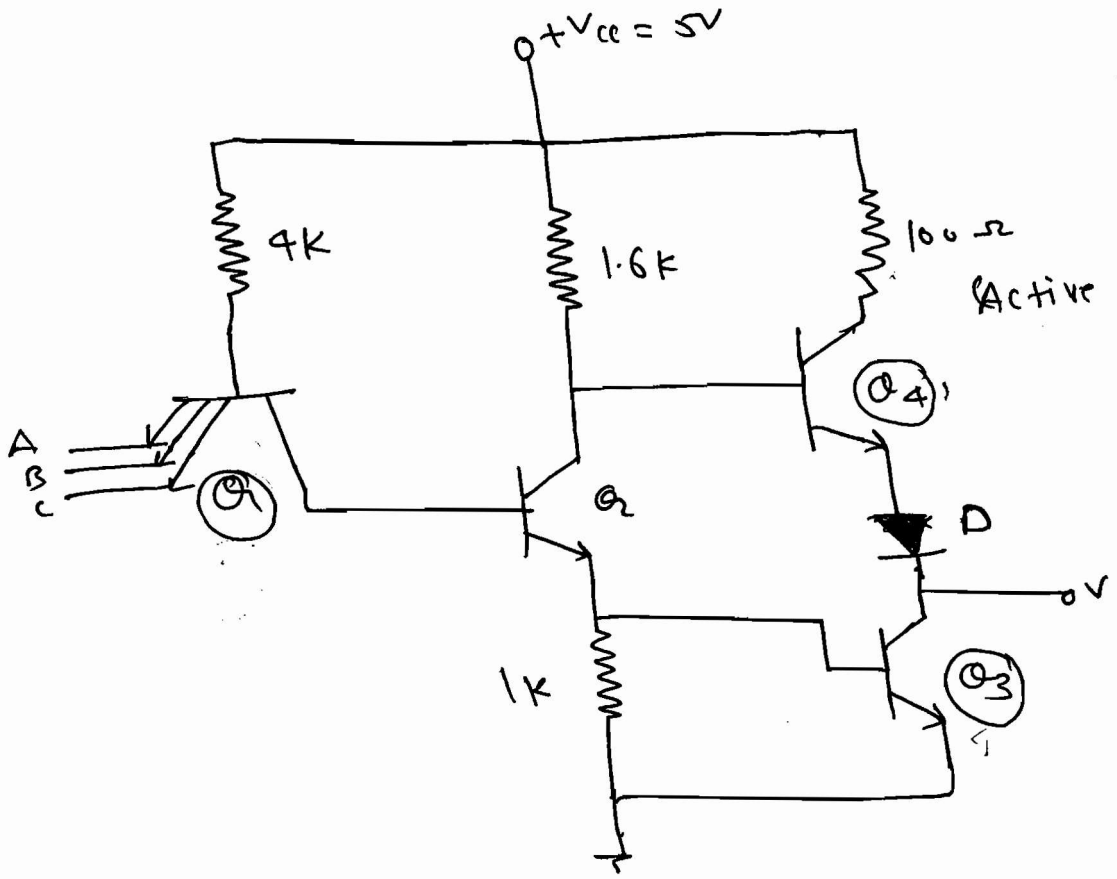
(2) Totempole: TTL;

→ To increase the speed of TTL the passive pull-up Resistor is Replace by active pull up which is a Emitter follower whose current gain is more and the o/p Resistance is less. Hence, the time constant is $\tau = R_o \cdot C$

where $\tau = R_o \cdot C$

where, R_o = output Resistance of emitter follower.

→



Q_4 → Emitter follower

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

→ Q_1 is in Forward Active mode
Q_2, Q_3 are OFF ⇒ $Y = +5V$
Q_4 ON

→ Q_1 is Reverse Active mode
Q_2, Q_3 are ON,
$Y = V_{CE,sat} = 0.2\,V$.
Q_4 OFF, D is OFF.

→ In TTL Logic floating inputs are considered

→ Q_2 is called phase spliter because it will maintain the exclusive condition betⁿ Q_3 & Q_4. that is one of them is on other one is off.

* Advantage:

→ High speed of operation because of less time constant $\tau = R_o \cdot C$

→ R_o = output resistance emitter follower.

* Disadvantge:

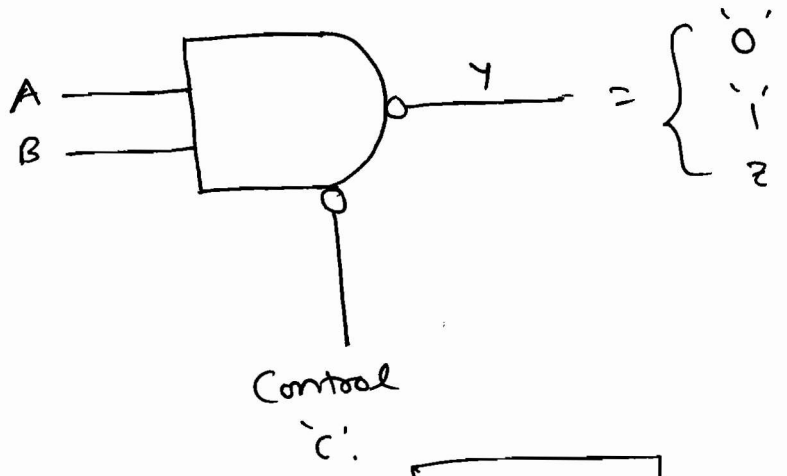
→ (i) As switch off time is more than switch on time, for a short period of time Both Q_3 & Q_4 will be in the on condition which results in large current drawn from the supply.

(ii) Wired And logic is not possible. with totempole & TTL.

⇒ To improve the speed of Totem pole TTL Q_4 and D are replaced by Darlington pair which has high current gain and

③ Tristate TTL:

→



If $C=0 \Rightarrow y = \overline{A \cdot B}$

If $C=1 \Rightarrow y = 'z'$. high Imp. state.

→ when $C=1$

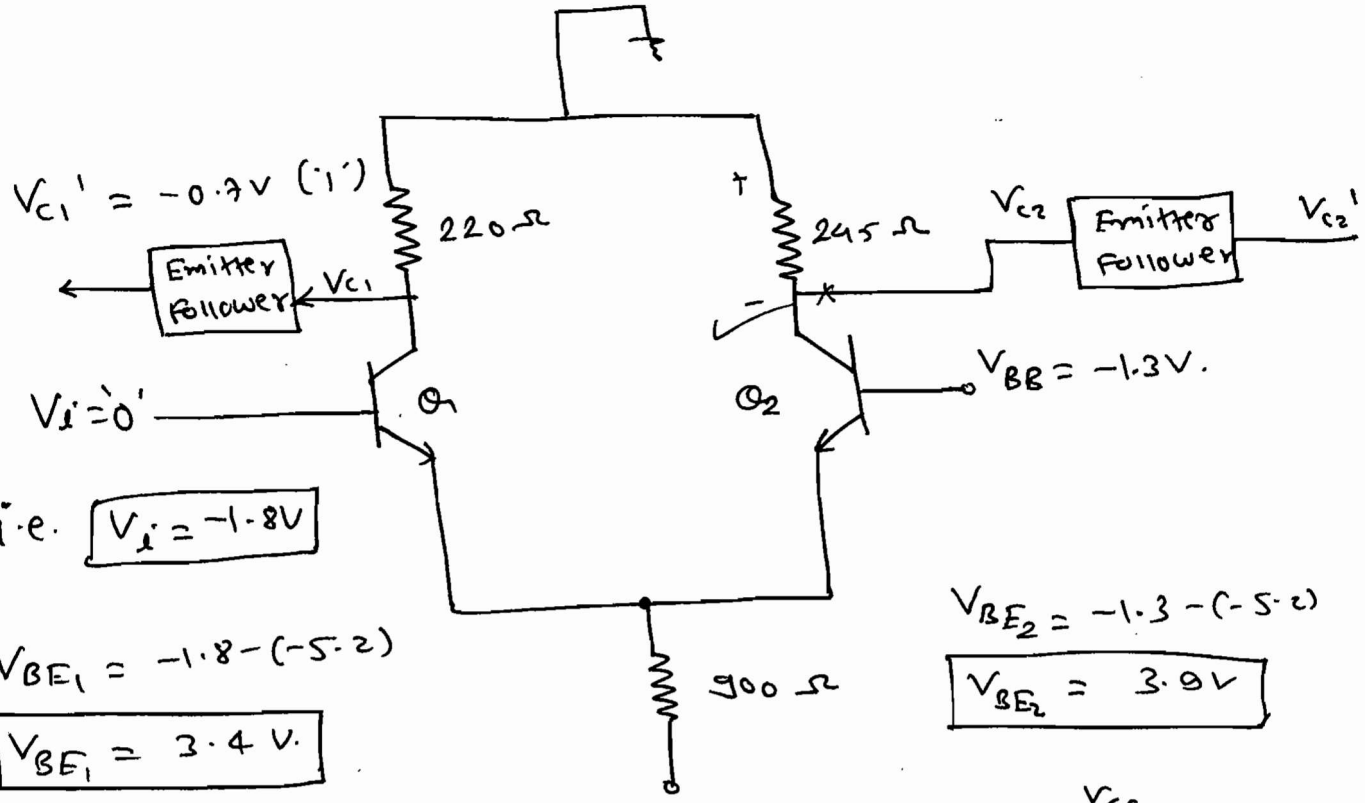
⇒ 'Both 'Q_3' and 'Q_4' will become OFF.

→ Tri-state TTL are used in Bus configurations of micro computer.

③ ECL (Emitter Coupled Logic).

(or) Non-Saturating Logic.

CML (Current mode logic).



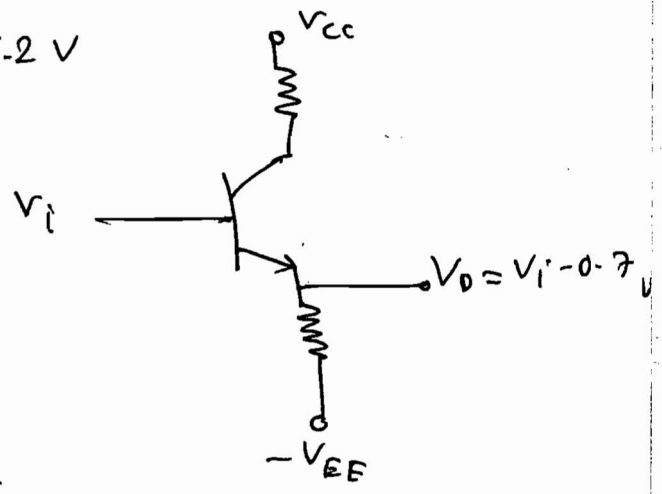
i.e. $\boxed{V_i = -1.8V}$

$V_{BE_1} = -1.8 - (-5.2)$

$\therefore \boxed{V_{BE_1} = 3.4V.}$

$V_{BE_2} = -1.3 - (-5.2)$

$\boxed{V_{BE_2} = 3.9V}$



$\therefore V_{C2} = -I_{C2} \cdot R_{C2}$.

$\therefore V_{C2} \approx -I_{E2} \cdot R_{C2}$.

$\therefore I_{E_2} = \dfrac{V_{BB} - V_{BE} - V_{EE}}{0.9}$.

$\therefore \boxed{V_{C2} = -0.9V}$

$\therefore = \dfrac{-1.3 - 0.7 - (-5.2)}{0.9}$

$\therefore I_{E_2} = \dfrac{3.2}{0.9} = 3.555\ mA$

V_i	Transistor	outputs.
'0' = -1.8V	Q_1 OFF Q_2 ON (Active Region)	$V_{C1} = 0$; $V_1' = -0.7$ ('1'). $V_{C2} = -0.9V$; $V_{C_2} = -0.9 - 0.7$

V_i	Transistor	outputs.
'1'	Q_2 OFF	$V_{c1} = -0.9V$; $V_{c1}' = -1.6V$ ('0').
$(-0.8V)$	Q ON (Active region)	$V_{c2} = 0$; $V_{c2}' = -0.7$ ('1').

(ii) If V_i = '1' = $-0.8V$.

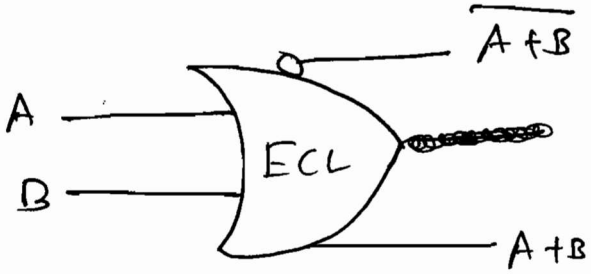
$V_{BE1} = 4.4V$;

$V_{BE2} = 3.9V$.

Hence Q_1 conducts, Q_2 is OFF.

→ From the above table we can observed that $\boxed{V_{c1}' = \overline{V_i} \quad \& \quad V_{c2}' = V_i}$

→



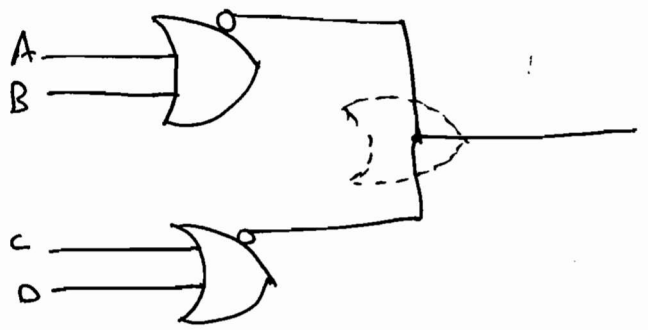
*Advantage:

→ High speed of operation because it is in non-saturating logic.

→ No current spikes.

④ Both NOR and OR gates are available.

⑤ Wired-OR logic is possible.



* Disadvantages:

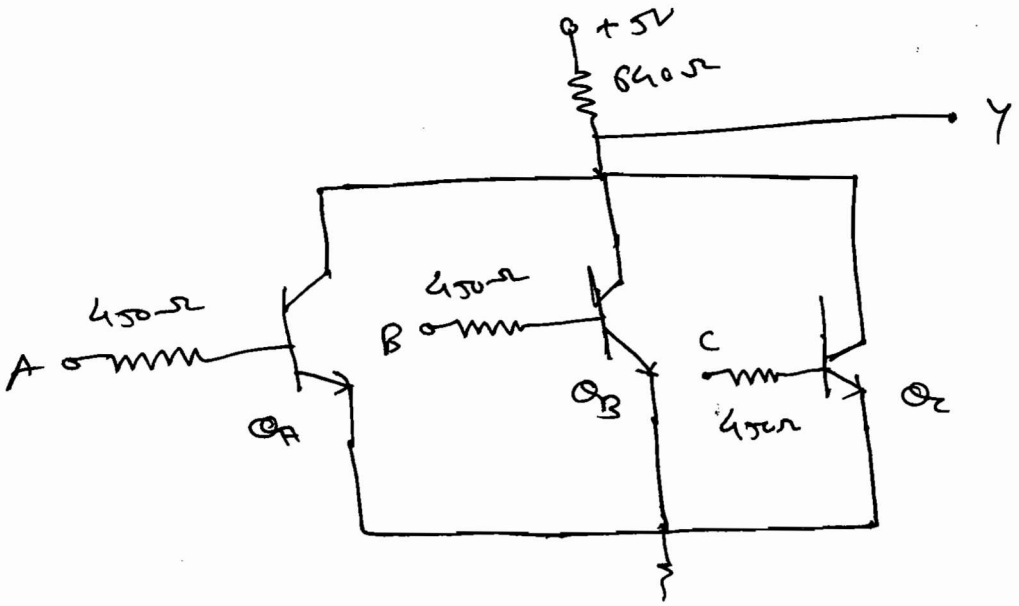
① High power dissipation because the Transistors operate in active region.

② the Noise margin of ECL gate is very less. [≈ 0.31 V].

Sr. No.	Parameters	Bipolar			MOSFET family	
		DTL	TTL	ECL	MOS	CMOS
1)	Fanout	8	10	25	20	>25
2)	Power Dissipation (mW)	8-12	12-22	40-55	0.2-1	0.01.
3)	Prop. Delay.	30	6-12	1-4	300	70x
4)	Noise Immunity	Good	very good	Fair	Good	very good.

→ BIMOS: Bipolar + MOSFET.

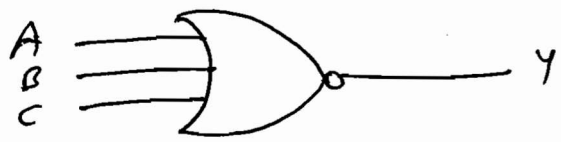
* RTL (Resistor Transistor Logic).



A	B	C	Y	
0	0	0	1	→ Q_A, Q_B, Q_C are OFF, $Y = +5V$
0	0	1	0	→ $Y = V_{CE,sat} = 0.2V$
0	1	0	0	
0	1	1	0	
1	0	0	0	
1	0	1	0	
1	1	0	0	
1	1	1	0	

$$Y = \overline{A+B+C}$$

So, it is NOR gate.



→ RTL has more resistors so it occupies more space than MOSFET families so it is outdated.

* I^2L : (Integrated Injection logic.

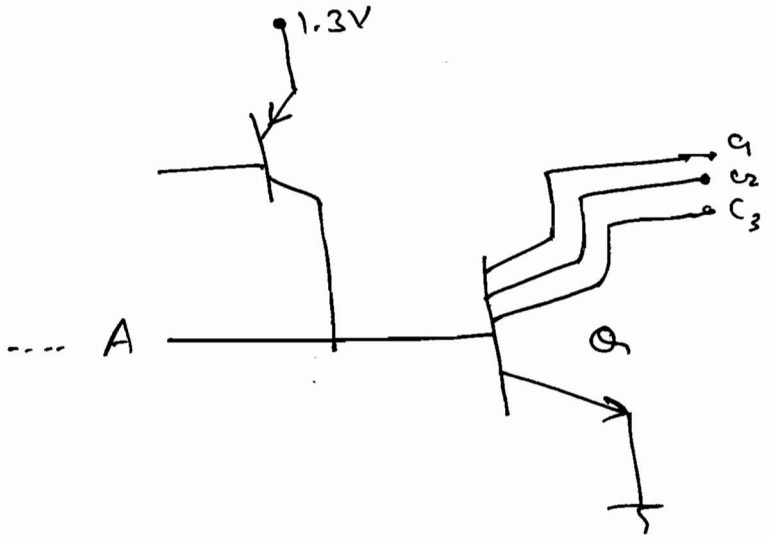
→ I^2L is obtained from RTL by making three changes:

(i) Base Resistors are omitted.

(ii) PNP transistors is used in place of collector Resistor.

(iii) Multicollector transistors are used.

→



* advantages:

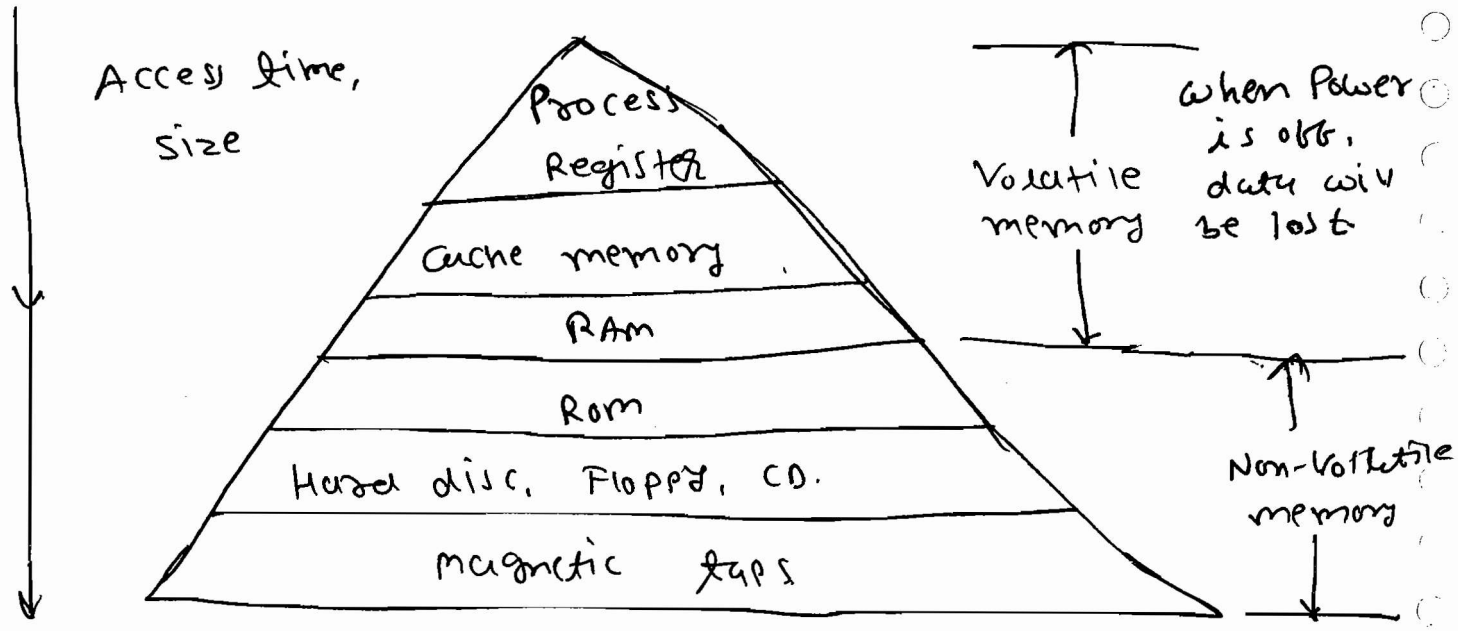
(i) High package density.

(ii) Low power and prop. delay product.

→ In I^2L the speed of operation can be control by choosing the voltage input of PNP transistor appropriately.

⇒ The High threshold logic (HTL) family is

☆ Semiconductors memories:



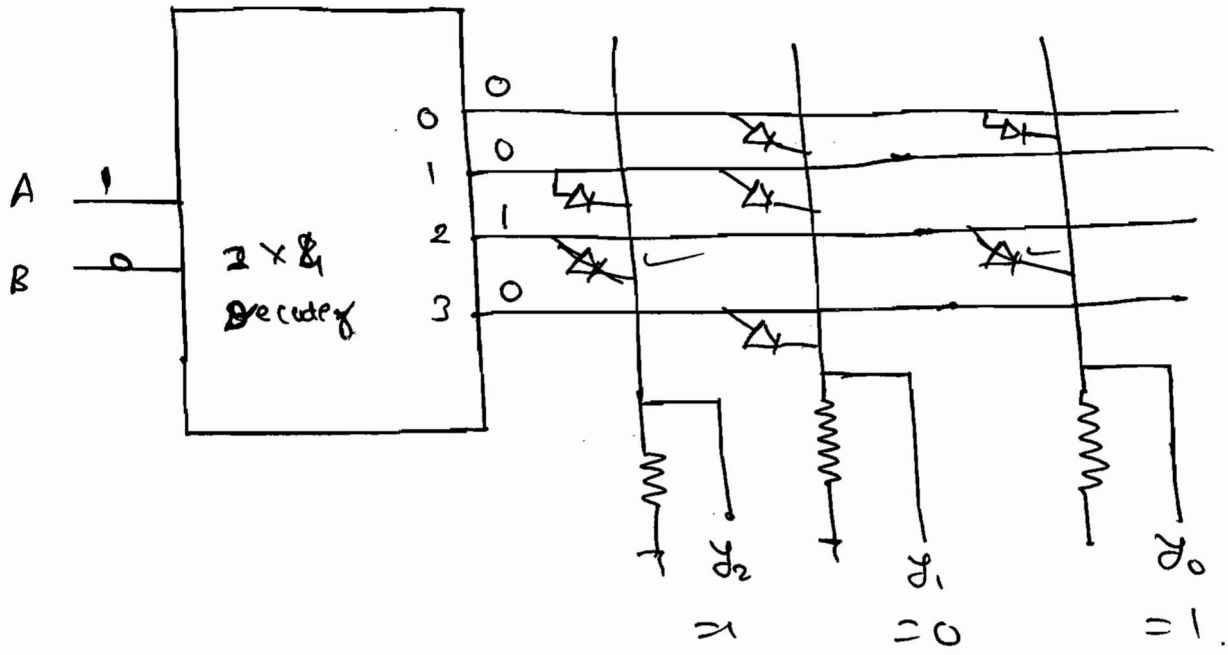
*

Semiconductor memory.

- ROM
  - PROM
  - EPROM
    - (Formerly)
  - EEPROM (?)
    - (FLOTOX)
  - Flash mem.
- RAM
  - SRAM
  - DRAM
- Sequential memory
  - SISO
  - SIPO
  - LIFO
  - FIFO
  - CCD
- CAM (content addressable memory)

* Rom using Diode matrix:

→



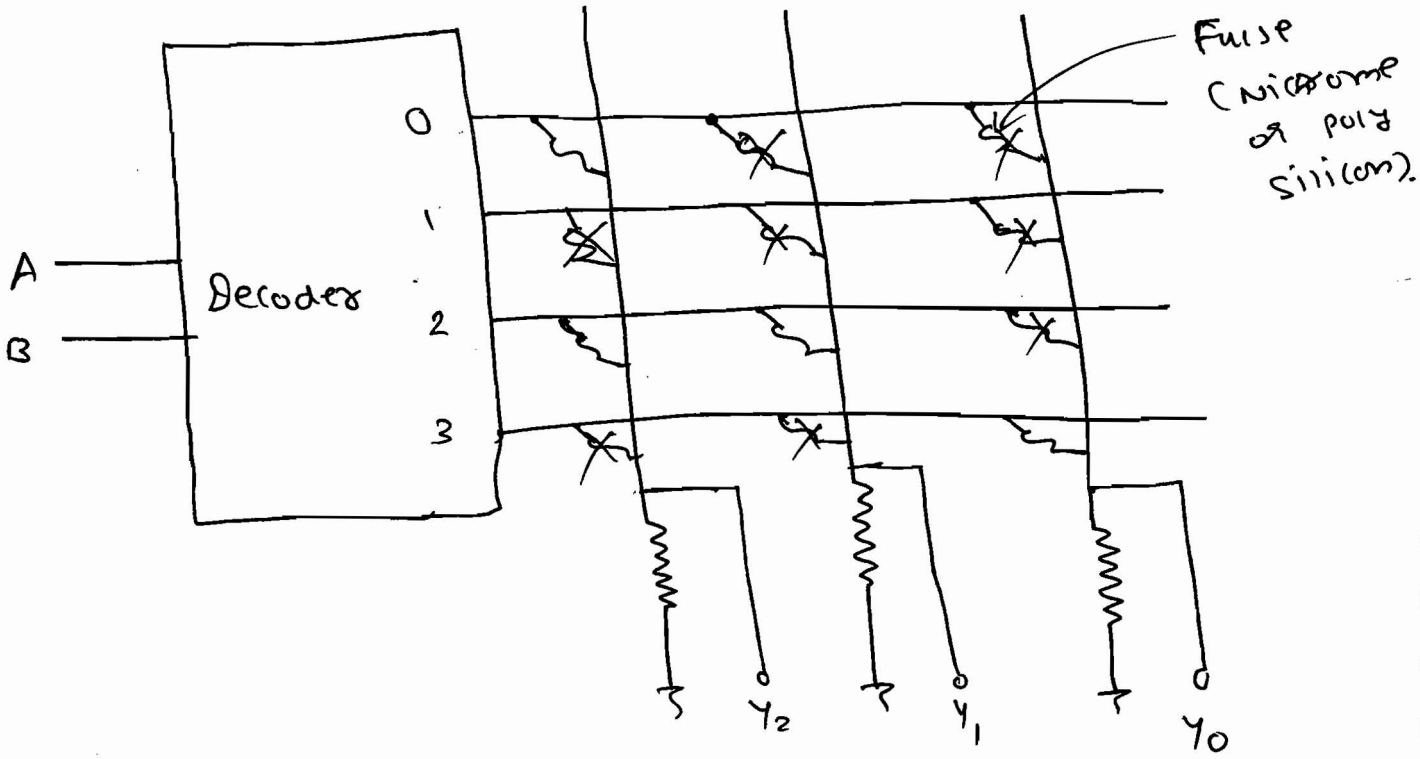
→ Rom as Combinational circuits.

$$\begin{cases} Y_2(A,B) = \Sigma m(1,2). \\ Y_1(A,B) = \Sigma m(0,1,3). \\ Y_2(A,B) = \Sigma m(0,2). \end{cases}$$

Rom size = $2^x \times y = 2^2 \times 3 = \boxed{12}$.

* PROM: (Programmable Rom) (OTP Rom)

(one time programmables.

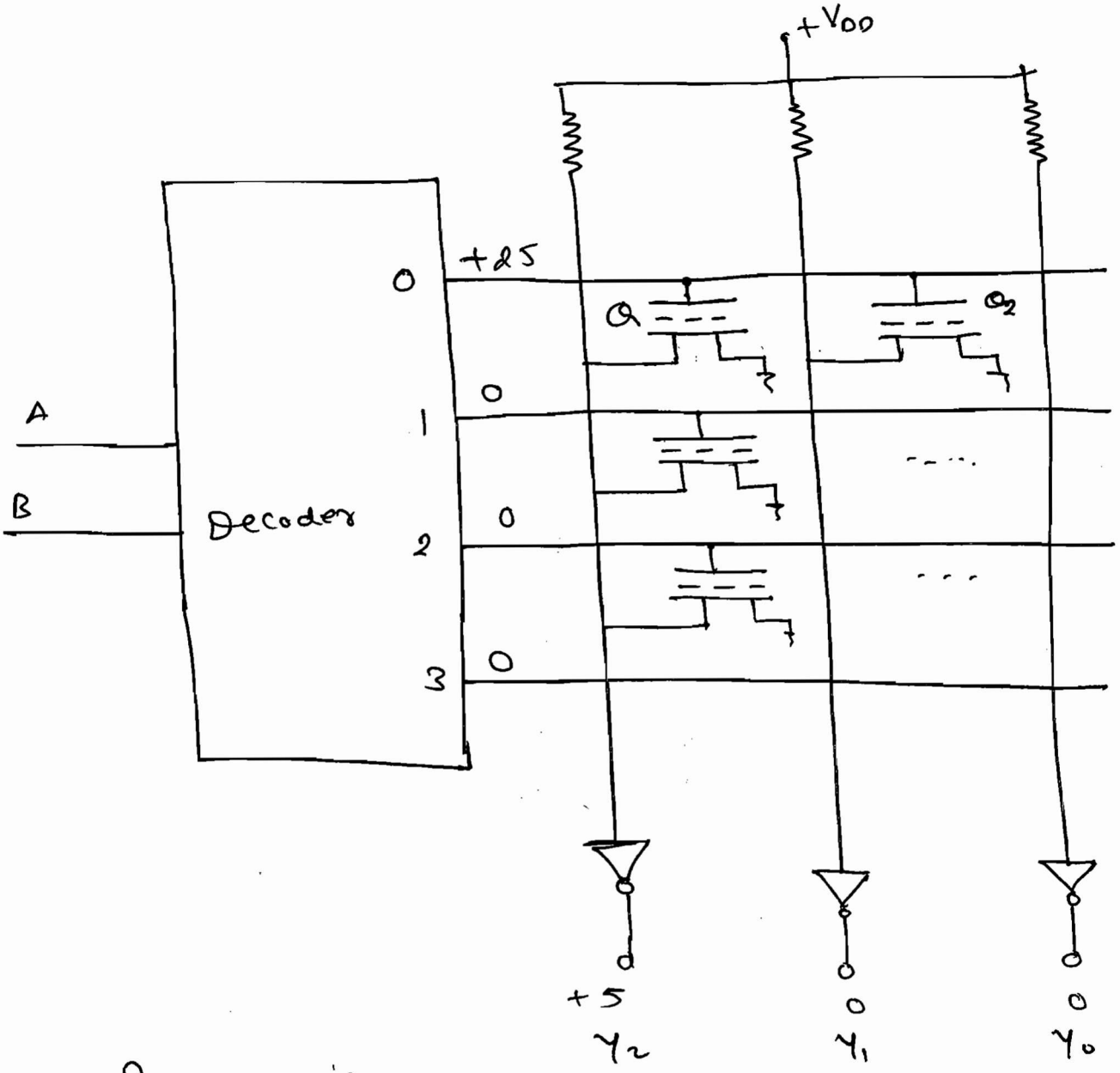


$Y_2(A,B) = \Sigma m(1,3)$.

$Y_1(A,B) = \Sigma m(0,1,3)$.

$Y_0(A,B) = \Sigma m(1,2,3)$

* Erasable PROM (EPROM).



(1) Programming:

- Q_1 → has Trapped electrons on floating gate
- Q_2 → has no trapped electrons on floating gate.

(2) Reading:

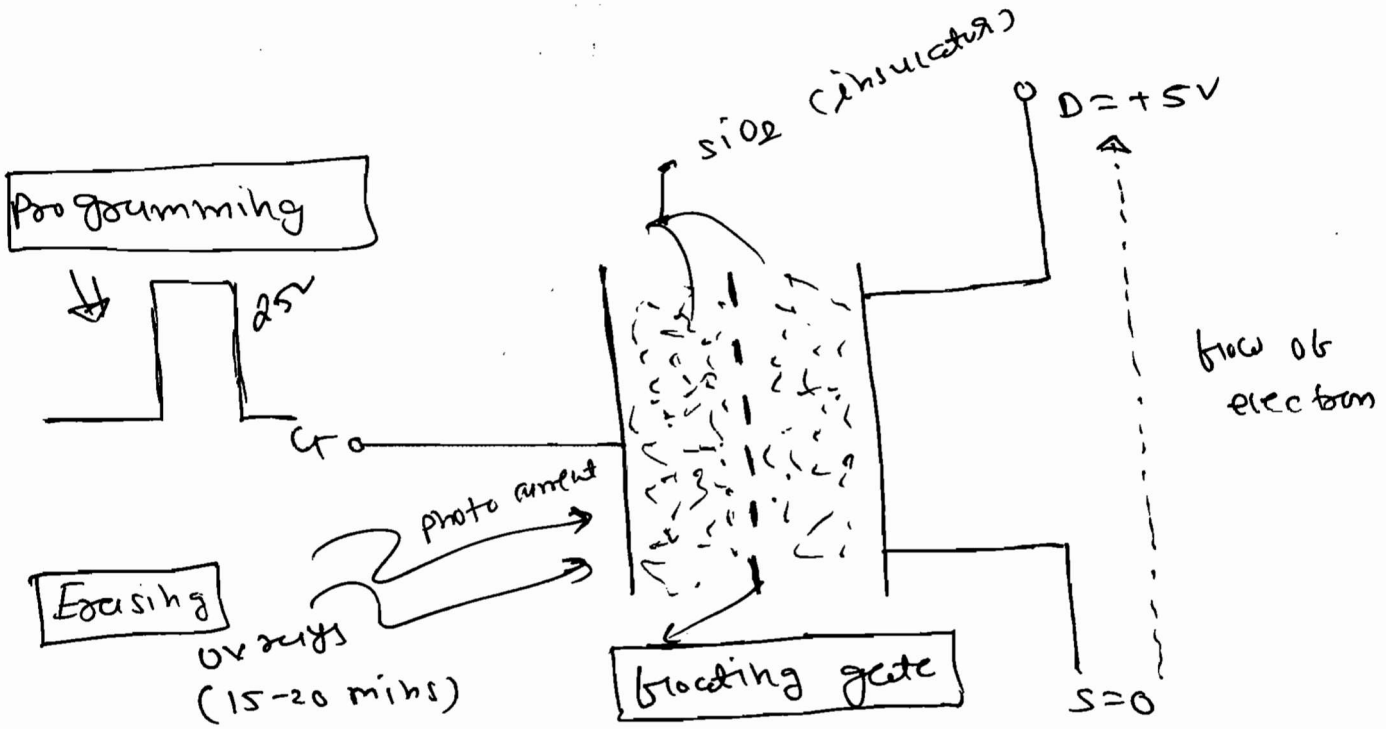
→ In a floating gate MOSFET if the electrons are trapped on the floating gate it results in Increasing in threshold voltage to 7 V.

→ Hence for 5 V Q_1 is going to be off and

$Y_2 = 0$ and $Y_1 = 1$.

(3) Erasing:

→ To erase we have to use UV rays bombard into it so that the electrons goes into their normal condition.



* Disadvantages:

(i) Insystem programming (ISP) not possible.

(ii) Erasing takes more time.

(iii) Partical erasing is not possible.

⇒ other name of it is

FAMOS

↓

Floating gate Avalanche injected MOSFET.

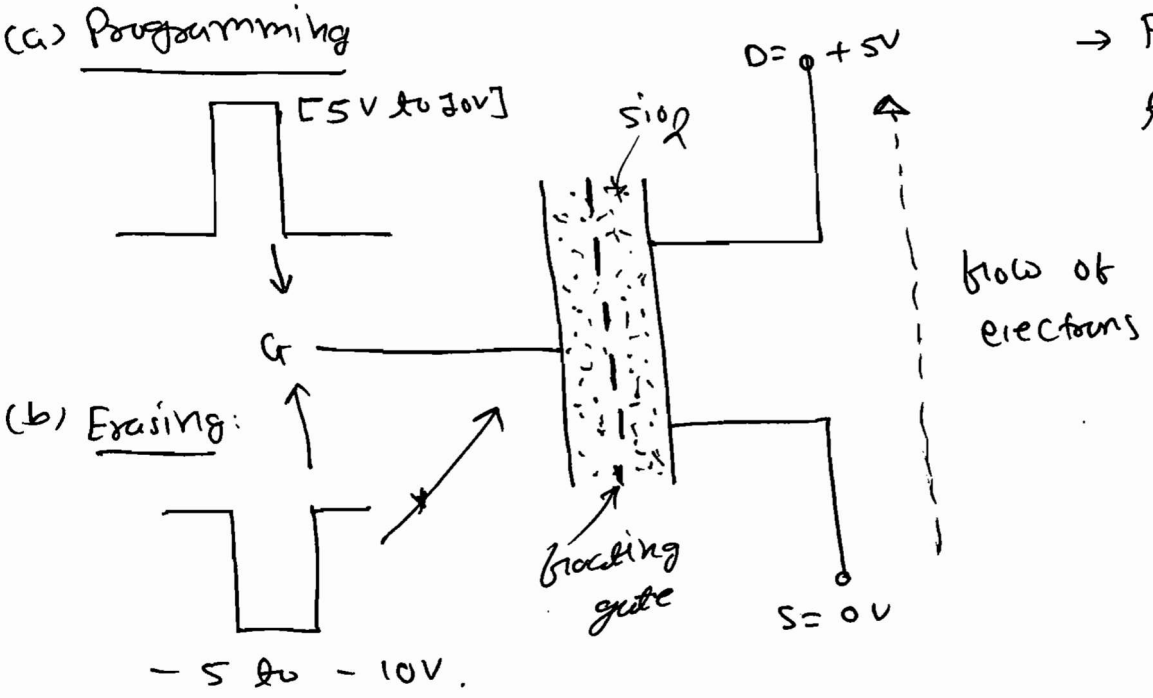
* E^2PROM (Electrically Erasable PROM).

→ In E^2PROM the thickness of silicon oxide layer in floating gate MOSFET is Reduced because of this, 5 to 10 V of programming pulse is sufficient to ~~dope~~ the electrons on the floating gate.

→ The MOSFET can be erased by reversing the polarity at the gate input.

FLOTAX

→ Floating gate tunneling oxide MOSFET.



* Advantages:

(1) Partial erasing is possible.

(2) Isp (In system programming) is possible.

(3) Erassing takes very less time.

* Disadvantages:

requires 2 MOSFETS one floating gate MOSFET and another one is ordinary MOSFET.

(2) High cost per bit.

* Flash Memory:

→ Advantages of Flash memory.

① High Package density

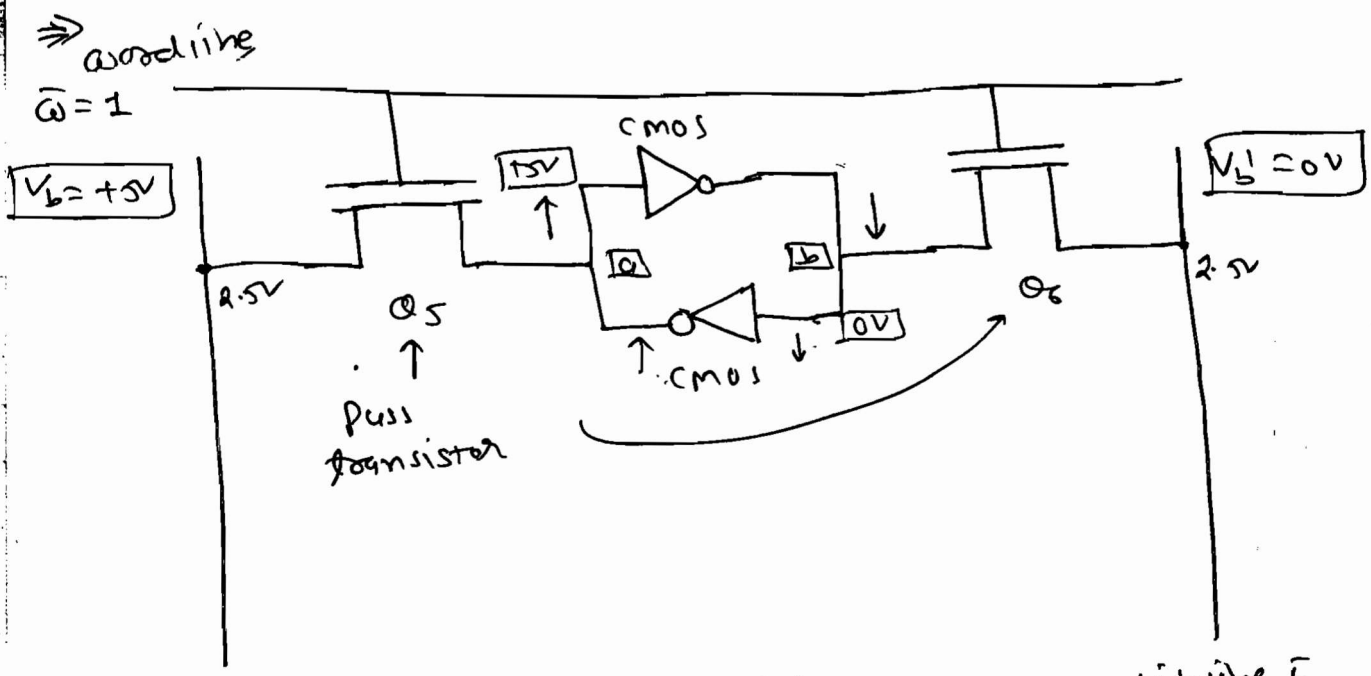
② Partial Erasing

③ Isp is possible.

④ Low cost.

⑤ More no. of Read/write cyles.

(a) SRAM (1bit mem. cell). (Static RAM)



FF (or) Latch.

→ To store Logic '1' in SRAM cell.

① bit lines are precharged to 2.5V

② Choose W=1 ; V_b = +5V ; V_b' = 0V.

③ 'V_a' rises to +5V ; V_b drops to 0V.

Thus logic '1' is store in SRAM cell.

→ To Read SRAM cell.

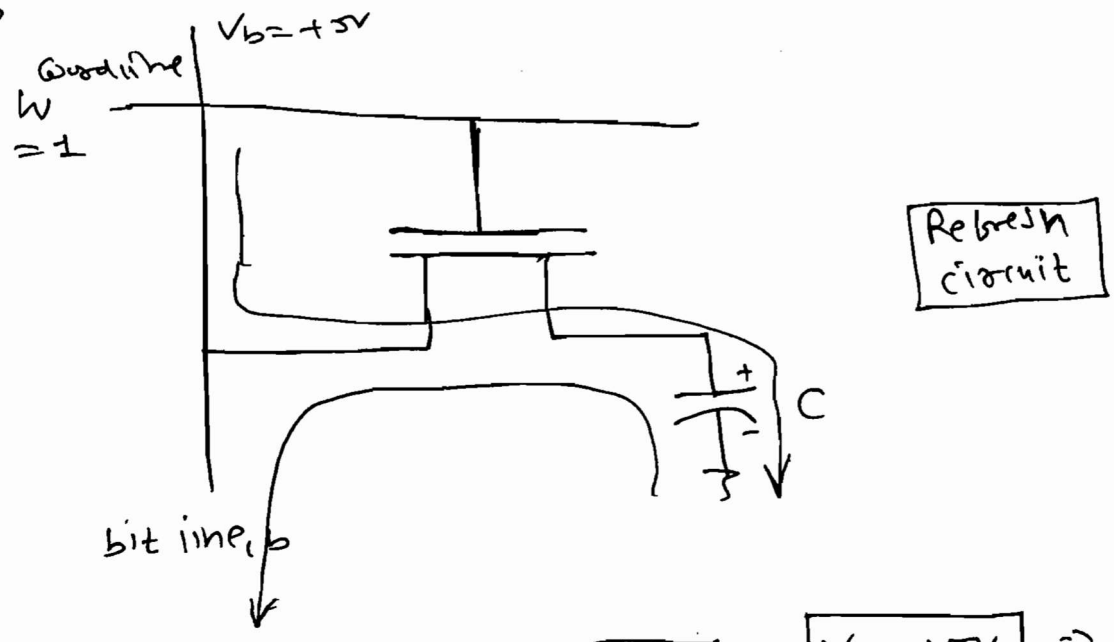
① Choose W=1.

② Q_5, Q_6 MOSFET are ON.

③ Hence, b='1', $\bar{b}$=0.

(2) DRAM: (Dynamic RAM).

⇒



Refresh circuit

a) To write: Choose W=1 ; V_b = +5V ⇒ Logic '1' is stored.

b) To Read: Choose W=1

⇒ If bit line = +5V ⇒ Logic '1'.

	SRAM	DRAM
Advantages:	① Speed is very high. (cache memory). ② Less hardware. Complecity.	① High package density. ② Low power Consumption. ③ Less cost
Disadvantages:	① Low package density ② High power Consmption ③ High cost	① Speed is less. (primary memory) ② more Hardware complexity. (because the voltage across Capacitor has to be refreshed at regular interval of time 2-4ms by using Refreshing CKT.