Number of Questions: 35 **Section Marks: 90**

Directions for questions 1 to 35: Select the correct alternative from the given choices.

1. For a certain transistor, I_B = 25μA, I_C = 2.5mA and β = 75, then the value of I_{CBO} is ______.

(A) 0.625 mA (B) 0.82 mA
(C) 8.22 μA (D) 7.5 μA

2. Two pure specimen of a semiconductor materials are taken, one is doped with 10^{15} cm^{-3} number of donors and the other is doped with 10^{18} cm^{-3} number of acceptors. The minority carrier density in the second specimen is 10^{8} cm^{-3}. What is the minority carrier density in the other specimen?

(A) 10^{12} cm^{-3} (B) 10^{14} cm^{-3}
(C) 10^{11} cm^{-3} (D) 10^{25} cm^{-3}

3. The intrinsic carrier concentration of *Si* sample at 300°K is 2.25 ×10^{16} m^{-3}. If after doping the number of majority carriers is 4.5 × 10^{19} m^{-3}, then find the minority carrier density.

(A) 1.125 × 10^{16} cm^{-3} (B) 11.25 × 10^{14} m^{-3}
(C) 2.25 ×10^{13} m^{-3} (D) 1.125 ×10^{13} m^{-3}

4. For a npn transistor I_E = 3mA, α = 0.97 and I_{CEO} = 1.5 mA, then find I_C value.

(A) 2.75 mA (B) 2.955 mA
(C) 2.9 mA (D) 2.25 mA

5. If the value of collector current I_C decreases, then the value of V_{CE} is

(A) decreases (B) increases
(C) remains the same (D) None of the above

6. For a voltage controlled current source, the Input impedance and output impedances are respectively

(A) Low, high (B) high, high
(C) high, low (D) low, low

7. Which of the following conditions must be satisfied to avoid thermal runaway?

(1) $\dfrac{\partial P_C}{\partial T_j} < \dfrac{1}{\theta_{jA}}$ (2) $2V_{CE} < V_{CC}$

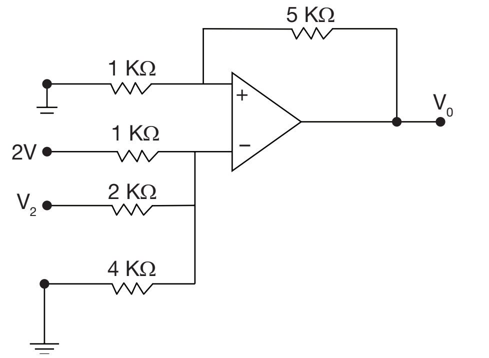
(3) $V_{CE} \geq 1/2V_{CC}$ (4) $\dfrac{\partial P_C}{\partial T_j} > \dfrac{1}{\theta_{jA}}$

(A) 1 and 2 only (B) 3 only
(C) 1 and 3 only (D) 2 and 4 only

8. In a JFET amplifier, the source resistance R_s is un bypassed. Find the voltage gain of the amplifier. Given g_m = 4ms, R_D = 2kΩ and R_s = 500Ω

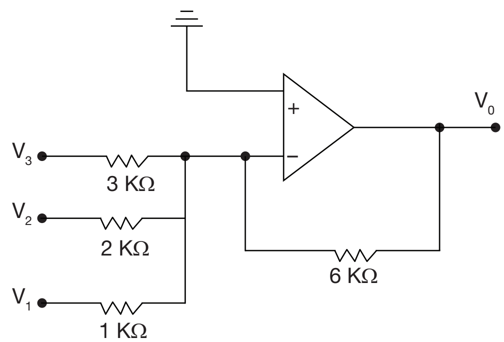
(A) 2.66 (B) 1.53
(C) 2.25 (D) 1.8

9. If the output V_0 = 12 V, then the input voltage V_2 is ______



(A) 3 V (B) 2 V
(C) –3 V (D) 6 V

10. If V_1 = 2V, V_2 = –3V and V_3 = 1V, then the output voltage V_0 is

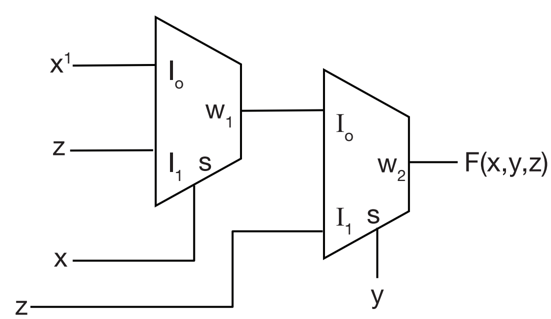


(A) 0 V (B) –10 V
(C) –5 V (D) 2.5 V

11. How many number of 2 input NAND gates are required to impalement $f(A, B, C) = \Sigma m$ (1, 3, 4, 5, 6, 7, 9, 11, 12, 13 14,15)

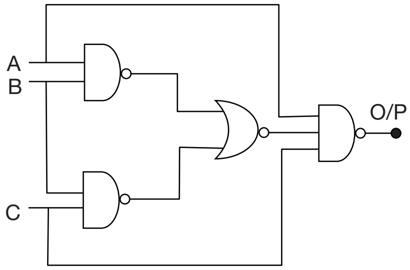
(A) 4 (B) 3
(C) 2 (D) 1

12. The output of the following Multiplexer circuit is



(A) $x^1 + yz$ (B) $x^1 y + z$
(C) $(x^1 + y)z$ (D) $x^1 y^1 + yz + xy^1 z$

13. The output of the following circuit is



(A) $\overline{AB}+\overline{BC}$ (B) $\overline{AB}+\overline{BC}+\overline{AC}$

(C) $\overline{A}+\overline{B}+\overline{C}$ (D) $\overline{AB+BC}$

14. Match the following

List I (Numbers in Decimal)

List II (equivalents in signed 2's complement representation)

	List –I		List – II
P.	– 43	1.	01100000
Q.	– 78	2.	00110110
R.	+ 54	3.	111010101
S.	+ 96	4.	10110010

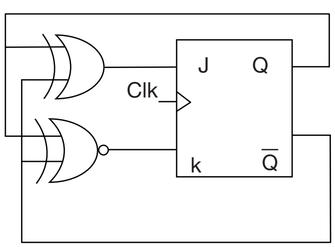
(A) $P-3, Q-4, R-1, S-2$

(B) $P-4, Q-3, R-1, S-2$

(C) $P-3, Q-4, R-2, S-1$

(D) $P-4, Q-3, R-1, S-2$

15. The states of Q, $\overline{Q}$ after clock pulse are



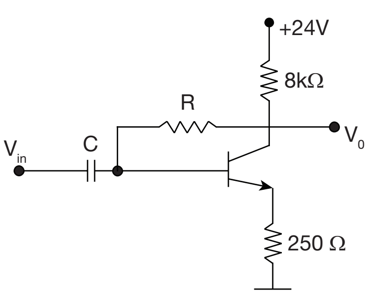
(A) 0, 1

(B) 1, 0

(C) 1, 1

(D) Cannot be determined without initial states

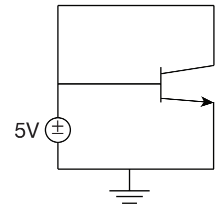
16. If the transistor having $V_{CE} = 4.5$ V, $V_{BE} = 0.7$ V and $\beta = 50$, then the value of R is ______.



(A) 79.51 KΩ (B) 82 KΩ

(C) 87.52 KΩ (D) 63.75 KΩ

17. In the following circuit transistor is in



(A) cut-off region (B) Active region

(C) saturation (D) inverse active

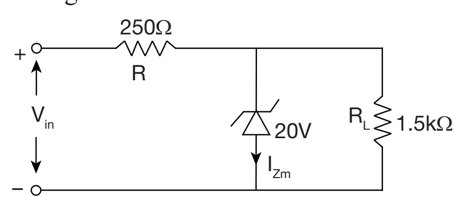
18. Group-I four different semiconductor devices. Match each device in Group-I with its characteristic property in Group-II.

Group – I	Group – II
w. Photo diode	1. Early effect
x. MOS capacitor	2. Coherent radiation
y. LASER	3. Flat band voltage
z. BJT	4. Dark current

(A) w–4, x–2, y–3, z–1 (B) w–2, x–3, y–2, z–4

(C) w–1, x–2, y–4, z–3 (D) w–4, x–3, y–2, z–1

19. Determine the range of values of V_{in} that will works as the zener regulator.



(consider $I_{zm} = 50$ mA)

(A) $25\text{ V} \le V_{in} \le 35\text{ V}$

(B) $23.33\text{ V} < V_{in} < 30\text{ V}$

(C) $23.33\text{ V} \le V_{in} \le 35.83\text{ V}$

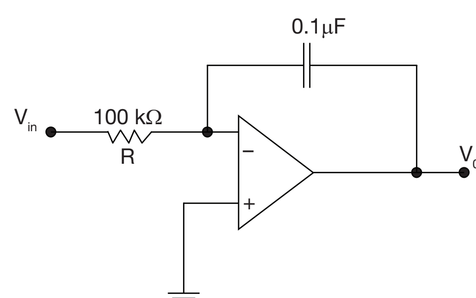
(D) $20\text{ V} \le V_{in} \le 35\text{ V}$

20. The drain of an n-channel MOSFET is shorted to the gate so that $V_{DS} = V_{GS}$. The threshold voltage (V_{th}) of MOSFET is $1.25V$ of the drain current I_D is 1.5mA for $V_{GS} = 3$V, then for $V_{GS} = 1.5$V, I_D is

(A) 2.37 mA (B) 3.45μA

(C) 4.23 mA (D) 30.61μA

21.

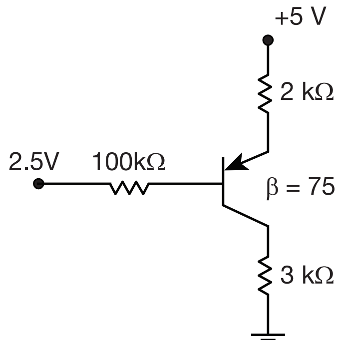


If $V_{in} = 5 + 1.5t^2$ Volts, then the output voltage of the given circuit at $t = 0.5$sec is

(A) –1.5 V (B) –3.84 V
(C) –5.375 V (D) –2.5625 V

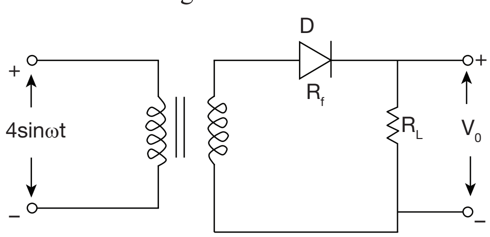
22. The unity gain bandwidth of a n – channel MOSFET amplifier having V_{Tn} = 2V, and biased at V_{GS} = 4 V. The high frequency n – channel MOSFET parameters are K_n = 0.5μA/V², C_{gd} = 0.05pF, C_{gs} = 0.2pF.
(A) 2.546 kHz (B) 2.546 MHz
(C) 1.273 kHz (D) 1.273 MHz

23. Find the region of operation of the transistor



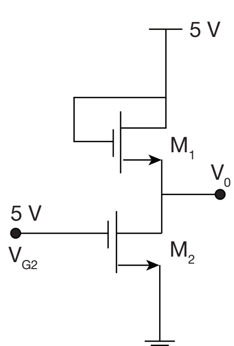
(A) Cut – off (B) Saturation
(C) Active (D) Inverse active

24. Consider the circuit given below where R_f = 250Ω, R_L = 3 kΩ. Then the average and RMS currents would be



(A) I_{avg} = 1.23 mA, I_{rms} = 0.615 mA
(B) I_{avg} = 0.87 mA, I_{rms} = 0.39 mA
(C) I_{avg} = 0.39 mA, I_{rms} = 0.87 mA
(D) I_{avg} = 0.39 mA, I_{rms} = 0.615 mA

25. The transistors in the circuit of figure have parameters V_{TN}= 0.3 V, K_n = 50 μA/V² and λ = 0. The width – to – length ratio of M_2 is $\left(\frac{W}{L}\right)_1$ = 2.If V_0 = 0.5V, when V_{in} = 5 V. Then $\left(\frac{W}{L}\right)_2$ is



(A) 15 (B) 16.8
(C) 2.38 (D) 1.6

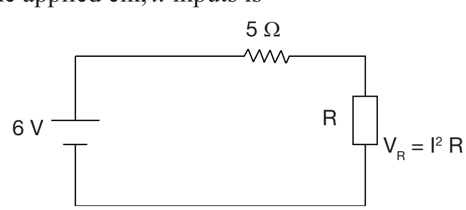
26. An 8 bit Digital to Analog converter has an output current of 5.8 mA, for the input 10010001, then the output current for input 11110100 is (in mA)
(A) 9.25 (B) 9.76
(C) 8.43 (D) 8.23

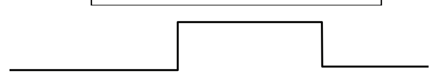
27. At the end of this program, the contents of Accumulator are?
MVI A, 64 H
MOV B, A
STC
CMC
RAL
X RA B
(A) C8H (B) 2CH
(C) 00H (D) ACH

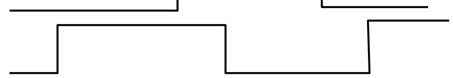
28. What is the operation performed in the following program.
LXI H, 4123 H
MOV A, M
CMA
MOV M, A
XRA A
(A) Contents of Register M are moved to Accumulator
(B) H = 23H, L = 41H, A = Un known
(C) contents of Memory location 4123 H are complemented. and stored in the same location
(D) contents of Memory location 4123 H are XORed with Accumulator and retained in Accumulator

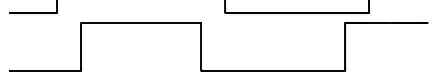
29. Convert the following number to base 9.
$(1101222.201121)_3$
(A) 1358.647 (B) 4172.647
(C) 4178.153 (D) 1358.153

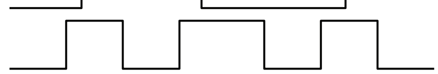
30. The initial value of Q = 0, then the output Q waveform for the applied clk, x inputs is



(A) 

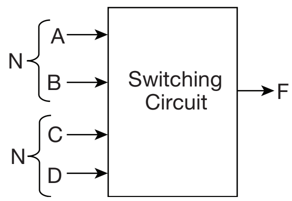
(B) 

(C) 

(D) 

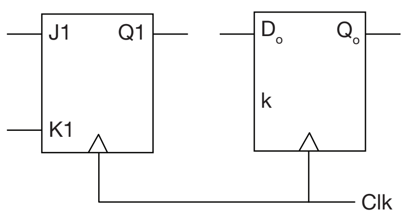
31. A switching circuit has four inputs as shown, A and B represent the first and second bits of a binary number $N1$, C and D represent the first and second bits of a binary number N_2,

The output is 1 only, if the product $N_1 \times N_2$ is less than or equal to 2.
The POS form of $F(A, B, C, D)$ is



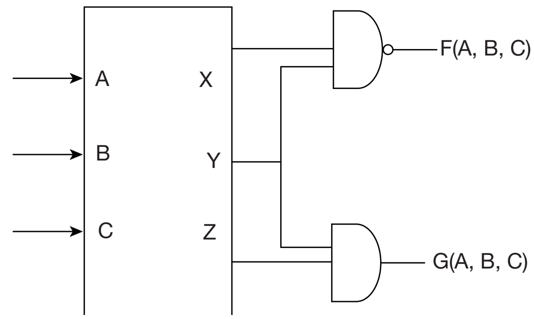
(A) $\overline{AB} + \overline{CD} + \overline{AC} + \overline{AD} + \overline{BC}$
(B) $(A + C)(A + B + D)(B + C + D)$
(C) $\left(\overline{A} + \overline{D}\right)\left(\overline{A} + \overline{B} + \overline{D}\right)\left(\overline{B} + C + \overline{D}\right)$
(D) $\left(\overline{A} + \overline{C}\right)\left(\overline{A} + \overline{B} + \overline{D}\right)\left(\overline{B} + \overline{C} + \overline{D}\right)$

32. The synchronous counter which follows (Q_1Q_0) 00 → 10 → 11 → 01 → 00 by using *JK* flip flop and *D* flip flop, has inputs as



(A) $J_1 = \overline{Q}_1, K_1 = Q_O, D_O = Q_O$
(B) $J_1 = Q_1, K_1 = \overline{Q}_1, D_O = Q_O$
(C) $J_1 = \overline{Q}_0, K_1 = Q_O, D_O = Q_1$
(D) $J_1 = Q_0, K_1 = \overline{Q}_O, D_O = Q_1$

33. A combinational circuit has 3 inputs *A*, *B*, *C* and 3 outputs *x*, *y*, *z*. and the functions *F* (*A*, *B*, *C*) and *G* (*A*, *B*, *C*)are generated from the combinational logic circuit as shown here with NAND, AND gates. Find the least possible minterm expression for *Y* (*A*, *B*, *C*).
$F(A, B, C) = \Sigma m\,(1, 3, 4, 5, 7)$
$G(A, B, C) = \Sigma m\,(4, 6)$
$Y(A, B, C) = \Sigma m\,(?)$



(A) Σm (0, 2, 3, 6, 7)
(B) Σm (1, 3, 4, 5, 7)
(C) Σm (0, 2, 4, 6,)
(D) Σm (0, 2, 4)

34. The minimum SOP form of

$$f(P, Q, R) = \left(\overline{P} + R + \overline{Q}\right)\left(\overline{P} + \overline{R} + Q\right)\left(\overline{P} + R + Q\right)$$

(A) $\overline{P} + QR$
(B) $\overline{P} + Q$
(C) $\overline{P}\overline{Q} + R$
(D) P

35. 6000: LXI H, 4C83H
6003: MOV A, L
6004: ADD H
6005: DAA
6006: MOV H, A
6007: PCHL
At the end of this program, from which address next instruction will be fetched?
(A) 9038H
(B) 8438H
(C) 8A38H
(D) 6008H

Answer Keys

1. C	**2.** C	**3.** D	**4.** B	**5.** B	**6.** B	**7.** A	**8.** A	**9.** A	**10.** C
11. B	**12.** B	**13.** C	**14.** C	**15.** B	**16.** A	**17.** B	**18.** D	**19.** C	**20.** D
21. D	**22.** D	**23.** C	**24.** D	**25.** B	**26.** B	**27.** D	**28.** C	**29.** A	**30.** A
31. D	**32.** C	**33.** C	**34.** A	**35.** C					

Hints and Explanations

1. $I_C = \beta . I_B + I_{CEO}$
$2.5 \times 10^{-3} - 75 \times 25 \times 10^{-6} = I_{CEO}$
$I_{CEO} = 0.625$ mA
$I_{CEO} = (1 + \beta).I_{CBO}$
$I_{CBO} = 8.22$ μA

Choice (C)

2. $n.p = n_i^2$

$n_1 p_1 = n_2 . p_2$
from the given data
$n_1 = 10^{15}$ cm^{-3}
$p_1 = ?$
$n_2 = 10^8$ cm^{-3}
$p_2 = 10^{18}$ cm^{-3}

$$p_1 = \frac{10^8 \times 10^{18}}{10^{15}} = 10^{11}\,\text{cm}^{-3}$$

Choice (C)

3. $n.p = n_i^2$

$$\therefore \text{ minority carrier density} = \frac{n_i^2}{\text{majority carrier density}}$$

$$= \frac{\left(2.25\times10^{16}\right)^2}{4.5\times10^{19}}$$

$= 1.125 \times 10^{13}$ per m^3 Choice (D)

4. $I_C = \alpha.I_E + I_{CBO}$

$$I_{CEO} = \frac{1}{1-\infty}.I_{CBO}$$

$I_{CBO} = (1 - \alpha).I_{CEO} = 45\ \mu A$
$I_C = 0.97 \times 3 \times 10^{-3} + 0.045 \times 10^{-3}$
$= 2.955$ mA Choice (B)

5. We know $V_{CC} = I_C R_C + V_{CE} + I_E R_E$
Let $I_C \approx I_E$
$\therefore\ V_{CE} = V_{CC} - I_C(R_C + R_E)$
$\therefore\ V_{CE}\uparrow \Rightarrow I_C\downarrow$ Choice (B)

6. Ideal VCCS
$R_{in} = \infty$
$R_0 = \infty$
But practical case
R_{in} & R_0 are very large values.
Choice (B)

7. Choice (A)

8. $A_v = \dfrac{g_m.R_D}{1+g_m+R_S}$; for R_s un by passed $[R_s \neq 0]$

$$A_v = \frac{4\times10^{-3}\times2\times10^3}{1+4\times10^{-3}\times0.5\times10^3} = \frac{8}{3} = 2.66$$

Choice (A)

9. Applying virtual GND concept
Let $V+ = V- = V_a$

$$\therefore\ V_0 = \left[1+\frac{R_f}{R_1}\right].V_a$$

$V_0 = 6V_a$
Apply nodal analysis at node $V+$ or V_a

$$\frac{V_a-2}{1}+\frac{V_a-V_2}{2}+\frac{V_a}{4}=0$$

$4[V_a] - 8 + 2V_a - 2V_2 + V_a = 0$
$7V_a = 8 + 2V_2$

$$V_a = \frac{V_0}{6} = 2$$

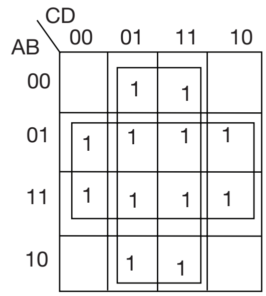
$14 - 8 = 2V_2$
$V_2 = 3$ Volts Choice (A)

10. The given circuit represents a inverting summing amplifier

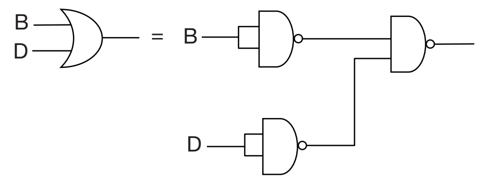
$$\therefore\ V_0 = \frac{-R_f}{R_1}.V_1 - \frac{R_f}{R_2}.V_2 - \frac{R_f}{R_3}.V_3$$

$\therefore\ V_0 = -\{6 \times 2 + 3 \times (-3) + 2 \times 1\}$
$= -\{12 - 9 + 2\} = -5$ Volts. Choice (C)

11. $F(A, B, C, D) = \Sigma m\ (1, 3, 4, 5, 6, 7, 9, 11, 12, 13, 14, 15)$



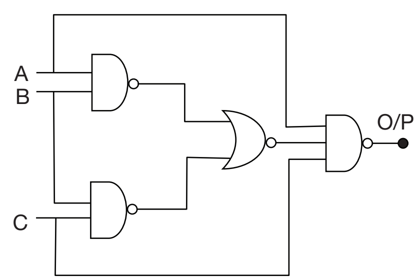
$F = B + D$



So 3, 2 input NAND gates are required to implement
$F(A, B, C, D) = B + D$ Choice (B)

12. The first multiplexer output is $w_1 = I_o\ \overline{S} + I_1 S$
$= x^1.\ x^1 + z.x = x^1 + zx = x^1 + z$
The output of second multiplexer is
$w_2 = I_1 S + I_o\ \overline{S}$
$= (x^1 + z)y + z.y^1$
$= x^1 y + yz + y^1 z$
$= x^1\ y + (y + y^1)z = x^1\ y + z$ Choice (B)

13. In the circuit NAND – NOR structure can be redrawn as AND – AND Structure



$\overline{A.ABC.C} = \overline{ABC} = \overline{A} + \overline{B} + \overline{C}$ Choice (C)

14. Positive numbers will be represented in their original binary magnitude but sign bit will be zero (0) to make it as positive number.
Negative Numbers are represented as 2'*s* complement of their positive numbers representation in 2'*s* complement signed number.
+ 43 = 000101011
– 43 = 111010101 (By taking 2'*s* complement)
+ 78 = 01001110
– 78 = 10110010 (By taking 2'*s* complement)
+ 54 = 00110110
+ 96 = 01100000 Choice (C)

15. $J = Q_n \oplus \overline{Q_n}\ (EX-OR\ of\ Q, \overline{Q}) = 1$

$K = Q_n \odot \overline{Q_n} (EX-NOR\ of\ Q, \overline{Q}) = 0$

When $J = 1$, $K = 0$, next clk pulse will give $Q = 1$, $\overline{Q} = 0$ Choice (B)

16. From the given circuit

$$I_E = \frac{24 - 4.5}{8} \text{ mA} = 2.43\,75 \text{ mA}.$$

Given $\beta = 50$

$V_E = I_E \cdot R_E = 2.4375 \times 250\ 10^{-3}$

$V_E = 0.61$ Volts

$V_B = 0.7 + V_E = 1.31$ Volts.

$V_{CE} = 4.5$ V

$V_C = 4.5 + V_E = 5.11$ Volts.

$I_E = (1 + \beta)\ I_B$

$I_B = 47.79\ \mu A$

$$\frac{V_0 - V_B}{R} = I_B$$

$$R = \frac{5.11 - 1.31}{47.79} \times 10^6$$

$R = 79.5\ 1\text{k}\Omega$. Choice (A)

17. From the given circuit

Base emitter junction forward bias.

$V_B > V_E$

and collector base junction reverse bias $V_{CB} = 0$

Choice (B)

18. BJT $\rightarrow$ early effect

LASER $\Rightarrow$ coherent

mos capacitor $\Rightarrow$ flat band voltage

photo diode $\Rightarrow$ dark current Choice (D)

19. $V_L = V_Z = \dfrac{R_L . V_{in}}{R + R_L}$

$$V_{i\,\min} = \frac{(R + R_L)}{R_L} V_Z = \frac{1750}{1500} \times 20\text{V} = 23.33\text{V}$$

$V_{i\ max} = I_{R\ max} \cdot R + V_Z$

$I_{R\ max} = I_{zm} + I_L = 50\text{mA} + 13.33$ mA

$= 63.33$ mA

$V_{i\ max} = 63.33 \times 10^{-3} \times 250 + 20$

$= 35.83$ volts Choice (C)

20. Given $V_{DS} = V_{GS}$

$\therefore$ $V_{DS(\min)} = V_{GS}$ = MOSFET operates in saturation region

$\therefore$ $I_D = k(V_{GS} - V_T)^2$

$\therefore$ $I_D\ \mu\ (V_{GS} - V_T)^2$

$$\frac{I_{D_2}}{I_{D_1}} = \frac{(V_{GS_2} - V_{Tn})^2}{(V_{GS_1} - V_{Tn})^2}$$

$$I_{D2} = \frac{(1.5 - 1.25)^2}{(3 - 1.25)^2} \times 1.5 \times 10^{-3} = 30.61\ \mu A$$

Choice (D)

21. The given circuit represents an integrator

$$\therefore\ V_0 = \frac{-1}{RC} \int V_{in} . dt$$

$$V_0 = \frac{-1}{100 \times 10^3 \times 10^{-5}} [5 + 1.5t^2]\,dt$$

$$= -\int \left[5 + \frac{3}{2} . t^2\right] dt$$

$$= -\left[5t + \frac{3}{2}\frac{t^3}{3}\right] = -\left|5t + \frac{t^2}{2}\right|$$

At $t = 0.5$ sec

$$V_0 = -\left[\frac{5}{2} + \frac{1}{16}\right] = -2.5625 \text{ Volts}$$ Choice (D)

22. $f_T = \dfrac{g_m}{2\pi\{C_{gs} + C_{gd}\}}$

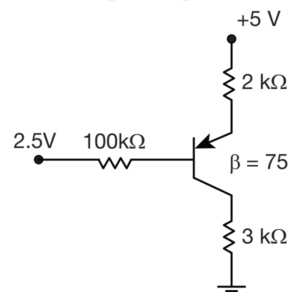
$I_D = k_n\{V_{GS} - V_{TN}\}^2$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = 2\text{K}_n[V_{GS} - V_{Tn}]$$

$g_m = 2 \times 0.5 \times 2\mu\text{AV}^2 = 2\text{mA/V}^2$

$$\therefore\ f_T = \frac{2 \times 10^{-6} \times 10^{12}}{2\pi\{0.25\}} = 1.273 \text{ MHz}$$ Choice (D)

23. Applying KVL to the input loop



$5 - I_E R_E - 0.7 - R_B I_B - 2.5 = 0$

$I_B = 7.14\mu A$

Applying KVL to the O/P loop.

$$I_C = \frac{5 - 0}{5} \text{ mA}$$

$I_{Csa_t} = 1$ mA

$I_{cactive} = \beta \cdot I_{Bactive}$

$= 75 \times 7.14 \times 10^{-6}\text{A} = -0.5355$ mA

$I_{Cactive} < I_{csat}$

$\therefore$ Transistor is in active mode. Choice (C)

24. During $+Ve$ half cycle $D \rightarrow$ ON

$-Ve$ half cycle $D \rightarrow$ OFF

t indicates half wave rectifier

$$\therefore\ I_{avg} = \frac{I_m}{\pi}$$

$$\text{But } I_m = \frac{V_m}{R_f + R_L} = \frac{4}{3.25} \text{ mA} = 1.23 \text{ mA}$$

$$I_{avg} = \frac{1.25}{\pi} \text{ mA} = 0.39\text{mA}$$

$$I_{rms} = \frac{I_m}{2} = 0.615 \text{ mA}$$ Choice (D)

25. For M_2 transistor $V_{GS2} = 5 - 0 = 5$ V
$V_{DS2} = V_0 = 0.5$ V
$\therefore$ $V_{DS2} < V_{GS2} - V_T$
$\therefore$ M_2 is in non saturation region
given $V_T = 0.3$V
For M_1 transistor
$V_{GS1} = 5 - V_0 = 5 - 0.5 = 4.5$ V
$V_{DS1} = 5 - V_0 = 4.5$
$V_{GS} - V_T = 4.5 - 0.3 = 4.2$
$V_{DS1} > V_{GS1} - V_T$
M_1 in saturation region
$\therefore$ $V_{DS1} = 4.5 > 4.2$V
$\therefore$ M_1 in saturation region

$$K_n^1 \times \left(\frac{W}{L}\right)_1 [V_{GS1} - V_T]^2$$

$$= K_n^1 \times \left(\frac{W}{L}\right)_2 \left[(V_{GS2} - V_T)V_{DS2} - V_{DS}^2\right]$$

$$2 \times 17.64 = \left(\frac{W}{L}\right)_2 \times [4.7 \times 0.5 - 0.25]$$

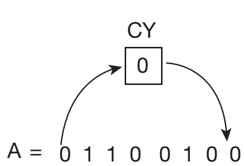
$$\left(\frac{W}{L}\right)_2 = \frac{35.28}{2.1} = 16.8$$ Choice (B)

26. Given 8 bit DAC
Output current is 5.8mA
For input $(10010001)_2 = (145)_{10}$
$I_o = K$(input in Decimal)
5.8 mA = k (145)

$$k = \frac{5.8\text{mA}}{145} = 0.04\text{mA}$$

For input $(11110100)_2 = (244)_{10}$
$I_o = k$ (input) = 0.04 × 244
= 9.76 mA Choice (B)

27. MVI A, 64 H – move 64 H to Accumulator
MOV B, A → move (64H) A to B.
STC – set carry (CY = 1)
CMC – complement carry (CY = 0)
RAL – Rotate Accumulator left Arithmetically
Before RAR



after RAR

CY $\boxed{0}$

A = 11001000

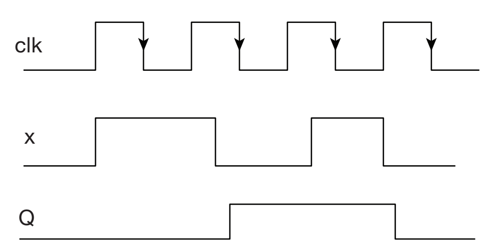
XRA B → XOR Accumulator with B
A = 11001000
B = 01100100
10101100 = ACH Choice (D)

28. LXI H, 4123H → 4123H are moved to HL register pair, i.e., H = 41H, L = 23H.
M stands for Memory Address specified by HL register pair
MOV A, M- contents of memory location (Here 4123H) are moved to Accumulator
CMA – Complement Accumulator
MOV M, A – Contents of Accumulator are moved to memory location 4123H (HL contents)
i.e., the complemented contents
XRA A → XOR ACC with Acc only
So Acc = 00H. – reset Accumulator

Choice (C)

29. Base 9 and base 3 are related ($3^2 = 9^1$)
2 digits of base 3 is equal to base 9 one digit.
base 3 base 9
00 – 0
01 – 1
02 – 2
10 – 3
11 – 4
12 – 5
20 – 6
21 – 7
22 – 8
100 – 10
Given number in base 3 is
01 10 12 22. 20 11 21
1 3 5 8 . 6 4 7
(1358 . 647) Choice (A)

30. given is D flip flop
$Q_{n+1} = D$
$= x \oplus \overline{Q_n} = x \,\Theta\, Q_n$
$Q_{n+1} = Qn$ when $x = 1$
$Q_{n+1} = \overline{Q_n}$ when $x = 0$



Choice (A)

31. The function output is 1 when ever the product of N_1, N_2 is less than or equal to 2
The minterms will be

N_1 AB \ N_2 CD	0 00	1 01	3 11	2 10
0 00	1	1	1	1
1 01	1	1		1
3 11	1			
2 10	1	1		

The max terms will be (for POS form)

AB \ CD	00	01	11	10
00				
01			0	
11		0	0	0
10			0	0

So $F = \left(\bar{A}+\bar{C}\right)\left(\bar{B}+\bar{C}+\bar{D}\right)\left(\bar{A}+\bar{B}+\bar{D}\right)$ Choice (D)

32. The excitation tables for *JK*, *D* are

Q_1 Q_O	J K	D
0 0	0 X	0
0 1	1 X	1
1 0	X 1	0
1 1	X 0	1

Present state		Next state		Inputs		
Q_1	QO	Q_1	QO	J_1	K_1	DO
0	0	1	0	1	X	0
1	0	1	1	X	0	1
1	1	0	1	X	1	1
0	1	0	0	0	X	0

From the above table

Writing the inputs interms of present state

$D_o = Q_1\ J_1 = \overline{Q_0}$, $K1 = Q_O$ Choice (C)

33. When we consider two min terms AND operation

$mi.\ mj = 0$ if $i \neq j$

ex :– $A\bar{B}C.A\bar{B}\bar{C} = 0$

$ABC.\overline{ABC} = 0$

$mi.\ mj = mi$ if $i = j$

ex :– $A\overline{BC}.A\overline{BC} = A\overline{BC}$

If two functions ANDed with minters

Then resultant is common min terms of the two functions

Example:

If $F1\ (a,b,c) = m_1 + m_2 + m_3$

$F2\ (a,b,c) = m_3 + m_4$

$F_1 . F_2 = (m_1 + m_2 + m_3)\ (m_3 + m_4)$

$= m_1 . m_3 + m_1 . m_4 + m_2 . m_3 + m_2 . m_4 + m_3 . m_3 + m_3 . m_4$

$= m_3$ (all other terms will be zero)

In the given problem $F(A,B,C) = \overline{X.Y}$

$= \Sigma m(1,3,4,5,7)$

So $XY = \Sigma m\ (0,2,6)$ (the remaining min terms)

$G(A,B,C) = Y.Z = \Sigma m\ (4,6)$

X and Y are having (0, 2, 6) min terms in common, i.e., Y will have all these 3 min terms

Similarly Y and Z have (4,6) min terms in common,

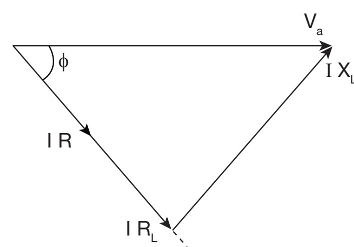
So Y will have these 2 min terms also

So $Y = \Sigma m\ (0, 2, 4, 6)$ Choice (C)

34. given function is in standard POS form

$f(P,Q,R) = \pi M\ (5, 6, 4)$

$= \Sigma m\ (0,1,2,3,7)$



$f\,(P, Q, R) = \overline{P} + QR$ Choice (A)

35. LXI H 4C38*H* → copy 4C38 H to HL register pair, i.e. H = 4CH, L = 38 H

MOV A, L → Move L = 38H to Accumulator,

ADD H → Add H = 4CH add Acc = 38H

Store in Accumulator

Acc = 0011 1000

H = 0100 1100

Acc = 10000100

Acc = 84H, and there is a auxiliary carry

DAA → Decimal Adjust Accumulator, if the reset is having any number more than 9 or if there is any auxiliary carry then DAA will add 6 to the result in Accumulator,

So Acc = 84 H + 06H = 8AH

MOV H, A → Acc = 8*A* H will be moved to H register.

Now HL = 8A38H

PCHL → Copy HL to program cainter

So PC = 8A38H Choice (C)