Chapter 2

Transistor Biasing

CHAPTER HIGHLIGHTS

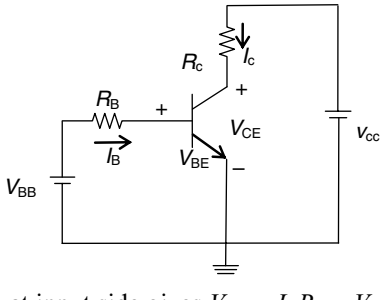
- *The Operating Point*
- *Bias Stability*
- *Biasing the BJT*
- *Bias Compensation*
- *Thermistor Compensation*
- *Sensistor Compensation*
- *Thermal Run Away*
- *Thermal Resistance*
- *Heat Sink*
- *Biasing the FET*

The Operating Point

A transistor is a current-controlled three-terminal device having two junctions, namely base–emitter junction and base–collector junction

Base—emitter junction	Base–collector junction	Application	Region of operation
FB	FB	ON switch	Saturation
FB	RB	Amplifier	Active
RB	FB	–	Inverse active
RB	RB	OFF switch	Cut-off

Transistor Circuit Under DC Condition



Apply KVL at input side gives $V_{BB} - I_B R_B - V_{BE} = 0$

$$\Rightarrow V_{BE} = V_{BB} - I_B R_B$$

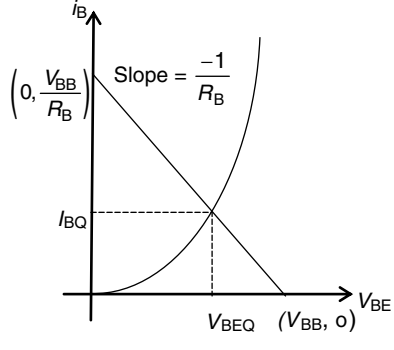
When $$V_{BE} = 0 \Rightarrow I_B = \frac{V_{BB}}{R_B}$$

$$I_B = 0 \Rightarrow V_{BE} = V_{BB}$$

DC load line is the line joining the two points.

$$(V_{BB}, 0) \text{ and } \left(0, \frac{V_{BB}}{R_B}\right)$$

Input Characteristics of CE Transistor



Intersection of the load line with the characteristics of the transistor gives the Q point (operating point)

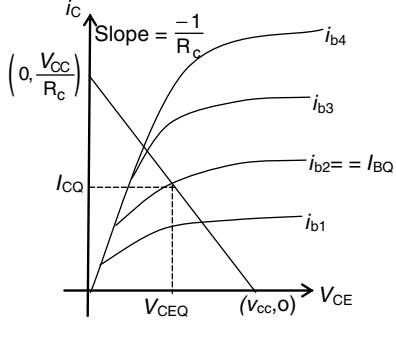
Apply KVL at the output.

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = 0 \Rightarrow I_C = \frac{V_{CC}}{R_C}$$

$$I_C = 0 \Rightarrow V_{CE} = V_{CC}$$

Output Characteristics of a CE Transistor

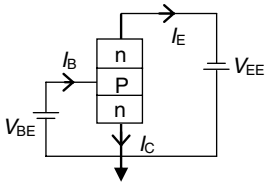


Intersection of the load line with the output characteristics for a particular value of I_B gives the Quiscent point/ operating point.

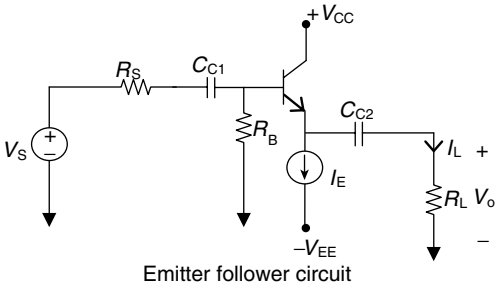
Hence, 'Q' point is given by $Q(I_{CQ}, V_{CEQ})$

Common Collector Amplifier

This is also known as emitter follower. This configuration mainly used for impedance matching because of it's high-input impedance and low-output impedance.

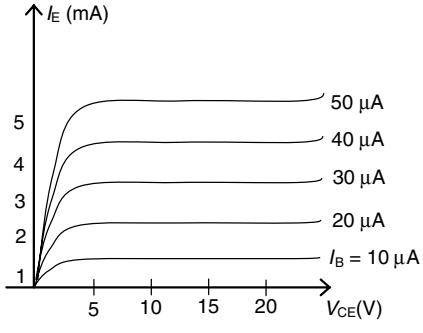


Notation of common collector configuration.



Emitter follower circuit

Output characteristics of common collector configuration are a plot of emitter current I_E versus V_{CE} for a range of I_B



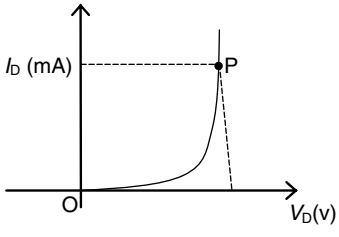
Output characteristics of common emitter configuration.

Static and Dynamic Resistance

DC (or) static resistance.

Operating point (Q) will not change with time if input voltage is DC.

DC resistance is the ratio of voltage to current at operating point.

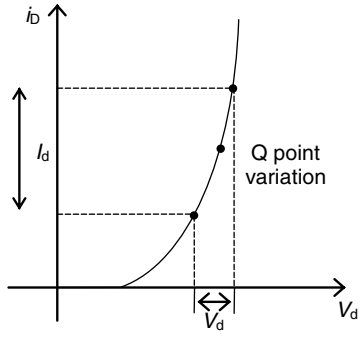


At point P, $R_D = \dfrac{V_D}{I_D}$

DC resistance is independent of the shape of characteristic surrounded by the point.

AC (or) Dynamic Resistance

If input is sinusoidal signal, then operating point moves up and down and thus gives a specific change in current and voltage.

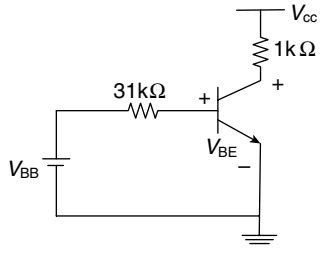


AC resistance $r_d = \dfrac{\Delta V_d}{\Delta I_d}$

Solved Examples

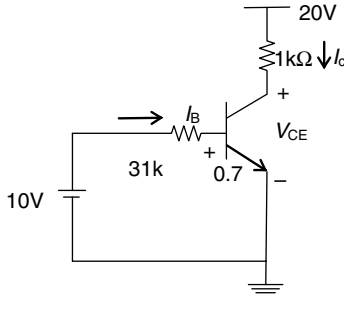
Example 1

Determine the 'Q' point for the following circuit if $\beta = 50$ and $V_{BB} = 10$ volts, $V_{BE} = 0.7$ volts, $V_{CC} = 20$ volts



(A) (0.3 mA, 5 V)
(B) (15 mA, 5 V)
(C) (0.6 mA, 4 V)
(D) (15 mA, 4 V)

Solution



Writing KVL for the base emitter loop gives

$$10 - 31\, I_B - 0.7 = 0$$

$$\Rightarrow I_B = 0.3 \text{ mA}$$

$$I_{CQ} = \beta\,(0.3 \text{ mA}) = 15 \text{ mA}$$

Writing KVL for the collector loop gives

$$20V - I_C\,(1\ \text{k}\Omega) - V_{CE} = 0$$

$$\Rightarrow V_{CE} = 20 - (15 \text{ mA})\,(1\text{k})$$

$$= 20 - 15$$

$$V_{CE} = 5 \text{ Volts}$$

$$(I_C, V_{CEQ}) = (15 \text{ mA}, 5 \text{ V})$$

BIAS STABILITY

Operating point defines where the transistor will operate on its characteristics curve, under DC conditions. For linear (minimum distortion) amplification, the DC operating point should not be too close to the maximum power and voltage or current rating and should avoid the regions of saturation and cut-off. To keep the operating point stable, we use external network to bias the transistor.

The stability of operating point depends on V_{BE}, β, I_{CO}. β is very sensitive to temperature, and V_{BE} decreases about 2.5 mV for each 1°C increase in temperature. The reverse saturation current typically doubles for every 10°C increase is temperature.

Stability Factor (S)

$$I_C = f(I_{CO}, V_{BE}\,\beta)$$

$$S = \frac{\partial I_C}{\partial I_{CO}},\ S^1 = \frac{\partial I_C}{\partial V_{BE}}.\ S^{11} = \frac{\partial I_C}{\partial \beta}$$

$$I_C = \beta\, I_B + (1 + \beta)\, I_{CO}$$

Differentiating with respect to I_C gives

$$1 = \beta\,\frac{\partial I_B}{\partial I_C} + (1 + \beta)\,\frac{\partial I_{CO}}{\partial I_C}$$

$$\Rightarrow 1 = \beta\,\frac{\partial I_B}{\partial I_C} + \frac{1+\beta}{S}$$

$$\Rightarrow S = \frac{1+\beta}{1-\beta\dfrac{\partial I_B}{\partial I_C}}$$

Where 'S' is the stability factor

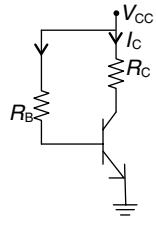
Smaller value of 'S' is desirable for a proper biasing of circuit to act as an amplifier.

The networks are the most stable and least sensitive to temperature changes have the smallest stability factors

BIASING THE BIPOLAR JUNCTION TRANSISTOR (BJT)

Base Bias or Fixed Bias

Input loop



$$V_{CC} = I_B R_B + V_{BE}$$

$$I_b = \frac{V_{CC} - V_{BE}}{R_B}$$

Output loop

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$I_C = \beta I_b = \beta\left(\frac{V_{CC} - V_{BE}}{R_b}\right)$$

Voltage drop across R_C can never be greater than V_{CC}.

$$I_C R_C < V_{CC} \Rightarrow I_C < \frac{V_{CC}}{R_C}$$

If I_C becomes greater than this value, the operating point will lie in saturation region,.

$$\text{Stability factor} = S = 1 + \beta \qquad \left(\because \frac{\partial I_B}{\partial I_C} = 0\right)$$

It is a simple circuit with few parts.

Operating point can be fixed anywhere in active region, by simply varying R_B

I_C depends on β, β in turn unstable with respect to temperature, this biasing in useful is switching and digital applications.

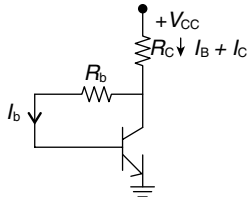
Collector-to-Base Bias Circuit

Input loop

$$V_{CC} - (I_B + I_C)\, R_C - R_b\, I_B - V_{BE} = 0$$

$$\Rightarrow \frac{\partial I_B}{\partial I_C} = \frac{-R_C}{R_C + R_B}$$

$$I_b = \frac{I_C}{\beta}$$



$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{(\beta+1)R_C + R_B}$$

$$\therefore I_C = \frac{\beta(V_{CC} - V_{BE})}{(\beta+1)R_C + R_B}$$

If 'β' is very large ($I_B = 0$), then the approximate value of

$$I_C = \frac{V_{CC} - V_{BE}}{R_C}$$

KVL at output side:

$$V_{CC} - (I_C + I_B)\, R_C - V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{CC} - (I_C + I_B)\, R_C$$

If $(\beta+1)\, R_C >> R_B$, then $I_C = \frac{V_{CC} - V_{BE}}{R_B}$ independent of 'β'

The feedback resistor R_B provides negative feedback for AC input consequently reduces the AC gain of the circuit.

$$\text{Stability factor } S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C + R_B}\right)}$$

Collector to base bias is having lesser stability factor than fixed bias. Thus, it provides better stability.

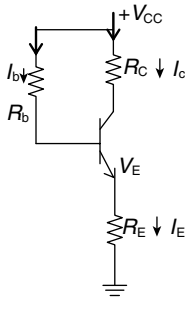
Emitter Feedback Bias

$$I_E = I_C + I_B$$

$$V_E = I_E\, R_E = (I_C + I_B)\, R_E$$

$$V_B = V_{BE} + (I_C + I_B)\, R_E$$

$$I_B = \frac{V_{CC} - V_B}{R_b}$$



Output loop

$$(I_C + I_B)\, R_E + R_C\, I_C - V_{CC} + V_{CE} = 0$$

$$\text{Stability factor } S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E + R_b}\right)}$$

I_C can be made insensitive to β, if we choose

$$R_E >> R_b$$

Advantages

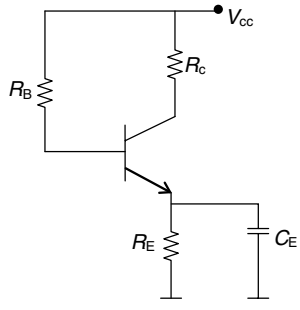
(i) Simplest biasing scheme

(ii) Better stability over fixed Bias if $R_E >> \frac{R_B}{(\beta+1)}$

Disadvantages

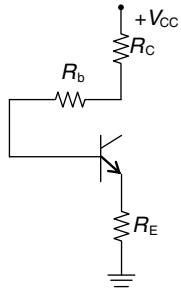
(i) The resistor R_E provides a negative feedback for AC input consequently reduces the gain

To increase the stability of the emitter feedback circuit, a bypass capacitor has been placed in parallel with R_E



The purpose of bypass capacitor is to make $R_E = 0$ for AC input and hence no gain reduction at the output of the circuit

Collector–Emitter Feedback Bias



By applying KVL to the circuit, the output loop will be as follows:

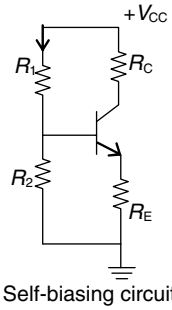
$$V_{CC} - (I_C + I_B)\, R_C - V_{CE} - R_E\, (I_C + I_B) = 0$$

Then, the input loop will be as follows:

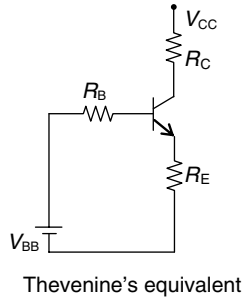
$$V_{CC} - (I_C + I_B)\, R_C - I_B R_b - V_{BE} - R_E\, (I_B + I_C) = 0$$

$$\text{Stability factor } S = \frac{1+\beta}{1+\beta(R_e + R_b)/(R_e + R_c + R_b)}$$

Self-Bias, Emitter Bias, or Voltage-Divide Bias



Self-biasing circuit



Thevenine's equivalent circuit

$$V_{BB} = \frac{R_2 . V_{CC}}{R_2 + R_1}, R_B = \frac{R_2 R_1}{R_2 + R_1}$$

Input loop

$$V_{BB} = I_B R_B + V_{BE} + (I_b + I_c)R_e$$

Output loop

$$V_{cc} - R_C I_c + V_{CE} + (I_b + I_c)R_c$$

Stability factor $S = \dfrac{1+\beta}{1+\beta\left(\dfrac{R_E}{R_E + R_B}\right)}$

KVL at input side is as follows:

$$V_{BB} - I_B R_B - V_{BE} - (I_B + I_C)R_E = 0$$
$$I_C = \beta I_B$$
$$\Rightarrow I_B = \frac{V_{BB} - V_{BE}}{(\beta+1)R_E + R_B} \Rightarrow I_C = \frac{\beta(V_{BB} - V_{BE})}{(\beta+1)R_E + R_B}$$

KVL at output side is as follows:

$$V_{cc} - I_c R_c - V_{CE} - (I_B + I_c)R_E = 0$$
$$\Rightarrow V_{CE} = V_{cc} - I_c R_c - (\beta + 1) I_B R_E$$

If 'β' is very large, then approximate value of

$$I_c \simeq \frac{V_{BE} - V_{BE}}{R_E}$$

Where $V_{BB} = \dfrac{V_{CC} \cdot R_2}{R_1 + R_2}$

$$R_B = R_1 \| R_2$$

If $(\beta + 1)\, R_E >> R_B$, then I_c is independent of 'β'

1. Better stability over, all biasing schemes if

$$R_E >> \frac{R_B}{(1+\beta)}$$

2. Most of the amplifiers uses self-biasing scheme.

BIAS COMPENSATION

Compensation Techniques

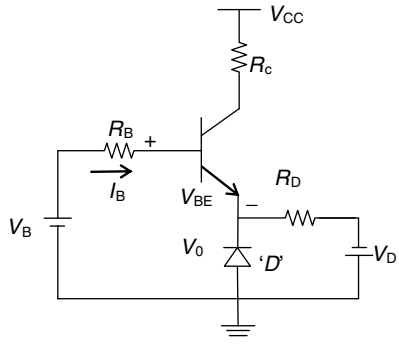
$$I_c = f(I_{co}, V_{BE}, \beta)$$

I_{co} (reverse saturation current), V_{BE}, and β are temperature-dependent parameters. Hence, to stabilize the circuit against the variation in temperature, that is, (to make I_c independent of I_{co}, V_{BE}, β) compensation techinques are used.

1. Reverse saturation current doubles for every 10°C rise in temperature.
2. V_{BE} decreases for 7.5 mv for 1°C rise in temperature

Compensation for V_{BE}

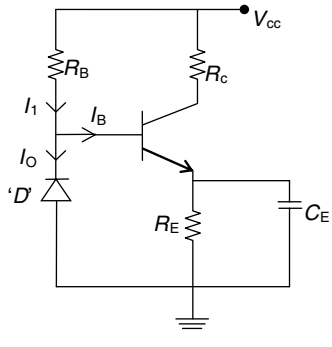
If the values of V_D and R_D are designed such that the voltage across the diode is V_{BE} from P–N side, I_B is $V_B - I_B R_B - V_{BE} + V_{BE} = 0$



$$I_B = \frac{V_B}{R_B} \text{ gives } I_c = \frac{\beta V_B}{R_B} \text{ independent of } V_{BE}$$

V_{BE} tracks V_0 with respect to temperature, and hence, I_C will be insensitive to variations in V_{BE}.

Compensation for I_{co}



Let us assume that the transistor and the diode are made up of same material. Hence, I_{co} is same for both

$$\therefore I_c = \beta I_B + (1 + \beta) I_{co}$$

$$I_c = \beta (I_1 - I_0) + (1 + \beta) I_{co} \quad (\because \text{ from the Figure})$$

If 'β' is assumed to be so large and $I_0 = I_{co}$

$$\Rightarrow \beta + 1 \simeq \beta$$

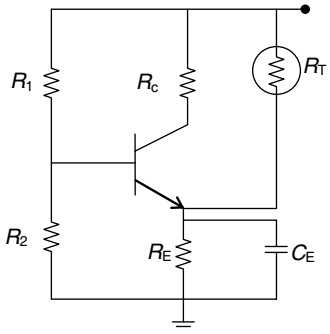
$$I_c = \beta I_1 - \beta I_0 + \beta I_{co}$$

$I_c = \beta I_1$ which is independent of reverse saturation current.

If the diode and transistor are of the same type, and material, the reverse, saturation current of diode will increase with temperature at the same rate as the transistor collector saturation current I_{CO}

Thermistor Compensation

The thermistor has a negative temperature coefficient its resistance decreases exponentially with increase in temperature



As T rises, R_T decreases, and the current fed through R_T into R_e increase. Since the voltage drop across R_e is in the direction to reverse bias the transistor. The temperature sensitivity of R_T acts so as to tend to compensate the increase in I_C due to temperature.

Sensistor Compensation

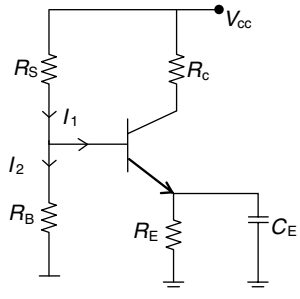


Figure 1 R_s sensistor

Sensistor is having a positive temperature coefficient of resistance whose resistance increases, as temperature increases, (as the collector current is increasing). Hence, the current through sensistor decreases

$$I_B = I_1 - I_2$$

I_1 decreases and I_B also starts decreasing.

Since $I_c = \beta I_B$, the collector current is in control, thus providing a better stability.

Thermal Runway

Power dissipated at collector causes self-heating, as a consequence junction temperature rises, and in turn, this increases collector current with a subsequent increase in power dissipation. If this phenomenon (known as thermal runway) continues, it may result in permanently damaging the transistor.

Thermal Resistance

It is found that steady-state temperature rises at the collector junction is proportional to the power dissipated at the junction.

$$\Delta T = T_J - T_A = \theta P_D$$

T_J – Junction temperature
T_A –Ambient temperature
P_D – Power dissipated at collector junction
θ – Thermal resistance

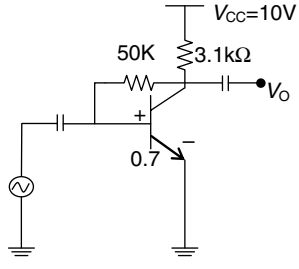
The required condition for thermal stability is the rate at which heat is released must not exceed the rate at which the heat can be dissipated $\frac{\partial P_C}{\partial T_j} < \frac{\partial P_D}{\partial T_j} \Rightarrow \frac{\partial P_C}{\partial T_j} < \frac{1}{\theta}$ is the condition to avoid thermal runway.

Heat Sink

It is a device that cools the diode or transistor by dissipating heat into surrounding.

Example 2

Find the DC collector current if $V_{BE} = 0.7$ volts and 'β' is considered as very large



(A) 2 mA (B) 4 mA (C) 5 mA (D) 3 mA

Solution

$$I_c = \frac{\beta(V_{CC} - V_{BE})}{(\beta+1)R_C + R_B}$$

As 'β' is large

$$(\beta + 1)\, R_C \simeq \beta\, R_C >> R_B$$

$$I_C \simeq \frac{V_{CC} - V_{BE}}{R_C}$$

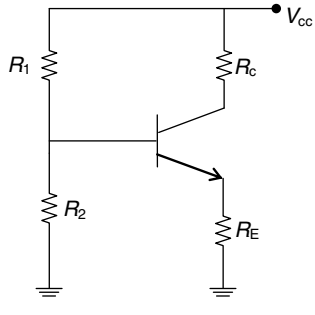
$$= \frac{10 - 0.7}{3.1\text{k}\Omega}$$

$$I_c = 3 \text{ mA}.$$

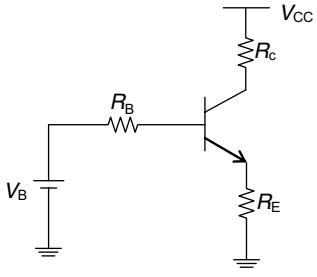
Example 3

A common emitter amplifier has a potential divider bias using $V_{cc} = 20$ volts, $R_1 = R_2 = 6.2$ kΩ and $V_{BE} = 0.7$ volts, β is assumed to be so large then, the operating point is (Given R_c as 1 kΩ and R_E as 2 kΩ)

(A) (4.65 mA, 6.05 volts) (B) (3 mA, 12 volts)
(C) (9 mA, 6 volts) (D) (9 mA, 14 volts)



Solution



$$V_{BB} = \frac{V_{CC} \cdot R_2}{R_1 + R_2} = 10 \text{ volts}$$

$$R_B = R_1 \| R_2 = 3.1 \text{ k}\Omega$$

$$I_c = \frac{\beta(V_{BB} - V_{BE})}{(\beta + 1)R_E + R_B}$$

As 'β' is very large, that is, $(\beta + 1)\, R_E >> R_B$

$$\therefore I_c \simeq \frac{V_{BB} - V_{BE}}{R_E}$$

$$I_c = \frac{10 - 0.7}{3.1\text{k}\Omega}$$

$$I_c = 4.65 \text{ mA}$$

Apply KVL at output side.

$$V_{CEQ} = V_{cc} - I_{CQ}R_c - I_E R_E \text{ as '}\beta\text{' is large } I_E \simeq I_{CQ}$$

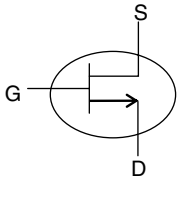
$$\therefore V_{CEQ} = V_{cc} - I_{CQ}(R_c + R_E)$$

$$= 20 - (4.65 \text{ mA})\,(1 + 2\text{k}\Omega)$$

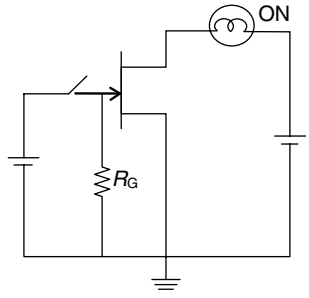
$$V_{CEQ} = 6.05 \text{ volts.}$$

Biasing the Field Effect Transistor (FET)

1. Field Effect transistor (FET) is a voltage controlled Device having 3 terminals Gate, source and Drain



2. FET is a symmetrical Device (i.e. Source and Drain are interchangable)
3. FET acts as a better switch over BJT

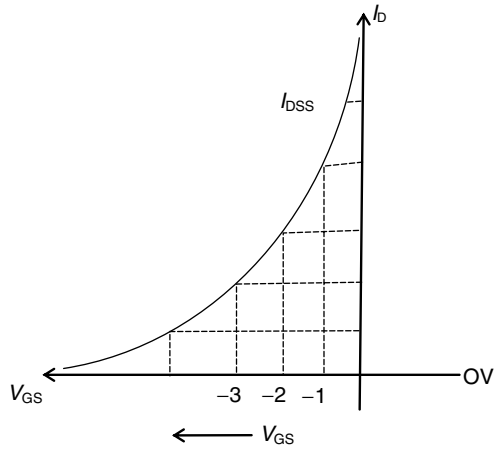


For junction field effect transistor (JFET) and depletion mode MOSFET'S Shockley's equation is valid.

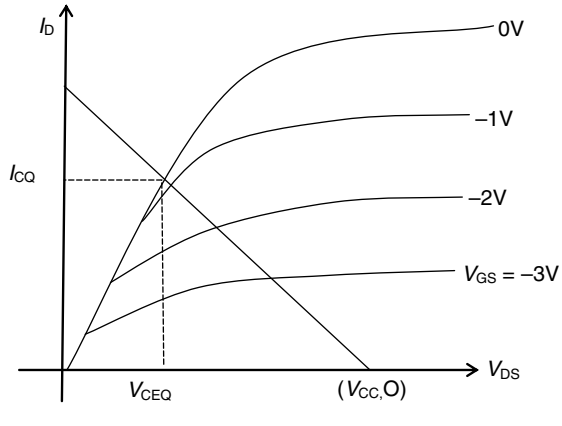
R_G is called the bleeder Resistor, FET is ON when input circuit is open

$$\therefore I_G = 0$$

Transfer characteristics



Output characteristics



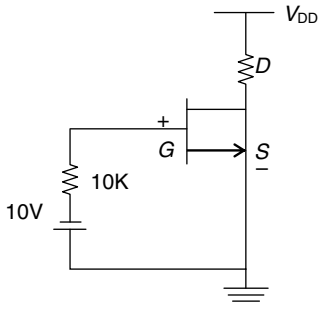
Transfer characteristics are governed by the equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

When I_D = drain current, $I_D = I_{DSS}$. When $V_{GS} = 0$, that is, drain saturation current V_P = pinch off voltage.

Example 4

Find I_D, V_{GS} for the given circuit assuming $V_{DD} = 30$ volts, $V_P = -5$ volts, $I_{DSS} = 30$ mA



(A) 0.27 amp, 10 volts
(B) 0.27 amp, 20 volts
(C) 0.135 amp, 10 volts
(D) 0.27 amp, −10 volts

Solution

$$I_G = 0 \text{ Amps}$$

Apply KVL at input side gives

$$-10 - V_{GS} - 0\,(10k) = 0$$

$$V_{GS} = -10 \text{ volts}$$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$= 30 \text{ mA}\left[1 + \frac{10}{5}\right]^2$$

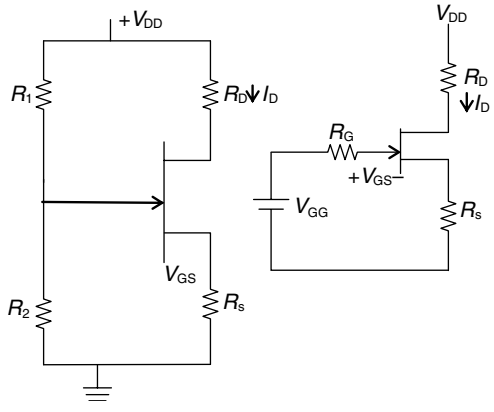
$$= 270 \text{ mA}$$

$$I_D = 0.27 \text{ amps.}$$

In MOS circuits biasing schemes, control deviations in the operating point caused by fabrication variations in the threshold voltage V_T and transconductance (processing) parameter k. Both integrated circuits and discrete component JFET circuits are biased so that the effects of unit to unit variations in the pinch off voltage V_P and zero bias drain saturation current I_{DSS} are controlled.

BJT	FET
(i) Current-controlled device.	(i) Voltage-controlled device.
(ii) Apply KVL at input gives I_B	(ii) $I_G = 0$ Amps
(iii) $I_C = \beta I_B$	(iii) $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$
(iv) Not symmetrical	(iv) Symmetrical device (source and drain are interchangable)

Four-Resistor Bias Circuit



$$V_{GG} = \frac{R_2}{R_1 + R_2} \cdot V_{DD}$$

$$R_G = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}, \; I_s = I_D$$

By KVL for the gate loop, $-V_{GG} + V_{GS} + I_D R_S = 0$

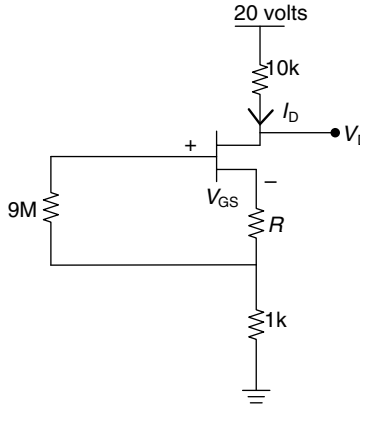
By KVL for drain and source loop,

$$-V_{DD} + R_D I_D + V_{DS} + R_S I_D = 0$$

In this analysis, $I_G = 0$ was assumed. However, the small reverse saturation current I_{GSS} exits in the gate loop. The resistance R_G is selected to be as large as it is feasible while maintaining the voltage drop ($I_{GSS} R_G << V_{GG}$) at a negligible value.

Example 5

Find the value of resistor 'R'. If the drain to ground voltage = 0. Given $I_{DSS} = 50$ mA, $V_p = -6$ volts



(A) 1.2 kΩ
(B) 1.4 kΩ
(C) 1.3 kΩ
(D) 1.5 kΩ

Solution

$$I_G = 0 \text{ Amps}$$

$$I_D = \frac{20 - V_D}{10\text{k}}$$

$$I_D = \frac{20 - 0}{10\text{k}} \simeq 2 \text{ mA}$$

$$I_D = I_S = 2 \text{ mA}$$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$2 \text{ mA} = 50 \text{ mA}\left[1 + \frac{V_{GS}}{6}\right]^2$$

$$\Rightarrow 1 + \frac{V_{GS}}{6} = \frac{1}{5}$$

$$\Rightarrow V_{GS} = -4.8 \text{ volts}$$

KVL at input gives

$$-V_{GS} - I_D[R + 1\text{ k }\Omega] = 0$$

$$\Rightarrow 4.8 = I_D[R + 1\text{ k}\Omega]$$

$$\Rightarrow 4.8 = 2\text{ mA }[R + 1\text{ k}\Omega]$$

$$\Rightarrow R = 1.4\text{ k}\Omega.$$

JFET as Analog Switch

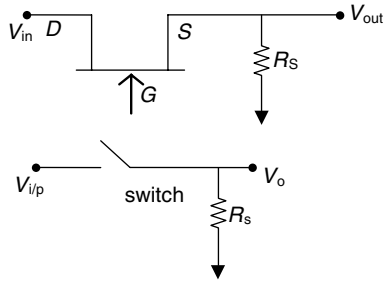
JFET can be used as multiplexer, amplifier, switch, etc. Major application of JFET is analog switch.

For analog switch, we consider two points that are lie in cut-off and saturation region.

If FET is in saturation region, then it acts as a closed switch. If it is in cut-off region, then it acts as an open switch.

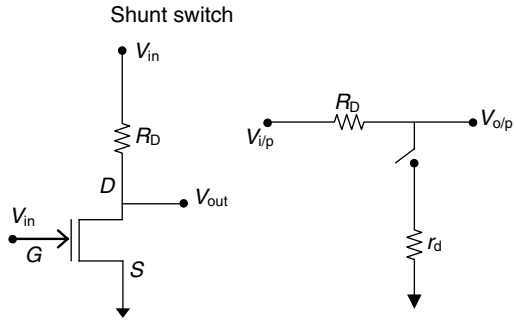
FET can be used as a series switch or shunt switch

Series Switch



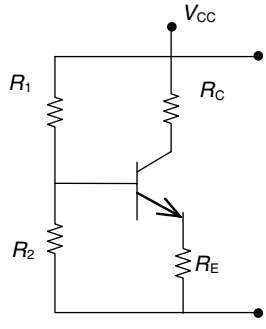
FET as a series switch, equivalent circuit.

Shunt Switch



Example 6

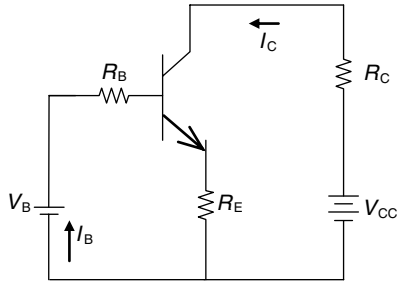
A common emitter amplifier has a potential divider bias using $V_{CC} = 12$V. If $R_C = 4$ kΩ, $R_E = 1$ kΩ, $R_1 = 20$ kΩ, $R_2 = 5$ kΩ, $V_{BE} = 0.6$ V, $\beta = 100$, and then, the operating point is_____.



(A) 5 V, 1 mA
(B) 4 V, 1.4 mA
(C) 5.14 V, 1.2 mA
(D) 3.41 V, 1.71 mA

Solution

$$V_B = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{5}{20 + 5} \times 12 = 2.4\text{V}$$



Writing KVL for the base–emitter loop

$$V_B = I_B \cdot R_B + V_{BE} + (I_B + I_C)R_E$$

$$R_B = \frac{R_1 \cdot R_2}{R_1 + R_2} = \frac{20 \times 5}{20 + 5} = 4\text{k}\Omega, \quad I_B = \frac{I_C}{\beta}$$

$$2.4 = \frac{I_C}{100} \times 4 + 0.6 + \left(\frac{I_C}{100} + I_C\right) \times 1$$

$$1.8 = \frac{21}{20} \cdot I_C \Rightarrow I_C = 1.714\text{mA}$$

Writing KVL for the collector loop

$$V_{CC} = I_C \cdot R_C + V_{CE} + (I_C + I_B) R_E$$

$$12 = 1.714 \times 4 + V_{CE} + \left(1.714 + \frac{1.714}{100}\right) \times 1$$

$$V_{CE} = 3.41\text{V}$$

Example 7

When β is doubled, what are the operating point and stability factor in the previous problem?

(A) 1.756 mA, 3.21 V, 4.9
(B) 1.71 mA, 3.14 V, 4.9
(C) 1.71 mA, 3.21 V, 4.81
(D) 1.756 mA, 3.21 V, 4.81

Solution

$$V_B = 2.4\text{V}, R_B = 4\text{k}\Omega, I_B = \frac{I_C}{\beta} = \frac{I_C}{200}$$

Writing KVL for the base–emitter loop

$$V_B = I_B \cdot R_B + V_{BE} + (I_B + I_C) R_E$$

$$2.4 = \frac{I_C}{200} \times 4 + 0.6 + \left(\frac{I_C}{200} + I_C\right) \times 1$$

$$= \frac{5}{200} I_C + I_C + 0.6$$

$$1.8 = 1.025 I_C \Rightarrow I_C = 1.756 \text{ mA}$$

Writing KVL for the collector loop

$$V_{CC} = I_C \cdot R_C + V_{CE} + (I_C + I_B) R_E$$

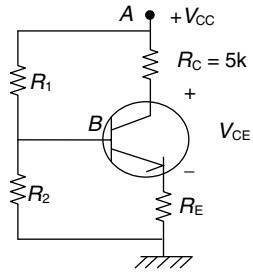
$$12 = 1.756 \times 4 + V_{CE} + \left(\frac{1.756}{200} + I_C\right) \times 1$$

$$V_{CE} = 3.21 \text{ V}$$

$$S_1 = (\beta + 1) \frac{1}{1 + \frac{\beta R_E}{R_B + R_E}} = \frac{201}{1 + \frac{200}{4+1}} = 4.9024$$

Example 8

A silicon transistor with $\beta = 100$ is to be used in the self-biasing circuit, shown in figure such that the quiescent point corresponds to $V_{CE} = 10$ V and $I_C = 2$ mA, find 'R_E' if $V_{CC} = 24$ V, $R_C = 5$ kΩ?



(A) 2 kΩ
(B) 1.98 kΩ
(C) 980Ω
(D) $R_1 \| R_2$

Solution

By applying KVL between V_{CC} and ground,

$$V_{CC} = V_{RC} + V_{CE} + V_{RE}$$
$$= I_C R_c + V_{CE} + (I_B + I_c) R_E$$

$$24\text{V} = 2 \times 10^{-3} \times 5 \times 10^3 + 10 + \left(\frac{2 \times 10^{-3}}{100} + 2 \times 10^{-3}\right) \cdot R_E$$

$$\Rightarrow R_E = \frac{4}{2 \times 10^{-3}(1.01)} = 1.98\text{k}\Omega$$

Example 9

In the above question, it is desired to have $S \le 3$, find the limiting value of R_1 and R_2 assuming $V_{BE\,(active)} = 0.65$ V.

(A) 41.39 kΩ, 10.16 kΩ
(B) 20.69 kΩ, 10.16 kΩ
(C) 20.69 kΩ, 5.08 kΩ
(D) 41.39 kΩ, 5.08 kΩ

Solution

$$S = \frac{(\beta + 1)(R_B + R_E)}{R_B + R_E(\beta + 1)} = \frac{R_B + R_E}{R_E + \frac{R_B}{\beta + 1}}$$

$$3 = \frac{101(R_B + 1.98)}{R_B + 1.98(101)}$$

$$3R_B + 599.94 = 101R_B + 199.98$$

$$98R_B = 3999.96 \Rightarrow R_B = 4.08\text{k}\Omega$$

$$R_B < 4.08\text{k}\Omega \text{ for } S \le 3$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2}, V_B = V_{CC} \cdot \frac{R_2}{R_1 + R_2}$$

By solving

$$R_1 = \frac{V_{CC} \cdot R_B}{V_B}, R_2 = \frac{R_1 V_B}{V_{CC} - V_B}$$

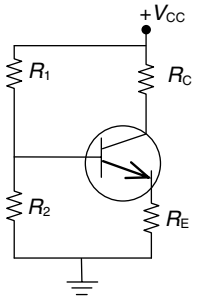
$$V_B = I_B \cdot R_B + V_{BE} + V_{RE}$$
$$= 0.02 \times 10^{-3} \times 4.08 \times 10^3 + 0.65 + 4$$
$$= 4.7312 \text{ V}$$

$$R_1 = \frac{24 \times 4.08}{4.7312} = 20.69\text{k}\Omega$$

$$R_2 = \frac{20.69 \times 4.7312}{24 - 4.73} = 5.08\text{k}\Omega$$

Example 10

Consider the transistor circuit of figure where V_{cc} = 24 V, R_C = 5.6 kΩ, R_E = 1 kΩ, R_2 = 10 kΩ, and R_1 = 80 kΩ, β = 60, V_{BE} = 0.6 V, the transistor operates in the active region. The operating point of the transistor is



(A) 1.78 mA, 13.254 V (B) 1.78 mA, 12.28 V
(C) 1.39 mA, 13.25 V (D) 1.39 mA, 12.28 V

Solution

$$R_B = \frac{R_1.R_2}{R_1 + R_2} = \frac{80x10}{80+10} = 8.89\text{k}\Omega$$

The operating point can be found from the forward characteristics by writing the bias equation

$$I_B = \frac{I_C}{\beta} = \frac{I_C}{60}$$

$$V_B = I_B R_B + V_{BE} + I_E R_E$$

$$\frac{V_{CC} \cdot R_2}{R_1 + R_2} = I_B R_B + V_{BE} + (I_C + I_B) R_E$$

$$\frac{24 \times 10}{80+10} = I_B \times 8.89 + 0.6 + (60+1) I_B \times 1$$

$$2.67 = I_B(69.89) + 0.6$$

$$I_B = 0.0296\text{mA} \Rightarrow 29.6\mu\text{A}$$

$$I_C = 60 \times 29.6\mu\text{A} = 1.78\text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C - (I_B + I_C) \cdot R_E = 12.23\text{V}$$

$$(I_{CQ}, V_{CEQ}) = (1.78\text{mA}, 12.23\text{V})$$

Example 11

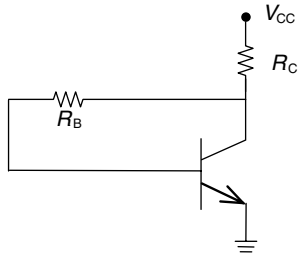
The stability factor of the above transistor is
(A) 1.99 (B) 3.13 (C) 6.31 (D) 8.63

Solution

$$S = \frac{R_B + R_E}{R_E + \frac{R_B}{\beta + 1}} = \frac{8.89 + 1}{1 + \frac{8.89}{61}} = 8.63$$

Example 12

The fixed bias circuit as shown is used as collector bias circuit, the value of R_B is? Quiescent point (9.2 mA, 4.4 V), the transistor has DC current gain 115. V_{BE} = 0.7 V, V_{CC} = 9 V, R_C = 500 Ω.



(A) 500 Ω (B) 45.75 kΩ
(C) 75.42 kΩ (D) 125.63 kΩ

Solution

$$V_{CC} = (I_B + I_C) R_C + I_B \cdot R_B + V_{BE}$$

$$9 = \left(\frac{9.2}{115} + 9.2\right) \times 0.5 + \frac{9.2}{115} \times R_B + 0.7$$

$$R_B = \frac{3.66}{0.08} = 45.75\text{k}\Omega$$

Example 13

The stability factor and the thermal stability factor for the above circuit are
(A) 62.81 and 0.525 (B) 51.71 and 0.446
(C) 42.36 and 0.345 (D) 33.81 and 0.824

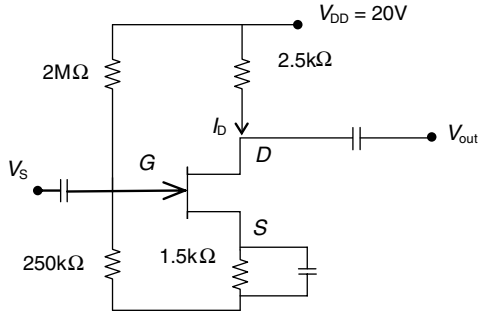
Solution

$$S = \frac{1 + h_{FE}}{1 + \frac{h_{FE} \cdot R_C}{R_C + R_B}} = \frac{1+115}{1 + \frac{115 \times 0.500}{0.5 + 45.75}} = 51.711$$

Thermal stability factor $K = \frac{S}{1 + h_{FE}} = \frac{51.7111}{116} = 0.446$

Example 14

FET voltage divider bias is shown in given figure. If I_D = 4 mA, then V_{GS} and V_{DS} will be respectively



(A) –3.78 V, 4 V
(B) 4 V and –3.78 V
(C) –3.78 V and –4 V
(D) –4 V and –3.78 V

Solution

$$V_G = \frac{20 \times 0.25}{2 + 0.25} = \frac{20}{9}$$

$$V_{GS} = V_G - I_D \cdot R_S = \frac{20}{9} - 4 \times 1.5 = -3.78\text{V}$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

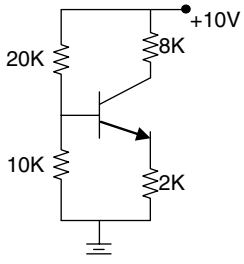
$$= 20 - 4 \times (1.5 + 2.5) = 4\text{ V}$$

EXERCISES

Practice Problems I

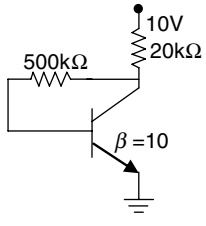
Direction for questions 1 to 25: Select the correct alternative from the given choices.

1. For the circuit showing in figure assume $\beta = 100$ for BJT, the transistor will be in



(A) Cut-off region
(B) Active region
(C) Inverse active region
(D) Saturation region.

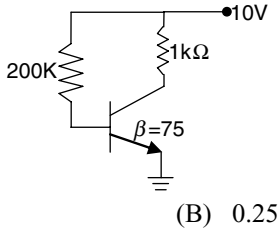
2. For the given biasing network, the stability factor '*S*' is



(A) 101 (B) 17.14 (C) 20.84 (D) 34

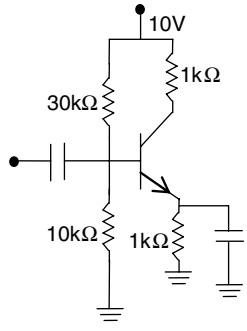
3. In a fixed bias circuit, $S = 51$ for $I_c = 2$ mA. Given $V_{cc} =$ 10volt. The value of R_B is_____
(A) 250 kΩ
(B) 250 Ω
(C) 25 kΩ
(D) 2.5 kΩ

4. In the given fixed bias circuit, $V_{CE(sat)} = 0$ volt, the minimum value of I_B to saturate the transistor is _____



(A) 10 mA
(B) 0.25 mA
(C) 0.133 mA
(D) 0.16 mA

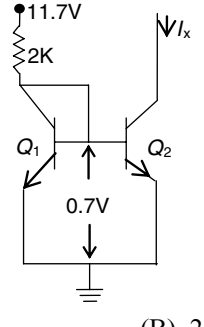
5. For the given biasing network, β is taken as very large. Assume $V_{BE} = 0.2$ V, the value of I_E and V_{CE} are ___



(A) 2.3 mA, 0 V
(B) '0'mA, 10 V
(C) 10 mA, 5.4 V
(D) 2.3 mA, 5.4 V

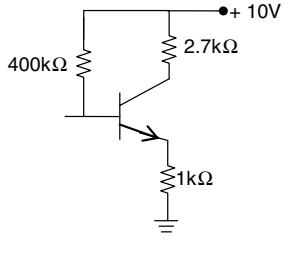
6. A Ge transistor is used in the self-bias arrangement with $V_{CC} = 20$ V, $R_C = 2$ kΩ, $R_E = 500$ Ω. The Q-point is selected at $V_{CE} = 10$ V, $I_C = 5$ mA and $S = 12$. If $V_{BE} = 0.3$ V and $\beta = 60$, then the values of R_1 and R_2 are _____
(A) 40.65 kΩ, 8.24 kΩ
(B) 8.24 kΩ, 40.65 kΩ
(C) 40.65 kΩ, 18.6 kΩ
(D) 18.6 kΩ, 4.65 kΩ

7. In the BJT current mirror shown below, assume that the emitter area of Q_1 is double that of Q_2. What is the value of I_x?



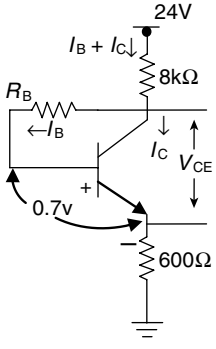
(A) 5.5 mA
(B) 2.75 mA
(C) 6.2 mA
(D) 11 mA

8. The transistor has following parameters. $\beta = 50$ and $V_{BE} =$ 0.6 V. If β is increased by 5%, what is the change in V_{CE}?



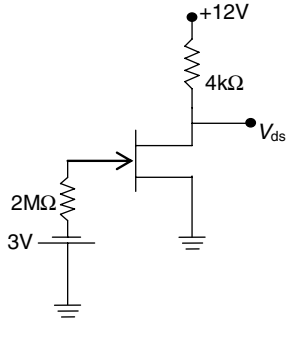
(A) increased by 4.57% (B) increased by 2.97%
(C) decreased by 4.57% (D) decreased by 2.97%

9. A Si transistor with $\beta = 50$ at 50°c is used, and it is desired that $V_{CE} = 8$ V. Consider I_{CO} varies from 0.5 to 10 μA when temperature changes from 50°c to 100°c.



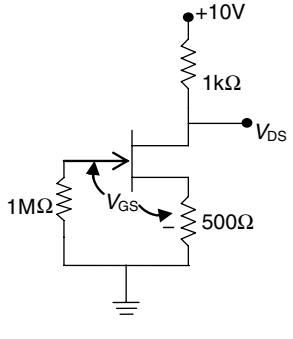
The values of R_B, stability factor, and I_c at 100°c are, respectively _____
(A) 200 kΩ, 51, 2.5 mA
(B) 20.5 kΩ, 50, 1 mA
(C) 200.5 kΩ, 16.7, 1.98 mA
(D) 2 kΩ, 10.4, 1.75 mA

10. Given $I_{DSS} = 6$ mA and $V_P = -4$ V for the given FET biasing Network, the value of V_{DS} is _____



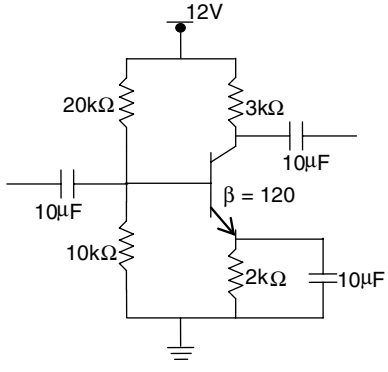
(A) 12V (B) 0V (C) 10.5V (D) 13.5V

11. A self-bias network with FET is given below; it has $I_D = 5$ mA



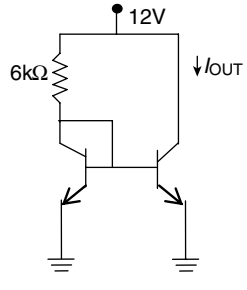
What are the values of V_{GS} and V_{DS}?
(A) −2.5 V, –2.5 (B) –2.5 V, 2.5 V
(C) −5 V, 0 V (D) 0 V, –5 V

12. For the given biasing network, calculate I_B and V_{CE} (assume $V_{BE} = 0.7$ V)



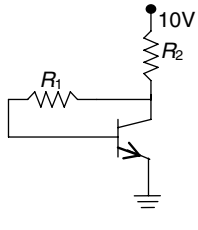
(A) 13.4μA, 3.95V (B) 13.4μA, 6V
(C) 1.34μA, 3.95V (D) 1.34μA, 6V

13. A constant current source using two matched N-P-N transistors with $\beta = 100$ and $V_{BE} = 0.6$ V is shown. Calculate I_{out}



(A) 1.5 mA (B) 0.2 mA
(C) 1.86 mA (D) 2 mA

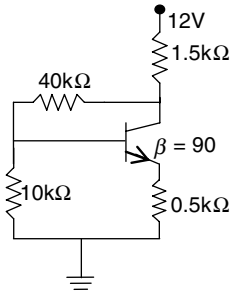
14. A transistor with $V_{BE} = 0.7$ V is shown. The values of R_1 and R_2 are such that the transistor is operating at $V_{CE} = 5$ V and $I_C = 2$ mA where $\beta = 100$. What is the operating point values for a transistor with $\beta = 200$.



(A) 3.78 V, 3.1 mA (B) 3.5 V, 2.6 mA
(C) 5 V, 2.5 mA (D) 3.5 V, 1.25 mA

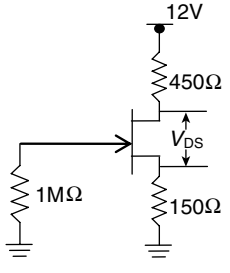
15. A transistor with $\beta = 100$ is used in CE mode. It is connected in collector to base bias mode with $\frac{R_B}{R_C} = 9$. Calculate the stability factor?
(A) 99 (B) 19.1 (C) 20.86 (D) 9.18

16. Calculate the stability factor for the given biasing network.



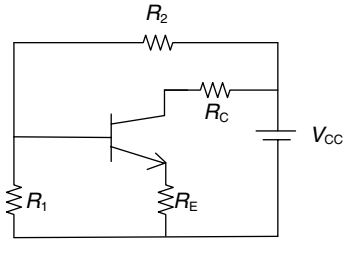
(A) 10 (B) 6.2 (C) 4.8 (D) 1

17. For a given FET-biasing network, $V_{DS} = \frac{1}{2} V_{DD}$, what are the values of I_D and V_{GS}?



(A) 1 mA, −1 V (B) 10 mA, −1 V
(C) 1 mA, −1.5 V (D) 10 mA, −1.5 V

18. The values of resistors R_C, R_E, respectively, for I_C = 5 mA, V_{CE} = 8 V, V_E = 6 V, and $S(I_{co})$ = 10, h_{fe} = 200, and V_{CC} = 20 V, are?



(A) 1.194 kW, 1.2 kΩ (B) 1.2 kW, 1.194 kΩ
(C) 10.3 kW, 17.43 kΩ (D) 2.1 kW, 4.12 kΩ

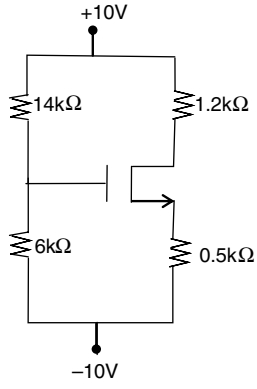
19. The values of resistors R_1 and R_2 in the above circuit are
(A) 17.2 kW, 32.86 kΩ (B) 12.8 kW, 23.6 kΩ
(C) 12.8 kW, 22.86 kΩ (D) 17.2 kW, 32.86 kΩ

20. A P-N-P transistor uses potential divider bias V_{BE} = −0.7 V, and β = 100, the operating point is to be at I_C = −1 mA, and V_{CE} = −5 V, V_{CC} = −20 V, voltage drop across R_E is −3 V, for SC(I_{co}) = 5, the value of R_C and R_E are
(A) 12 kΩ, 3 kΩ (B) 11.7 kΩ, 2.97 kΩ
(C) 11.7 kΩ, 3 kΩ (D) 12 kΩ, 2.97 kΩ

21. The values of R_1 and R_2 (bias resistances) in the above problem are?
(A) 4.2 kΩ, 12.4 kΩ (B) 64.4 kΩ, 15.35 kΩ
(C) 42 kΩ, 12 kΩ (D) 6.3 kΩ, 24 kΩ

Direction for questions 22 to 24:

22. In the current circuit, if the transistor parameters are V_{th} = 2 V, k_n = 60μA/v², $\frac{W}{L}$ = 60, and the transistor is in saturation, the value of V_{GS} is



(A) 3.62 V (B) −3.62 V
(C) 0.74 V (D) −0.74 V

23. The value of I_D is
(A) 12.5 mA (B) 9.2 mA
(C) 6.3 mA (D) 4.7 mA

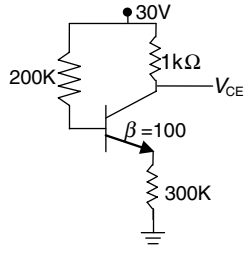
24. The value of V_{DS} is
(A) 12.95 V (B) 11.9 V (C) 9.3 V (D) 7.5 V

25. A BJT for which the manufacturer specifies $P_{D(max)}$ = 125 mw at 25°c free air temperature and max junction temperature is 150°c. The thermal resistance of BJT is _____.
(A) 5°c/w (B) 1°c/mw
(C) 1°c/w (D) 10°C/mW

Practice Problems 2

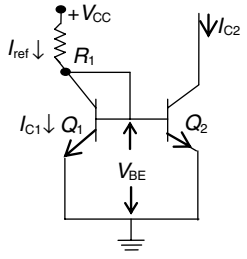
Direction for questions 1 to 18: Select the correct alternative from the given choices.

1. For the given biasing network, the collector to emitter voltage V_{CE} is _____ volt.



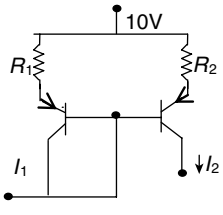
(A) '0' V (B) 30 V (C) 15.2 V (D) 13.1 V

2. A current mirror shown below, provide a 1.5mA current with V_{CC} = 12 V. Assume β = 150 and V_{BE} = 0.7volts. What is R_1?



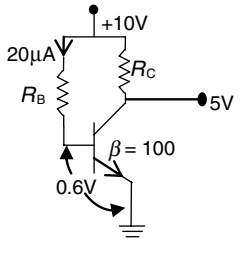
(A) 9.25 kΩ (B) 7.43 kΩ
(C) 7.53 kΩ (D) 8.5 kΩ

3. In the figure given, I_1 = 10 μA and I_2 = 40 μA. What is the ratio R_1/R_2.



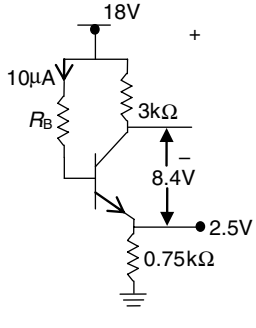
(A) 1 (B) 2 (C) $\frac{1}{2}$ (D) 4

4. In the given biasing network, the value of R_B and R_C are_____



(A) 470 kΩ, 2.5 kΩ (B) 2.5 kΩ, 470 kΩ
(C) 4.7 kΩ, 250 Ω (D) 470 kΩ, 25 kΩ

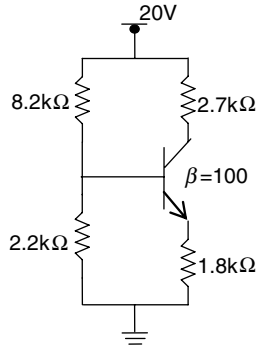
5. A transistor with emitter to base bias is given below.



The values β of transistor, the base resistance R_B are _____

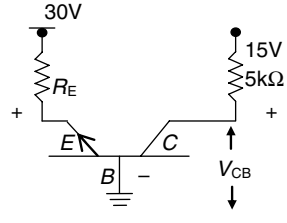
(A) 100, 155 kΩ (B) 166, 1.75 MΩ
(C) 333, 1.55 MΩ (D) 158, 1.8 MΩ

6. The self-bias network is given below. Its stability factor (S) is_____



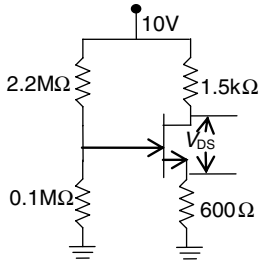
(A) 101 (B) 9.5 (C) 58 (D) 2

7. The value of R_E which will saturate the transistor is nearly _____ kΩ.



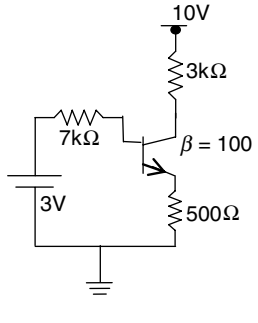
(A) 5 (B) 25 (C) 10 (D) 20

8. Calculate I_D and V_{GS} for V_{DS} = 2 V



(A) 4.6 mA, −1.85 V (B) 3.8 mA, −0.63 V
(C) 4.6 mA, −0.63 V (D) 3.8 mA, −1.85 V

9. Find the region of operation of transistor.

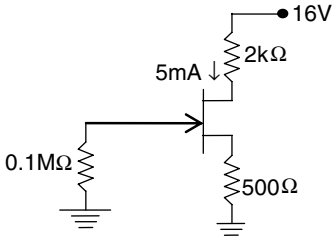


(A) saturation (B) active
(C) cut-off (D) none

10. A FET-biasing network is used with following specifications.

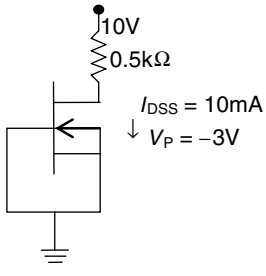
$V_P = 5$ V, $I_{DSS} = 8$ mA

Calculate g_m?



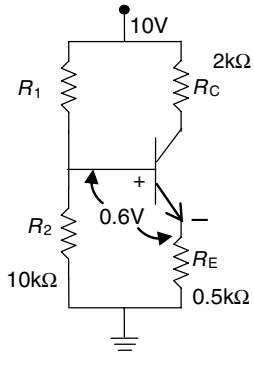
(A) 1.6 mS (B) 2 mS (C) 10 mS (D) 2.3 mS

11. The figure below shows a MOSFET-biasing network. Calculate V_{DS}.



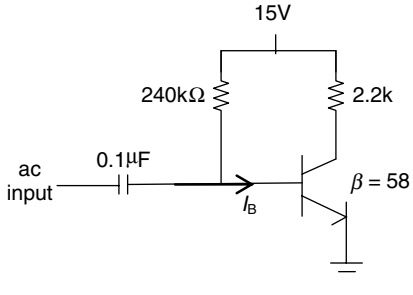
(A) 5 V (B) 10 V (C) 0 V (D) −5 V

12. A transistor with β is assumed to be very large is shown below. What is the value of R_1 required to make $I_C = 2.5$ mA.



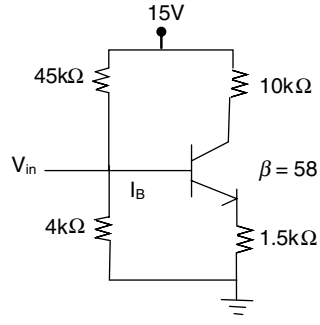
(A) 2 kΩ (B) 10k Ω (C) 44 kΩ (D) 54 kΩ

13. I_B for a given circuit is



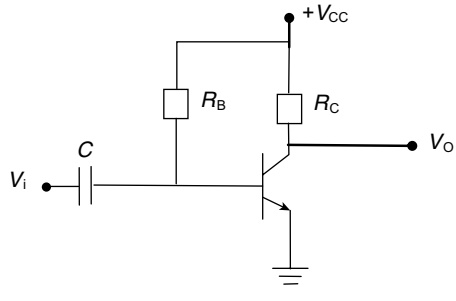
(A) 59.6 μA (B) 49 μA
(C) 62.5 μA (D) 68.1 μA

14. The equivalent base resistance of the given circuit is



(A) 49 kΩ (B) 45 kΩ
(C) 4 kΩ (D) 3.67 kΩ

15. The circuit shown in figure is that of a fixed bias circuit. Estimate the values of the collector load resistor R_c, and bias resistor R_B, If the quiescent collector current and voltage values are 10 mA and 5 V, respectively. The transistor has a dc current gain of 110. V_{BE} is 0.7 V, $V_{CC} = 12$ V.

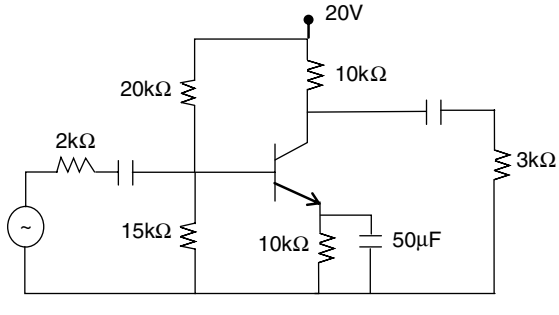


(A) 500 Ω, 103.7 kΩ (B) 500 Ω, 124.3 kΩ
(C) 700 Ω, 124.3 kΩ (D) 700 Ω, 103.7 kΩ

16. Calculate the thermal stability factor for the above circuit?

(A) 111 (B) 1 (C) 12 (D) 18

17. The circuit gives details for one stage of a transistor amplifier. Calculate the quiescent values of I_E, V_{CE}, $h_{fe} = 100$, $V_{BE} = 0$.



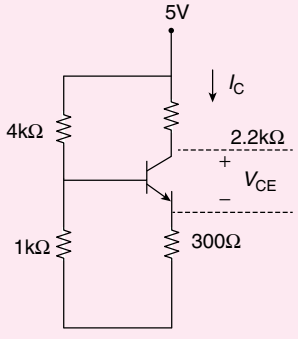
(A) 0.857 mA, 2.959 V (B) 1.23 mA, 5.67 V
(C) 1.11 mA, 7.69 V (D) −0.857 mA, 2.95 V

18. The thermal resistance of power transistor is 20°C/W. The ambient temperature is 40°C and junction temperature is 160 . If $V_{CE} = 4.2$ V, the maximum the collector can carry without destruction is _____.

(A) 1.2 A (B) 2.5 A (C) 1.66 A (D) 2 A

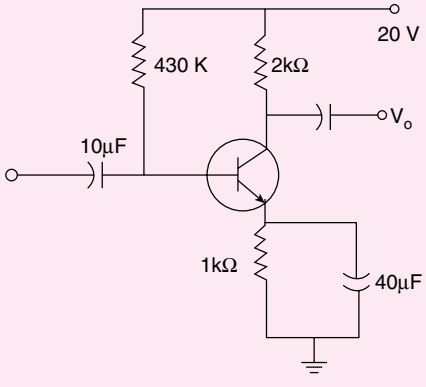
Previous Years' Questions

1. Assuming that the b of the transistor is extremely large and $V_{BE} = 0.7$ V, $I_{C,}$ and V_{CE} in the circuit shown in figure, are **[2004]**



(A) $I_C = 1$ mA, $V_{CE} = 4.7$ V
(B) $I_C = 0.5$ mA, $V_{CE} = 3.75$ V
(C) $I_C = 1$ mA, $V_{CE} = 2.5$ V
(D) $I_C = 0.5$ mA, $V_{CE} = 3.9$ V

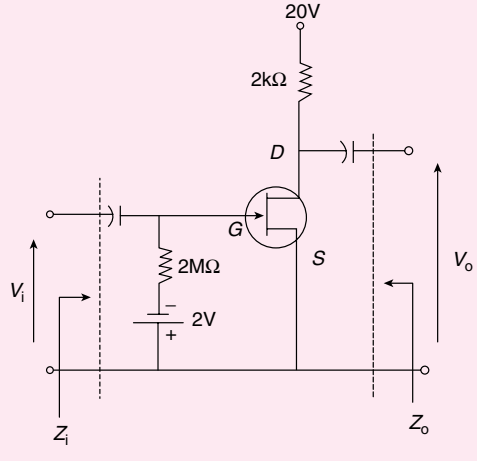
2. The circuit using a BJT with $\beta = 50$ and $V_{BE} = 0.7$ V is shown in figure. The base current I_B and collector voltage V_C are respectively. **[2005]**



(A) 43 μA and 11.4 volts (B) 40 μA and 16 volts
(C) 45 μA and 11 volts (D) 50 μA and 10 volts

Direction for questions 3 to 5:

Given $r_d = 20$ kΩ, $I_{DSS} = 10$ mA, $V_P = -8$ V.



3. Z_i and Z_0 of the circuit are respectively. **[2005]**

(A) 2 MΩ and 2 kΩ (B) 2 MΩ and $\frac{20}{11}$ kΩ
(C) Infinity and 2 kΩ (D) Infinity and $\frac{20}{11}$ kΩ

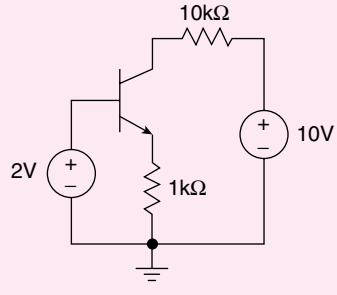
4. I_D and V_{DS} under DC conditions are respectively. **[2005]**

(A) 5.625 mA and 8.75 V
(B) 7.500 mA and 5.00 V
(C) 4.500 mA and 11.00 V
(D) 6.250 mA and 7.50 V

5. Transconductance in millisiemens (mS) and voltage gain of the amplifier are respectively. **[2005]**

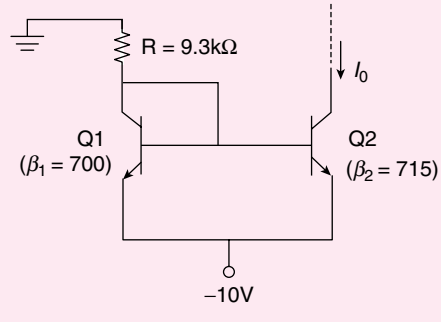
(A) 1.875 mS and 3.41
(B) 1.875 mS and –3.41
(C) 3.3 mS and –6
(D) 3.3 mS and 6

6. For the BJT circuit shown, assume that the β of the transistor is very large and $V_{BE} = 0.7$ V. the mode of operation of the BJT is: **[2007]**



(A) cut-off (B) saturation
(C) normal active (D) reverse active

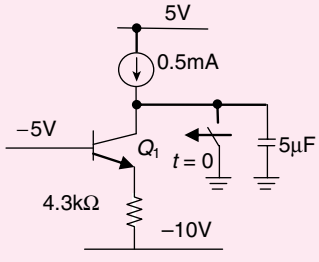
7. In the silicon BJT circuit shown below, assume that the emitter area of transistor Q_1 is half that of transistor Q_2. **[2010]**



The value of current I_0 is approximately
(A) 0.5 mA (B) 2 A
(C) 9.3 mA (D) 15 mA

8. For the BJT, Q_1 in the circuit shown as follows, $\beta = \infty$, $V_{BEon} = 0.7$ V, $V_{CEsat} = 0.7$ V. The switch is

initially closed. At time $t = 0$, the switch is opened. The time t at which Q_1 leaves the active region is **[2011]**

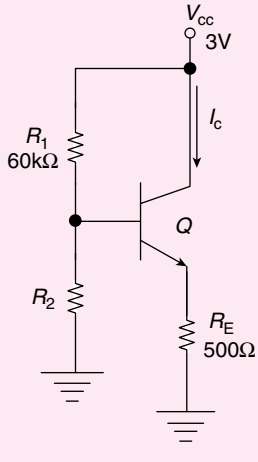


(A) 10 ms (B) 25 ms
(C) 50 ms (D) 100 ms

9. For a BJT, the common-base current gain $\alpha = 0.98$ and the collector base junction reverse bias saturation current $I_{CO} = 0.6$ μA. This BJT is connected in the common emitter mode and operated in the active region with a base drive current $I_B = 20$ μA. The collector current I_C for this mode of operation is **[2011]**

(A) 0.98 mA (B) 0.99 mA
(C) 1.0 mA (D) 1.01 mA

10. In the circuit shown below, the silicon npn transistor Q has a very high value of β. The required value of R_2 in kΩ to produce $I_C = 1$ mA is **[2013]**

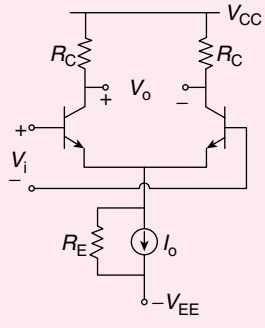


(A) 20 (B) 30 (C) 40 (D) 50

11. A good current buffer has **[2014]**

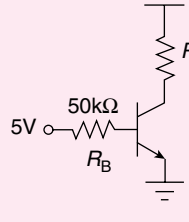
(A) low-input impedance and low-output impedance
(B) low-input impedance and high-output impedance
(C) high-input impedance and low-output impedance
(D) high-input impedance and high-output impedance

12. In the differential amplifier shown in the figure, the magnitudes of the common-mode and differential-mode gains are A_{cm} and A_d, respectively. If the resistance R_E is increased, then **[2014]**



(A) A_{cm} increases
(B) common-mode rejection ratio increases
(C) A_d increases
(D) common-mode rejection ratio decreases

13. In the circuit shown, the silicon BJT has $\beta = 50$. Assume $V_{BE} = 0.7$ V and $V_{CE(sat)} = 0.2$ V. Which one of the following statements is correct? **[2014]**



(A) For $R_C = 1$ kΩ, the BJT operates in the saturation region.
(B) For $R_C = 3$ kΩ, the BJT operates in the saturation region.
(C) For $R_C = 20$ kΩ, the BJT operates in the cut-off region.
(D) For $R_C = 20$ kΩ, the BJT operates in the linear region.

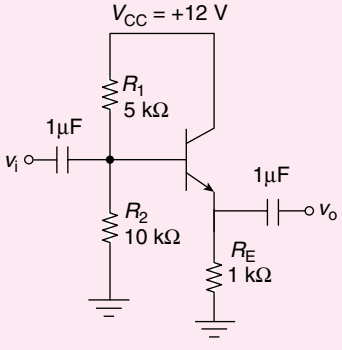
14. If the emitter resistance in a common-emitter voltage amplifier is not bypassed, it will **[2014]**

(A) reduce both the voltage gain and the input impedance.
(B) reduce the voltage gain and increase the input impedance.
(C) increase the voltage gain and reduce the input impedance.
(D) increase both the voltage gain and the input impedance.

15. A BJT in a common-base configuration is used to amplify a signal received by a 50 Ω antenna.

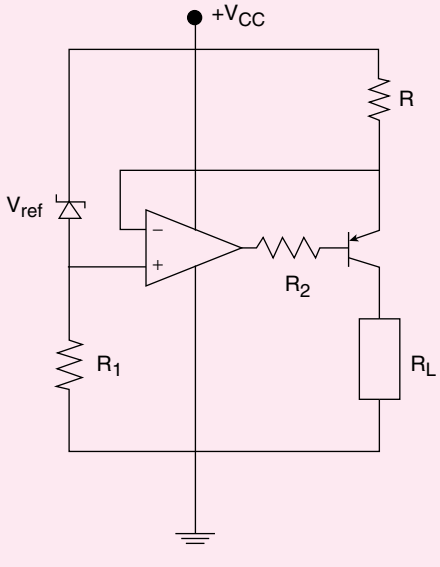
Assume $kT/q = 25$ mV. The value of the collector bias current (in mA) required to match the input impedance of the amplifier to the impedance of the antenna is _____. **[2014]**

16. For the common collector amplifier shown in the figure, the BJT has high β, negligible $V_{CE(sat)}$, and $V_{BE} = 0.7$ V. The maximum undistorted peak-to-peak output voltage v_o(in Volts) is _____ **[2014]**



17. The built-in potential of an abrupt *p-n* junction is 0.75 V. If its junction capacitance (C_J) at a reverse bias (V_R) of 1.25 V is 5 pF, the value C_J (in pF) when V_R = 7.25 V is _____. **[2015]**

18. Consider the constant current shown in the figure below. Let *b* represent the current gain of the transistor.

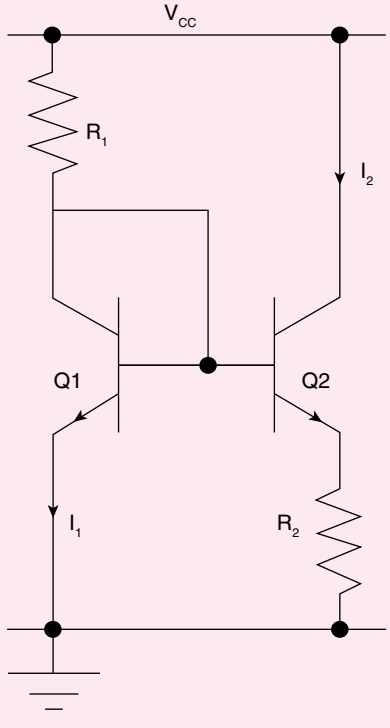


The load current I_0 through R_L is

(A) $I_0 = \left(\frac{\beta+1}{\beta}\right)\frac{V_{ref}}{R}$ (B) $I_0 = \left(\frac{\beta}{\beta+1}\right)\frac{V_{ref}}{R}$

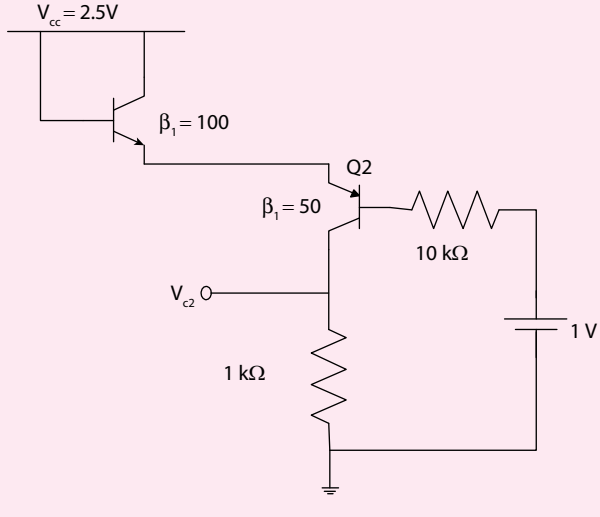
(C) $I_0 = \left(\frac{\beta+1}{\beta}\right)\frac{V_{ref}}{2R}$ (D) $I_0 = \left(\frac{\beta}{\beta+1}\right)\frac{V_{ref}}{2R}$

19. Resistor R_1 in the circuit below has been adjusted so that $I_1 = 1$ mA. The bipolar transistors Q1 and Q2 are perfectly matched and have very high current gain, so their base currents are negligible. The supply voltage V_{cc} is 6 V. The thermal voltage k T/q is 26 m V.



The value of R_2 (in Ω) for which I_2 = 100 μ A is _____.

20. Consider the circuit shown in the figure. Assuming $V_{BE1} = V_{EB2} = 0.7$ volt, the value of the dc voltage V_{c2} (in volt) is _____ .



Answer Keys

Exercises

Practice Problems 1

1. D	**2.** C	**3.** B	**4.** C	**5.** D	**6.** A	**7.** B	**8.** D	**9.** C	**10.** C
11. B	**12.** A	**13.** C	**14.** B	**15.** D	**16.** C	**17.** D	**18.** B	**19.** D	**20.** D
21. B	**22.** A	**23.** D	**24.** B	**25.** B					

Practice Problems 2

1. D	**2.** B	**3.** D	**4.** A	**5.** C	**6.** D	**7.** C	**8.** D	**9.** A	**10.** A
11. A	**12.** C	**13.** A	**14.** D	**15.** C	**16.** A	**17.** A	**18.** C		

Previous Years' Questions

1. C	**2.** B	**3.** B	**4.** A	**5.** B	**6.** B	**7.** B	**8.** C	**9.** D	**10.** C
11. B	**12.** B	**13.** B	**14.** B	**15.** 0.5	**16.** 9.4	**17.** 2.4 to 2.6		**18.** B	
19. 598 Ω		**20.** 0.5 V							