DIGITAL CIRCUITS TEST 3

Number of Questions: 25 **Time: 60 min.**

Directions for questions 1 to 25: Select the correct alternative from the given choices.

1. Assume the propagation delay time of 2 input gates as EXOR-20ns, AND – 10ns, *OR*-10ns, the propagation delay time for sum and carry output of a full adder circuit are respectively, when all the data inputs are applied simultaneously?
(A) 30ns, 20ns (B) 40ns, 30ns
(C) 40ns, 20ns (D) 20ns, 20ns

2. The minimized POS expression of the function $f(A, B, C, D) = AB + A\overline{C} + C + AD + A\overline{B}C + ABC$
(A) $A + \overline{C}$ (B) $\overline{A} + \overline{B}$
(C) AC (D) $A + C$

3. The signed two's complement representation of $(-783)_{10}$ is (in HEX)?
(A) 830FH (B) 04F1H
(C) FCF1H (D) F3F1H

4. The two numbers represented in signed 2's complement form are P = 11011101 and Q = 11100101, if Q is subtracted from P, the value obtained in signed 2's complement form is?
(A) 11110111 (B) 11000010
(C) 11111000 (D) 00000111

5. The subtraction of a binary number B from another binary number A, done by adding the 2's complement of B to A, results in a binary number without carry, this implies that the result is
(A) negative and is in normal form
(B) positive and is in normal form
(C) negative and is in 2's complement form
(D) positive and is in 2's complement form

6. $f(a, b, c) = ab + b^1c$ in the canonical POS form is represented as
(A) $(a + b + c)(a + b + c^1)(a + b^1 + c)(a^1 + b^1 + c)$
(B) $(a + b^1 + c)(a + b^1 + c^1)(a + b + c)(a^1 + b + c)$
(C) $(a + b + c)(a^1 + b^1 + c)(a + b^1 + c)$
(D) $(a^1 + b + c)(a^1 + b^1 + c)(a + b + c)(a + b^1 + c)$

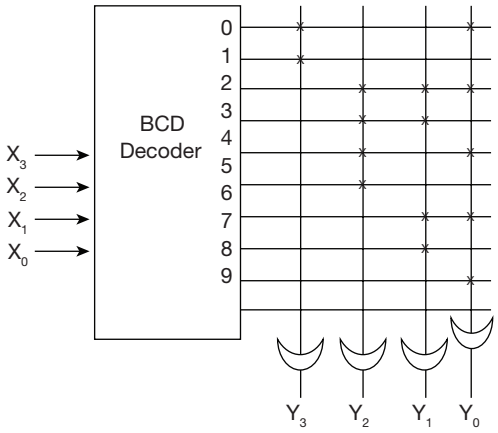
7. The Essential prime Implicants of the function $f(A, B, C, D) = \overline{A}C + ABD + \overline{A}B + \overline{B}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}D$ are
(A) $BD, \overline{B}\,\overline{D}, \overline{A}$ (B) $\overline{A}C, \overline{B}\,\overline{D}, B$
(C) $BD, \overline{A}C, \overline{B}$ (D) $\overline{A}\,\overline{B}, \overline{B}\,\overline{D}, C$

8. A combinational circuit has 3 inputs x, y, z and three outputs A, B, C. When the binary input is 4, 5, 6 and 7, the binary output is 2 less than the binary input. When the binary input is 0, 1, 2 and 3, the output is 4 more than the binary input the Boolean expression for output A and C respectively are?
(A) $x^1 y, z$ (B) $x + y^1, z^1$
(C) x, z (D) $x^1 + y, z$

9. In the above problem statement, how many number of *NOR* are gates required implement output B.
(A) 3 (B) 4
(C) 5 (D) 6

10. A combinational circuit takes 2 inputs and output is the 2's complement of input binary number. Consider the inputs as a and b and output as x and y, the equations of x and y respectively?
(A) $a \odot b, b$ (B) $a^1 b, a \odot b$
(C) $a^1 b, ab^1$ (D) $a \sum b, b$

11. If $X_3\ X_2\ X_1\ X_0$ are the inputs are $Y_3\ Y_2\ Y_1\ Y_0$ are the outputs for the following *PROM* circuit, then the output is?



(A) 2's complement of input
(B) 8's complement of input
(C) 9's complement of input
(D) 10's complement of input

12. To construct a 5 to 32 line decoder, how many number of 3 to 8 line decoders and 2 to 4 line decoders are required respectively without using any extra hardware?
(A) 3, 2 (B) 4, 1
(C) 2, 4 (D) 2, 2

13. Parity is a common error detection mechanism that is often used in data reception or retrieval systems. Consider a parity encoder that is used for data transmission or storage. If a word contains an even number of 1's, the parity bit is 0. If the word has odd number of 1's the parity bit is 1. If the data is w, x, y, z then the min terms for parity bit is?
(A) $\sum$m(1, 2, 4, 7, 8, 11, 13, 14)
(B) $\sum$m(0, 3, 5, 6, 9, 10, 12, 15)
(C) $\sum$m(0, 1, 3, 5, 8, 10, 13, 15)
(D) $\sum$m(1, 3, 5, 7, 9, 11, 13, 15)

14. Consider the Boolean functions
$f_1(A, B, C, D) = AC + BD$
$f_2(A, B, C, D) = \sum m(4, 5, 6, 7, 10, 11, 14, 15)$
Then find $f_1 + f_2$ in minimized *POS* form

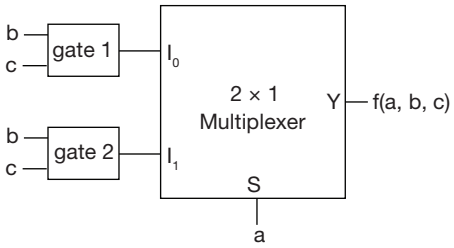
(A) $\left(\overline{A} + B\right)\left(B + D\right)\left(\overline{A} + \overline{B} + C\right)$

(B) $(A + B)\,(B + C)\left(\overline{A} + C + D\right)$

(C) $\left(A + \overline{B}\right)\left(B + D\right)\left(\overline{A} + C + D\right)$

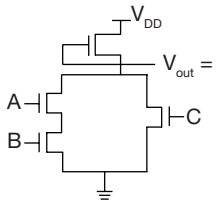
(D) $\left(A + D\right)\left(B + C\right)\left(\overline{A} + B + C\right)$

15. The Boolean function $f(a, b, c) = a^1\, b + b^1\, c + ac^1$ has to be implemented by the following 2 × 1 multiplexer then the gate 1 and gate 2 are respectively?



(A) *OR*, *NAND*
(B) *AND, OR*
(C) *NOR*, *AND*
(D) *NAND, OR*

16. Consider the NMOS circuit here, find the output

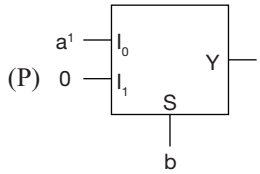


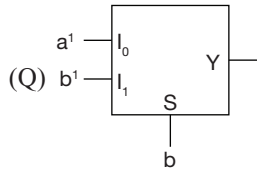
(A) $(A + B)C$
(B) $\overline{(A+B)C}$
(C) $AB + C$
(D) $\overline{AB+C}$

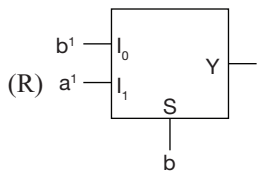
17. If the Boolean function $f(a, b, c, d) = a + b + c + d$ has to be implemented with only 2 input *NAND* gates, then how many *NAND* gates are required?

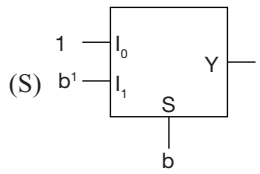
(A) 6
(B) 7
(C) 8
(D) 9

18. Which of the following multiplexer implements 2 input *NAND* gate?

(P)


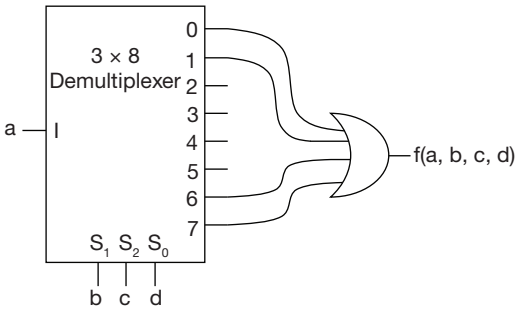
(Q)


(R)


(S)


(A) Q, R
(B) P, R
(C) P, S
(D) R, S

19. The output of the following Demultiplexer circuit is



(A) $a(b \odot c)$
(B) $a(b \odot c)$
(C) $(a \odot b)c$
(D) $(a \odot b)c$

20. For a 4 bit magnitude comparator with two inputs each of 4 bit $A(a_3, a_2, a_1, a_0)$ and $B(b_3, b_2, b_1\, b_0)$, the Boolean equation for $A < B$ is?

(A) $a_3^1\, b_3 + a_2^1\, b_2 + a_1^1\, b_1 + a_0^1\, b_0$

(B) $a_3\, b_3^1 + (a_3 \oplus b_3)\; a_2 b_2^1 + (a_3 \oplus b_3)\,(a_2 \oplus b_3)\; a_2 b_1^1 + (a_3 \oplus b_3)(a_2 \oplus b_2)\,(a_1 \oplus b_1)\; a_0 b_0^1$

(C) $a_3^1 b_3 + (a_3 \odot b_3)\; a_2^1\; b_2 + (a_3 \odot b_3)\,(a_2 \odot b_2)\; a_1^1\; b_1 + (a_3 \odot b_3)\,(a_2 \odot b_2)\,(a_1 \odot b_1)\; a_0^1\; b_0$

(D) $a_3^1\; b_3 + (a_3 \oplus b_3)\; a_2^1\; b_2 + (a_3 \oplus b_3)\; a_1^1\; b_1 + (a_3 \oplus b_3)(a_2 \oplus b_2)(a_1 \oplus b_1)\; a_0^1\, b_0$

21. For an open collector *TTL* gate has the specifications V_{OH} = 2.4 V, V_{OL} = 0.4V, I_{OH} = 250 μA, I_{OL} = 16mA, I_{IH} = 40 μA, I_{IL} = –1.6 mA
Find the fan out for *TTL* gate specified

(A) 6
(B) 8
(C) 10
(D) 16

22. An 8 × 1 multiplexer has inputs A, B, C connected to the selection inputs S_2, S_1 and S_0 respectively. The data inputs I_0 through I_7 are as follows. $I_1 = I_2 = 0$; $I_3 = I_5 = I_7 = 1$; $I_0 = I_4 = D$; and $I_6 = D^1$ then the Boolean function that the multiplexer implements is?

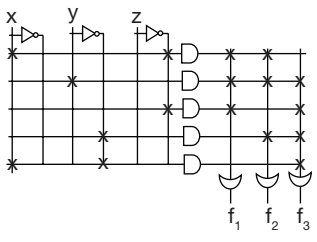
(A) $AB + BC + A\overline{C}\,D + \overline{B}\;\overline{C}\;D$

(B) $AC + BD + A\overline{B}\,D + B\,\overline{C}\;\overline{D}$

(C) $\overline{B}\overline{C}D + AB\overline{D} + BC + AC$

(D) $A\overline{B}\,D + \overline{B}\,\overline{C}\,D + A\overline{C} + BC$

23.



In the above *PLA* implementation the Boolean functions

(A) $f_1 = f_2$ (B) $f_1 = f_3$

(C) $f_2 = f_3$ (D) $f_1 \neq f_2 \neq f_3$

24. When a logic gate is driving another logic gate, the condition which must be satisfied for proper operation is

(A) $V_{OH} > V_{IH}$ and $V_{OL} > V_{IL}$

(B) $V_{OH} < V_{IH}$ and $V_{OL} > V_{IL}$

(C) $V_{OH} > V_{IH}$ and $V_{OL} < V_{IL}$

(D) $V_{OH} < V_{IH}$ and $V_{OL} < V_{IL}$

25. The minimized POS expression for *k*-map shown is

CD \ AB	00	01	11	10
00	0		0	X
01	X		X	X
11	0		0	0
10	0		0	0

(A) $\overline{A} + B$ (B) $\overline{A}\,B$

(C) $(\overline{A}+\overline{B})(\overline{A}+B)(A+B)$ (D) $\overline{A}(A+B)$

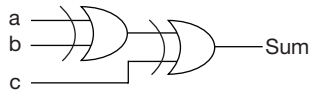
Answer Keys

1. B	**2.** D	**3.** C	**4.** C	**5.** C	**6.** B	**7.** A	**8.** D	**9.** C	**10.** D
11. C	**12.** B	**13.** A	**14.** B	**15.** A	**16.** D	**17.** D	**18.** D	**19.** B	**20.** C
21. A	**22.** C	**23.** C	**24.** C	**25.** B					

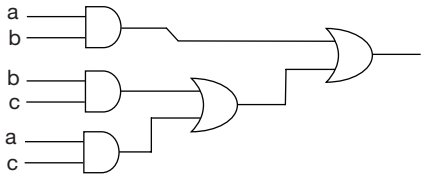
Hints and Explanations

1. Sum = $a \oplus b \oplus c$

Carry = $ab + bc + ac$



20 + 20 = 40 ns



10 + 10 + 10 = 30 ns

Two level exor gate for sum

So 20 + 20 = 40 ns

Carry will be implemented with 2 input gates in 3 levels, so 10 + 10 + 10 = 30 ns Choice (B)

2. $f = AB + A\overline{C} + C + AD + A\overline{B}\,C + ABC$

$= AB + A + C + AD + AC$

$= A(B + 1 + D + C) + C = A + C$ Choice (D)

3. 783 = 512 + 256 + 8 + 4 + 2 + 1 = 1100001111

+ 783 = 0000 0011 0000 1111 (add 0's to *MSB*)

– 783 = 1111 1100 1111 0001 (2's complement of +783)

In *HEX* ⇒ *FCF*1 Choice (C)

4. P = 11011101

00100011 (by taking 2's complement)

P = –35

Q = 11100101

00011011 (By taking 2's complement)

Q = –27

$P - Q$ = –35 – (–27) = –8 = 1111 1000 (in signed 2's complement form)

(or)

P = 1101 1101

Q = 1110 0101 (direct subtraction)

1111 1000 Choice (C)

5. $A - B$ has to be performed

So the 2's complement of B (which is $2^n - B$, n = no. of bits in B) is added to A

So result is $A + 2^n - B$; and there is no carry

$A + 2^n - B = 2^n - (A - B)$

So the result is negative and it is in 2's complement form. Choice (C)

6. $f(a, b, c) = ab + b^1.c$

$= (ab + b^1)(ab + c)$ $[x + yz = (x + y)(x + z)]$

$= (a + b^1)(a + c)(b + c)$

$= (a + b^1 + c.c^1)(a + b.b^1 + c)(a.a^1 + b + c)$

$= (a + b^1 + c)(a + b^1 + c^1)(a + b + c)(a + b^1 + c)$ $(a + b + c)$ $(a^1 + b + c)$

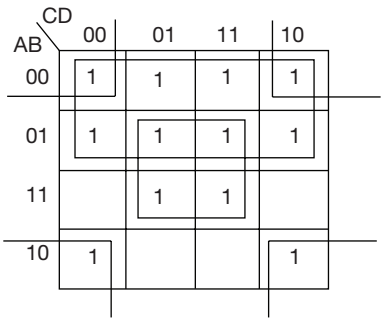
$= (a + b^1 + c)(a + b^1 + c^1)(a + b + c)(a^1 + b + c)$

Choice (B)

7. $f(A, B, C, D) = \overline{A}\,C + ABD + \overline{A}\,B + \overline{B}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}\,D$

Product term	Equivalent	Min terms
$\overline{A}$ C	0X1X	0010, 0011, 0110, 0111
ABD	11X1	1101, 1111
$\overline{A}B$	01XX	0100, 0101, 0110, 0111
$\overline{B}\,\overline{D}$	X0X0	0000, 0010, 1000, 1010
$\overline{A}\,\overline{B}\,\overline{C}\,D$	0001	0001

$f(A, B, C, D) = \sum m(0, 1, 2, 3, 4, 5, 6, 7, 8, 10, 13, 15)$



$f(A, B, C, D) = \overline{A} + BD + \overline{B}\,\overline{D}$

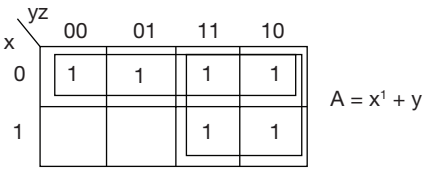
Essential prime implicants are $\overline{A}$, BD, $\overline{B}\,\overline{D}$

Choice (A)

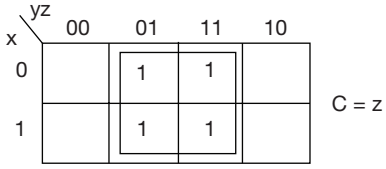
8. The truth table is

x	y	z	A	B	C	
0	0	0	1	0	0	output is 4 more than input
0	0	1	1	0	1	
0	1	0	1	1	0	
0	1	1	1	1	1	
1	0	0	0	1	0	output is 2 less than input
1	0	1	0	1	1	
1	1	0	1	0	0	
1	1	1	1	0	1	

$A(x, y, z) = \sum m(0, 1, 2, 3, 6, 7)$
$B(x, y, z) = \sum m(2, 3, 4, 5)$
$C(x, y, z) = \sum m(1, 3, 5, 7)$
The k map for A

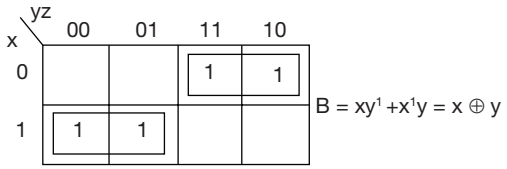


The k map for C



Choice (D)

9. $B(x, y, z) = \sum m(2, 3, 4, 5)$



2 input *XOR* required 5 *NOR* gates. Choice (C)

10. a, b are inputs of 2's complementer, and x, y are the outputs.
So truth table is

a	b	x	y
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	1

$x = a^1b + ab^1 = a \oplus b$
$y = b$ Choice (D)

11. From the circuit diagram, we can write truth table

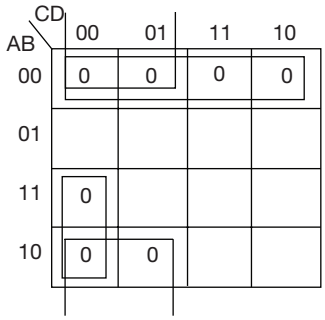
X_3	X_2	X_1	X_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	1	0	0	1
0	0	0	1	1	0	0	0
0	0	1	0	0	1	1	1
0	0	1	1	0	1	1	0
0	0	1	1	0	1	1	0
0	1	0	0	0	1	0	1

We can observe that output is 9's complement of input.
Choice (C)

12. 5 to 32 line decoder will have 32 output lines
So 4, 3 to 8 line Decoders are required, these 4 decoders will be selected by one 2 to 4 lines decoder.
So 4, 3 to 8 line decoder and 1, 2 to 4 line decoder (or)
5 to 32 line decoder will have 32 output lines
So 8, 2 to 4 line Decoders are required, to select one of these 8, one 3 to 8 line Decoder is required.
8, 2 to 4 Decoders, and 1, 3 to 8 Decoder. Choice (B)

13. For even number of 1's parity bit is 0.
So even parity,
Even parity can be implemented by *XOR* gate
XOR of even 1's given output 0.
XOR of add 1's gives output 1.
So parity bit $P = w \oplus x \oplus y \oplus z$
$P = \sum m(0001, 0010, 0100, 0111, 1000, 1011, 1101, 1110)$
$= \sum m(1, 2, 4, 7, 8, 11, 13, 14)$ Choice (A)

14. $f_1(A, B, C, D) = AC + BD$
$= AC(B + \overline{B})(C + \overline{C}) + (A + \overline{A})(C + \overline{C})BD$
$= \sum m(5, 7, 10, 11, 13, 14, 15)$
$= \Pi M(0, 1, 2, 3, 4, 6, 8, 9, 12)$
$f_2 = \sum m(4, 5, 6, 7, 10, 11, 14, 15)$
$= \Pi M(0, 1, 2, 3, 8, 9, 12, 13)$
$f_1 + f_2 = \Pi M(0, 1, 2, 3, 8, 9, 12)$
[common max terms of f_1 and f_2]



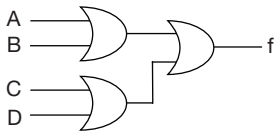
$f_1 + f_2 = (A + B)\,(B + C)\,(\overline{A} + C + D)$

Choice (B)

15. Given $f(a, b, c) = a^1b + b^1c + ac^1$
$= a^1b + (a + a^1)b^1c + ac^1$
$= a^1b + a^1b^1c + ab^1c + ac^1$
$= a^1[b + b^1c] + a[b^1c + c^1]$
$= a^1[b + c] + a[b^1 + c^1]$
By comparing this equation with output of 2 × 1 multiplexer
$Y = I_0\,\overline{S} + I_1\,S = I_0\,\overline{a} + I_1\,a = [b + c]a^1 + \overline{[bc]}\,a$
Gate 1 is OR gate, gate 2 is NAND gate. Choice (A)

16. For NMOS, when transistors are in series AND operation, transistors are in parallel OR operation overall output is in complement form.
$V_{out} = \overline{AB + C}$ Choice (D)

17.



Each 2 input OR gate required 3 – 2input NAND gates
So total 9 NAND gates are required. Choice (D)

18. For multiplexer P, $Y = I_0\,\overline{S} + I_1S = a^1\,b^1 + 0.b$
For mux, Q $Y = a^1\,b^1 + b^1.b = a^1\,b^1$
For mux, R, $Y = b^1.b^1 + a^1.b = a^1 + b^1 = (ab)^1$
For mux, S, $Y = 1.a^1 + b^1.a = a^1 + b^1 = (ab)^1$
So, R, S implement NAND gate P, Q implements *NOR* gate. Choice (D)

19. The demultiplexer output $Y_0 = I\,\overline{S_2}\,\overline{S_1}\,\overline{S_0}$

$Y_1 = I\,\overline{S_2}\,\overline{S_1}\,S_0$

$Y_2 = I\,\overline{S_2}\,S_1\,\overline{S_0}$

$Y_3 = I\,S_2\,\overline{S_1}\,\overline{S_0}$ …. Etc

$f(a, b, c, d) = Y_0 + Y_1 + Y_6 + Y_7$
$= ab^1c^1d^1 + ab^1c^1d + abcd^1 + abcd$
$= ab^1c^1 + abc = a[b \odot c]$ Choice (B)

20. If $A(a_3\,a_2\,a_1\,a_0)$ and $B(b_3\,b_2\,b_1\,b_0)$ are the two inputs the $A < B$ is possible only when the bits in A are 0 and the bits in B are 1. So we can check *MSB* by using $a_3^1b_3$, if the *MSB* bits are equal, then we check next bits $(a_3 \odot b_3)\;a_2^1\,b_2$ and if the higher order bits are equal then we move to next bits so $(A < B) = a_3^1\,b_3 + (a_3 \odot b_3)\;a_2^1b_2 + (a_3 \odot b_3)\,(a_2 \odot b_2)\;a_1^1b_1 + (a_3 \odot b_3)(a_2 \odot b_2)(a_1 \odot b_1)\;a_0^1\;b_0$. Choice (C)

21. Fan out (logic 1) $= n_1 = \dfrac{I_{OH}}{I_{IH}}$

$= \dfrac{250\mu A}{40\mu A} = 6.25$

Fanout (logic 0) $n_0 = \dfrac{I_{OL}}{I_{IL}} = \dfrac{16\,mA}{1.6\,mA} = 10$

The overall fanout = $\min(n_1, n_0) = 6$ Choice (A)

22. For 8 × 1 multiplexer output
$Y = I_0\,\overline{S_2}\,\overline{S_1}\,\overline{S_0} + I_1\,\overline{S_2}\,\overline{S_1}\,S_0 + I_2\,\overline{S_2}\,S_1\,\overline{S_0} + I_3\,\overline{S_2}\,S_1\,S_0 +$
$I_4\,S_2\,\overline{S_1}\,\overline{S_0} + I_5\,S_2\,\overline{S_1}\,S_0 + I_6\,S_2\,S_1\,\overline{S_0} + I_7\,S_2\,S_1\,S_0$
$= \overline{A}\,\overline{B}\,\overline{C}\,D + 0 + 0 + \overline{A}\,BC + A\overline{B}\,\overline{C}\,D + A\,\overline{B}\,C +$
$AB\overline{C}\,\overline{D} + ABC$

AB \ CD	00	01	11	10
00		1		
01			1	1
11	1		1	1
10		1	1	1

$= \sum m(1, 6, 7, 9, 10, 11, 12, 14, 15)$
$Y = \overline{B}\,\overline{C}\,D + AB\overline{D} + BC + AC$ Choice (C)

23. The product terms are xz^1, x^1y, yz^1, y^1z, xy^1
So $f_1 = xz^1 + x^1y + yz^1 = xz^1 + x^1y$ [consensus theorem]
$= \sum m(2, 3, 4, 6)$
$f_2 = xz^1 + x^1y + y^1z = \sum m(1, 2, 3, 4, 5, 6)$
$f_3 = x^1y + yz^1 + y^1z + xy1 = \sum m(1, 2, 3, 4, 5, 6)$
So $f_2 = f_3$ Choice (C)

24. Choice (C)

25. Two octates present so minimized expression is $\overline{A}\,.B$

CD \ AB	00	01	11	10
00	0		X	X
01	X		X	X
11	0		0	0
10	0		0	0

Choice (B)