CHAPTER

3.3

BASIC FET CIRCUITS

Statement for Q.1–3:

In the circuit shown in fig. P3.3.1–3 the transistor parameters are as follows:

Threshold voltage $V_{TN} = 2$ V

Conduction parameter $K_n = 0.5$ mA / V^2

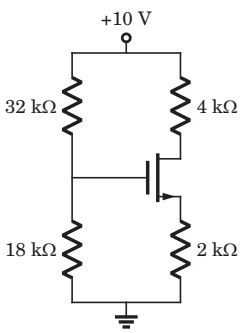

Fig. P3.3.1–3

1. $V_{GS} = ?$

(A) 2.05 V (B) 6.43 V

(C) 4.86 V (D) 3.91 V

2. $I_D = ?$

(A) 1.863 mA (B) 1.485 mA

(C) 0.775 mA (D) None of the above

3. $V_{DS} = ?$

(A) 4.59 V (B) 3.43 V

(C) 5.35 V (D) 6.48 V

Statement for Q.4–6:

In the circuit shown in fig. P3.3.4–6 the transistor parameter are as follows:

$$V_{TN} = 2 \text{ V}, \quad k_n' = 60 \ \mu\text{A} / \text{V}^2, \quad \frac{W}{L} = 60$$

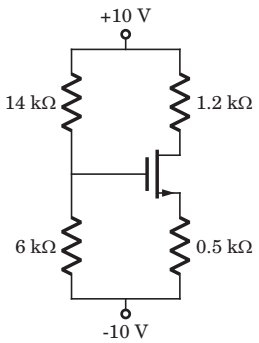

Fig. P3.3.4–6

4. $V_{GS} = ?$

(A) –3.62 V (B) 3.62 V

(C) –0.74 V (D) 0.74 V

5. $I_D = ?$

(A) 13.5 mA (B) 10 mA

(C) 19.24 mA (D) 4.76 mA

6. $V_{DS} = ?$

(A) 2.95 V (B) 11.9 V

(C) 3 V (D) 12.7 V

16. The parameter of the transistor in fig. P3.3.16 are $V_{TN} = 1.2$ V, $K_n = 0.5$ mA / V^2 and $\lambda = 0$. The voltage V_{DS} is

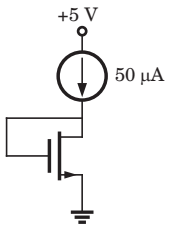

Fig. P3.3.16

(A) 1.69 V (B) 1.52 V

(C) 1.84 V (D) 0

17. The parameter of the transistor in fig. P3.3.17 are $V_{TN} = 0.6$ V and $K_n = 0.2$ mA / V^2. The voltage V_S is

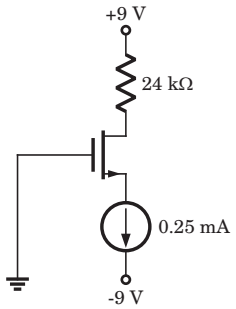

Fig. P3.3.17

(A) 1.72 V (B) –1.72 V

(C) 7.28 V (D) –7.28 V

18. In the circuit of fig. P3.3.18 the transistor parameters are $V_{TN} = 1.7$ V and $K_n = 0.4$ mA / V^2.

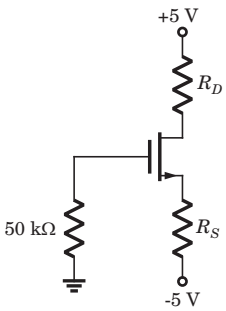

Fig. P3.3.18

If $I_D = 0.8$ mA and $V_D = 1$ V, then value of resistor R_S and R_D are respectively

(A) 2.36 kΩ, 5 kΩ (B) 5 kΩ, 2.36 kΩ

(C) 6.43 kΩ, 8.4 kΩ (D) 8.4 kΩ, 6.43 kΩ

19. In the circuit of fig. P.3.3.19 the PMOS transistor has parameter $V_{TP} = -1.5$ V, $k'_p = 25$ μA / V^2, $L = 4$ μm and $\lambda = 0$. If $I_D = 0.1$ mA and $V_{SD} = 2.5$ V, then value of W will be

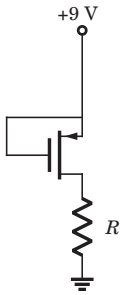

Fig. P3.3.19

(A) 15 μm (B) 1.6 μm

(C) 32 μm (D) 3.2 μm

20. The PMOS transistor in fig. P3.3.20 has parameters

$$V_{TP} = -1.2 \text{ V}, \quad \frac{W}{L} = 20, \text{ and } k'_p = 30 \text{ μA / V}^2.$$

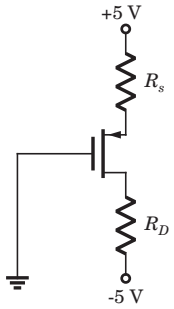

Fig. P3.3.20

If $I_D = 0.5$ mA and $V_D = -3$ V, then value of R_S and R_D are

(A) 4 kΩ, 5.8 kΩ (B) 4 kΩ, 5 kΩ

(C) 5.8 kΩ, 4 kΩ (D) 5 kΩ, 4 kΩ

21. The parameters for the transistor in circuit of fig. P3.3.21 are $V_{TN} = 2$ V and $K_n = 0.2$ mA / V^2. The power dissipated in the transistor is

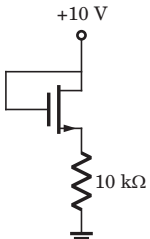

Fig. P3.3.21

(A) 5.84 mW (B) 2.34 mW

(C) 0.26 mW (D) 58.4 mW

Statement for Q.22–23:

Consider the circuit shown in fig. P3.2.22–33.

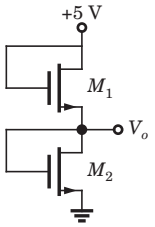

Fig. P3.3.22-23

The both transistor have parameter as follows

$$V_{TN} = 0.8 \text{ V}, \quad k_n' = 30 \ \mu\text{A} / \text{V}^2$$

22. If the width-to-length ratios of M_1 and M_2 are

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 40$$

The output V_o is

(A) –2.5 V (B) 2.5 V

(C) 5 V (D) 0 V

23. If the ratio is $\left(\frac{W}{L}\right)_1 = 40$ and $\left(\frac{W}{L}\right)_2 = 15$, then V_o is

(A) 2.91 V (B) 2.09 V

(C) 3.41 V (D) 1.59 V

24. In the circuit of fig. P3.324. the transistor parameters are $V_{TN} = 1$ V and $k_n' = 36 \ \mu\text{A} / \text{V}^2$. If $I_D = 0.5$ mA, $V_1 = 5$ V and $V_2 = 2$ V then the width to-length ratio required in each transistor is

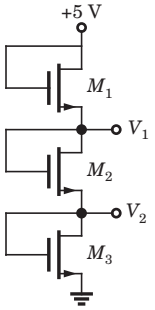

Fig. P3.3.24

	$\left(\frac{W}{L}\right)_1$	$\left(\frac{W}{L}\right)_2$	$\left(\frac{W}{L}\right)_3$
(A)	1.75	6.94	27.8
(B)	4.93	10.56	50.43
(C)	35.5	22.4	8.53
(D)	56.4	38.21	12.56

25. The transistors in the circuit of fig. P3.3.25 have parameter $V_{TN} = 0.8$ V, $k_n' = 40 \ \mu\text{A} / \text{V}^2$ and $\lambda = 0$. The width-to-length ratio of M_2 is $\left(\frac{W}{L}\right)_2 = 1$. If $V_o = 0.10$ V when $V_i = 5$ V, then $\left(\frac{W}{L}\right)_1$ for M_1 is

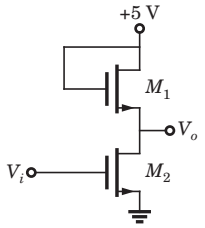

Fig. P3.3.25

(A) 47.5 (B) 28.4

(C) 40.5 (D) 20.3

Statement for Q.26–27:

All transistors in the circuit in fig. P3.3.26–27 have parameter $V_{TN} = 1$ V and $\lambda = 0$.

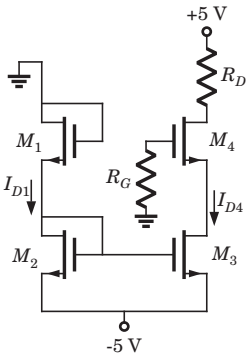

Fig. P3.3.26–27

The conduction parameter are as follows:

$$K_{n1} = 400 \ \mu\text{A} / \text{V}^2$$

$$K_{n2} = 200 \ \mu\text{A} / \text{V}^2$$

$$K_{n3} = 100 \ \mu\text{A} / \text{V}^2$$

$$K_{n4} = 80 \ \mu\text{A} / \text{V}^2$$

26. $I_{D1} = ?$

(A) 0.23 mA (B) 0.62 mA

(C) 0.46 mA (D) 0.31 mA

27. $I_{D4} = ?$

(A) 0.62 mA (B) 0.31 mA

(C) 0.46 mA (D) 0.92 mA

28. For the circuit in fig. P3.3.28 the transistor parameter are $V_{TN} = 0.8$ V and $k'_n = 30\ \mu A / V^2$. If output voltage is $V_o = 0.1$ V, when input voltage is $V_i = 4.2$ V, the required transistor width-to length ratio is

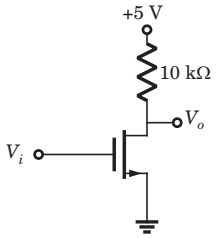

Fig. P3.3.28

(A) 1.568 (B) 0.986

(C) 0.731 (D) 1.843

29. For the transistor in fig. P3.3.29 parameters are $V_{TN} = 1$ V and $K_n = 12.5\ \mu A / V^2$. The Q-point (I_D, V_{DS}) is

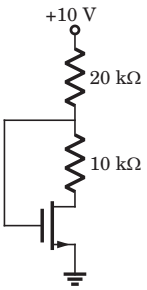

Fig. P3.3.29.

(A) (1 mA, 8 V) (B) (0.2 mA, 4 V)

(C) (1.17 mA, 8 V) (D) (0.23 mA, 3.1V)

30. For an *n*-channel JFET, the parameters are $I_{DSS} = 6$ mA and $V_P = -3$ V. If $V_{DS} > V_{DS(sat)}$ and $V_{GS} = -2$ V, then I_D is

(A) 16.67 mA (B) 0.67 mA

(C) 5.55 mA (D) 1.67 mA

31. For the circuit in fig. P3.3.32 the transistor parameters are $V_p = -3.5$ V, $I_{DSS} = 18$ mA, and $\lambda = 0$. The value of V_{DS} is

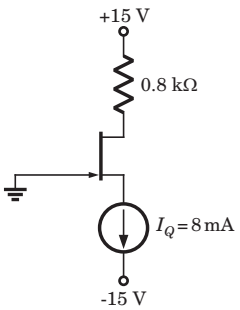

Fig. P3.3.32

(A) 7.43 V (B) 8.6 V

(C) –1.17 V (D) 1.17 V

32. A *p*-channel JFET biased in the saturation region with $V_{SD} = 5$ V has a drain current of $I_D = 2.8$ mA, and $I_D = 0.3$ mA at $V_{GS} = 3$ V. The value of I_{DSS} is

(A) 10 mA (B) 5 mA

(C) 7 mA (D) 2 mA

Statement for Q.33–34:

For the p-channel transistor in the circuit of fig. P3.3.33–34 the parameters are $I_{DSS} = 6$ mA, $V_P = 4$ V and $\lambda = 0$.

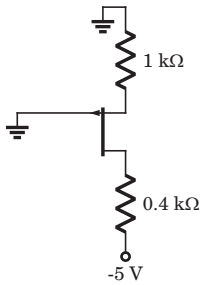

Fig. P3.3.33–34

33. The value of I_{DQ} is

(A) 8.86 mA (B) 6.39 mA

(C) 4.32 mA (D) 1.81 mA

34. The value of V_{SD} is

(A) –4.28 V (B) 2.47 V

(C) 4.28 V (D) 2.19 V

35. The transistor in the circuit of fig. P3.3.35 has parameters $I_{DSS} = 8$ mA and $V_P = -4$ V. The value of V_{DSQ} is

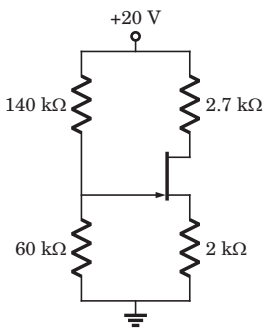

Fig. P3.3.35

(A) 2.7 V (B) 2.85 V

(C) –1.30 V (D) 1.30 V

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SOLUTIONS

1. (A) $R_1 = 32\ \text{k}\Omega, \quad R_2 = 18\ \text{k}\Omega, \quad V_{DD} = 10\ \text{V}$

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} = \left(\frac{18}{18 + 32}\right) 10 = 3.6\ \text{V}$$

Assume that transistor in saturation region

$$I_D = \frac{V_S}{R_S} = \frac{V_G - V_{GS}}{R_S} = K_n (V_{GS} - V_{TN})^2$$

$R_S = 2\ \text{k}\Omega, \quad K_n = 0.5\ \text{mA / V}^2$

$3.6 - V_{GS} = (2)(0.5)(V_{GS} - 0.8)^2 \quad \Rightarrow \quad V_{GS} = 2.05\ \text{V}$

2. (C) $I_D = \dfrac{V_G - V_{GS}}{R_S} = \dfrac{3.6 - 2.05}{2\text{k}} = 0.775\ \text{mA}$

3. (C) $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 10 - 0.775(4 + 2) = 5.35\ \text{V}$

$V_{DS(sat)} = V_{GS} - V_{TN} = (2.05 - 0.8) = 1.25\ \text{V}$

$V_{DS} > V_{DS(sat)}$ as assumed.

4. (B) $R_1 = 14\ \text{k}\Omega, \ R_2 = 6\ \text{k}\Omega, \ R_S = 0.5\ \text{k}\Omega, \ R_D = 1.2\ \text{k}\Omega$

$$V_G = \left(\frac{R_L}{R_1 + R_2}\right)(20) - 10 = \left(\frac{6}{14 + 6}\right)(20) - 10 = -4\ \text{V}$$

Assume transistor in saturation

$$I_D = \frac{V_S - (-10)}{R_S} = \frac{V_G - V_{GS} + 10}{R_S} = K_n (V_{GS} - V_{TN})^2$$

$$K_n = \frac{k'_n}{2}\frac{W}{L} = \frac{(60)(60 \times 10^{-6})}{2} = 1.8\ \text{mA / V}^2$$

$\Rightarrow \quad -4 - V_{GS} + 10 = (0.5)(1.8)(V_{GS} - 2)^2$

$\Rightarrow \quad V_{GS} = 3.62, \ -0.74\ \text{V}, \ V_{GS}$ will be positive.

5. (D) $I_D = \dfrac{V_G - V_{GS} + 10}{R_S} = \dfrac{-4 - 3.62 + 10}{0.5\text{k}} = 4.76\ \text{mA}$

6. (B) $10 = I_D(R_S + R_D) + V_{DS} - 10$

$V_{DS} = 20 - 4.76(1.2 + 0.5) = 11.9\ \text{V}$

$V_{DS(sat)} = V_{GS} - V_{TN} = 3.62 - 2 = 1.62\ \text{V}$

$V_{DS} = 11.9\ \text{V} > V_{DS(sat)}$, Assumption is correct.

7. (B) $R_1 = 8\ \text{k}\Omega, \ R_L = 22\ \text{k}\Omega, \ R_S = 0.5\ \text{k}\Omega, \ R_D = 2\ \text{k}\Omega$

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right)(20) - 10 = \left(\frac{22}{8 + 22}\right)(20) - 10 = 4.67\ \text{V}$$

Assume transistor in saturation

$$I_D = \frac{10 - V_S}{R_S} = K_P (V_{SG} + V_{TP})^2$$

$V_S = V_G + V_{SG}$

$10 - (4.67 + V_{SG}) = (0.5)(1)(V_{GS})$

$\Rightarrow \quad V_{SG} = 3.77\ \text{V}, \ -1.77\ \text{V}, \ V_{SG}$ is positive voltage.

8. (A) $I_D = \dfrac{10 - V_S}{R_S} = \dfrac{10 - (V_G + V_{GS})}{R_S}$

$$= \frac{10 - (4.67 + 3.77)}{0.5} = 3.12\ \text{mA}$$

9. (C) $10 = I_D(R_S + R_D) + V_{SD} - 10$

$V_{SD} = 20 - I_D(R_S + R_D) = 20 - 2.12(2 + 0.5) = 12.2\ \text{V}$

10. (C) Assume transistor in saturation.

$I_D = 0.4\ \text{mA}, \quad 0.4 = K_P (V_{GS} + V_{TP})^2$

$0.4 = (0.2)(V_{SG} - 0.8)^2 \quad \Rightarrow \quad V_{SG} = \sqrt{2} + 0.8 = 2.21\ \text{V}$

$V_G = 0, \quad V_{SG} = V_S - V_G = V_S$

11. (A) $V_D = I_D R_D - 5 = (0.4)(5) - 5 = -3\ \text{V}$

$V_{SD} = V_S - V_D = 2.21 - (-3) = 5.21\ \text{V}$

12. (C) $R_1 = 14.5\ \text{k}\Omega, \quad R_2 = 5.5\ \text{k}\Omega,$

$R_S = 0.6\ \text{k}\Omega, \ R_D = 0.8\ \text{k}\Omega,$

$$V_G = \left(\frac{R_L}{R_1 + R_2}\right)(10) - 5 = \left(\frac{5.5}{14.5 + 5.5}\right)(10) - 5 = -2.25\ \text{V}$$

Assume transistor in saturation.

$$I_D = \frac{V_S - (-5)}{R_S} = K_n (V_{GS} - V_{TN})^2$$

$V_S = V_G - V_{GS}$

$-2.25 - V_{GS} + 5 = (0.6)(0.5)(V_{GS} - (-1))^2$

$\Rightarrow \quad V_{GS} = 1.24, -6.58\ \text{V}$

V_{GS} is positive. Thus (D) is correct option.

13. (D) $I_D = \dfrac{V_S + 5}{R_S} = \dfrac{V_G - V_{GS} + 5}{R_S} = \dfrac{-2.25 - 1.24 + 5}{0.6\text{k}}$

$= 2.52\ \text{mA}$, Therefore (D) is correct option.

14. (B) $5 = I_D(R_S + R_D) + V_{DS} - 5$

$V_{DS} = 10 - I_D(R_S + R_D) = 10 - 2.52(0.8 + 0.6) = 6.47\ \text{V}$

$V_{DS(sat)} = V_{GS} - V_{TH} = 1.24 - (-1) = 2.24$

$V_{DS} > V_{DS(sat)}$,Assumption is correct.

15. (B) $I_S = 50\ \mu\text{A} = I_D \ , I_D = K_n (V_{GS} - V_{TN})^2$

$\Rightarrow \quad 50 \times 10^{-6} = 0.5 \times 10^{-3}(V_{GS} - 1.2)^2 \quad \Rightarrow \quad V_{GS} = 1.516\ \text{V},$

$V_G = 0, \ V_S = V_G - V_{GS} = -1.516\ \text{V}$

$V_{DS} = V_D - V_S = 5 - (-1.516) = 6.516\ \text{V}$

16. (B) $I_D = 50\mu = K_n (V_{GS} - V_{TN})^2$

$\Rightarrow \quad 50 \times 10^{-6} = 0.5 \times 10^{-3}(V_{GS} - 1.2)^2$

$V_{GS} = 1.52$ V, $V_{GS} = V_{DS}$

17. (B) $I_D = K_n(V_{GS} - V_{TN})^2$

$\Rightarrow \quad 0.25 = 0.2(V_{GS} - 0.6)^2 \quad \Rightarrow \quad V_{GS} = 1.72$ V,

$V_{GS} = V_G - V_S, \quad V_G = 0, \quad V_S = -1.72$ V

18. (A) $I_D = \dfrac{5 - V_D}{R_D} = 0.8$ mA, $\quad R_D = \dfrac{6-1}{0.8\text{m}} = 5$ kΩ

$I_D = K_n\,(V_{GS} - V_{TN})^2$

$\Rightarrow \quad 0.8 = (0.4)(V_{GS} - 1.7)^2 \quad \Rightarrow \quad V_{GS} = 3.11$ V

$V_{GS} = V_G - V_S\ , \quad V_G = 0, \quad V_S = -3.11$ V

$I_D = 0.8\text{ mA} = \dfrac{-3.11 - (-5)}{R_S} \quad \Rightarrow \quad R_S = 2.36$ kΩ

19. (C) $V_{SD} = V_{SG}, \quad I_D = \dfrac{k_p'}{2}\dfrac{W}{L}(V_{GS} + V_{TP})^2$

$10^{-4} = \left(\dfrac{25}{2}\right)\left(\dfrac{W}{4}\right)(2.5 - 1.5)^2 \quad \Rightarrow \quad W = 32\ \mu\text{m}$

20. (D) $K_p = \left(\dfrac{30 \times 10^{-6}}{2}\right)(20) = 0.3\text{ mA / V}^2$

$I_D = K_p(V_{SG} + V_{TP})^2 \quad \Rightarrow \quad 0.5 = 0.3(V_{SG} - 1.2)^2$

$\Rightarrow \quad V_{SG} = 2.49$ V, $V_G = 0$

$V_S = V_{SG} = 2.49$ V

$I_D = \dfrac{5 - V_S}{R_S} \quad \Rightarrow \quad R_S = \dfrac{5 - 2.49}{0.5\text{m}} = 5.02$ kΩ

$I_D = \dfrac{V_D - (-5)}{R_D} \quad \Rightarrow R_D = \dfrac{-3 + 5}{0.5\text{m}} = 4$ kΩ

21. (B) Assume transistor in saturation

$I_D = \dfrac{10 - V_{GS}}{10\text{k}} = K_n(V_{GS} - V_{TN})^2$

$10 - V_{GS} = (10)(0.2)(V_{GS} - 2)^2$

$\Rightarrow \quad V_{GS} = 3.77$ V, -0.27 V, V_{GS} will be 3.77 V

$V_{GS} = V_{DS} = 3.77$ V

$I_D = \dfrac{10 - 3.77}{10\text{k}} = 0.623$ mA

Power $= I_D V_{DS} = 2.35$ mW

$V_{DS} > V_{GS} - V_{TN}$ assumption is correct.

22. (B) For both transistor $V_{DS} = V_{GS}$,

$V_{DS} > V_{GS} - V_{TN}$ Therefore both transistor are in saturation.

$I_{D1} = I_{D2} \quad \Rightarrow \quad K_{n1}(V_{GS1} - V_{TN1})^2 = K_{n2}(V_{GS2} - V_{TN2})^2$

$K_{n1} = K_{n2}\ , \quad V_{TN1} = V_{TN2}$

$V_{GS1} = V_{GS2} = \dfrac{5}{2}$ V

$V_o = V_{GS2} = 2.5$ V

23. (A) $\left(\dfrac{W}{L}\right)_1 > \left(\dfrac{W}{L}\right)_2$ thus $V_{GS1} < V_{GS2}$

$40(V_{GS1} - 0.8)^2 = 15(V_{GS2} - 0.8)^2$

$V_{GS2} = 5 - V_{GS1}$

$1.63(V_{GS1} - 0.8) = (5 - V_{GS1} - 0.8)$

$V_{GS1} = 2.09,\ V_{GS2} = 2.91$ V, $\quad V_o = V_{GS2} = 2.91$ V

24. (A) Each transistor is biased in saturation because

$V_{DS} = V_{GS}$ and $V_{DS} > V_{GS} - V_{TN}$

For M_3, $V_2 = 2$ V $= V_{GS3}$

$I_D = 0.5 = \left(\dfrac{36 \times 10^{-3}}{2}\right)\left(\dfrac{W}{L}\right)_3 (2 - 1)^2 \quad \Rightarrow \quad \left(\dfrac{W}{L}\right)_3 = 27.8$

For M_2, $V_{GS2} = V_1 - V_2 = 5 - 2 = 3$ V

$I_D = 0.5 = \left(\dfrac{36 \times 10^{-3}}{2}\right)\left(\dfrac{W}{L}\right)_2 (3 - 1)^2 \quad \Rightarrow \quad \left(\dfrac{W}{L}\right)_2 = 6.94$

For M_1, $V_{GS1} = 10 - V_1 = 10 - 5 = 5$ V

$I_D = 0.5 = \left(\dfrac{36}{2} \times 10^{-5}\right)\left(\dfrac{W}{L}\right)_1 (5 - 1)^2 \ \Rightarrow \ \left(\dfrac{W}{L}\right)_1 = 1.74$

25. (D) M_2 is in saturation because

$V_{GS2} = V_{DS2} > V_{GS2} - V_{TN}$

M_1 is in non saturation because

$V_{GS1} = V_i = 5$ V, $\quad V_{DS1} = V_D = 0$ V

$V_{DS1} < V_{GS1} - V_{TN}\ , \quad I_{D1} = I_{D2}$

$\left(\dfrac{W}{L}\right)_1 [2(V_{GS1} - V_{TN1})V_{DS1} - V_{DS2}^2] = \left(\dfrac{W}{L}\right)_2 (V_{GS2} - V_{TN2})^2$

$\Rightarrow \left(\dfrac{W}{L}\right)_1 [2(5 - 0.8)(0.1) - (0.1)^2] = (1)(5 - 0.1 - 0.8)^2$

$\left(\dfrac{W}{L}\right)_1 (0.83) = 16.81 \quad \Rightarrow \quad \left(\dfrac{W}{L}\right)_1 = 20.3$

26. (B) $I_{D1} = K_{n1}(V_{GS1} - V_{TN})^2 = K_{n2}(V_{GS2} - V_{TN})^2$

$V_{GS1} = 5 - V_{GS2} \quad \Rightarrow \quad (5 - V_{GS2} - 1)^2 = 200\,(V_{GS2} - 1)^2$

$\Rightarrow \quad V_{GS2} = 2.76$ V, $\quad V_{GS1} = 2.24$ V

$I_{D1} = 400 \times 10^{-6}\,(2.24 - 1)^2 = 0.62$ mA

27. (B) $V_{GS2} = V_{GS3} = 2.76$ V

$I_{D4} = K_{n4}\,(V_{GS4} - V_{TN})^2 = K_{n3}\,(V_{GS3} - V_{TN})^2$

$= 100 \times 10^{-6}\,(2.76 - 1)^2 = 0.31$ mA

28. (C) $V_{GS} = 4.2$ V, $\quad V_{DS} = 0.1$ V

$V_{DS} < V_{GS} - V_{TN}$, Thus transistor is in non saturation.

$I_D = \dfrac{5 - 0.1}{10\text{k}} = 0.49$ mA

$I_D = \dfrac{k_n'}{2}\dfrac{W}{L}\left\{2\,(V_{GS} - V_{TN})\,V_{DS} - V_{DS}^2\right\}$