Chapter 4

Field Effect Transistors

CHAPTER HIGHLIGHTS

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Introduction

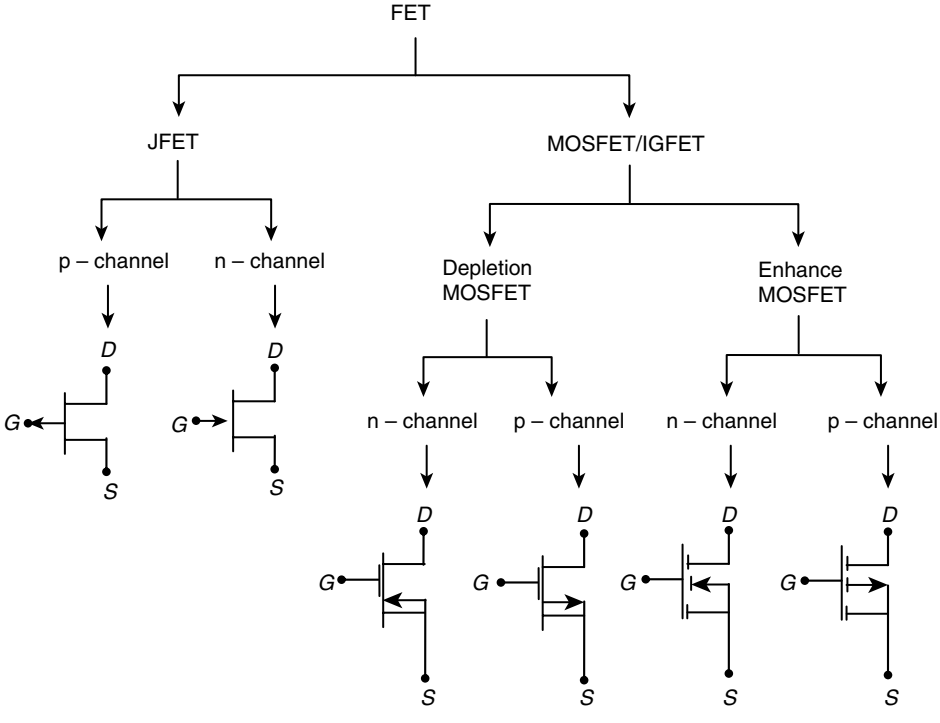
The bipolar junction transistor relies on two types of charge carriers, that is, free electrons and holes. Another kind of transistor is called the field-effect transistor (FET). This type of device is unipolar because its operation depends on only one type of charge, either free electrons or holes. In other words, an FET has majority carriers but not minority carriers.

The FET is generally much less noisy than the BJT. BJT is a current controlled device, and FET is a voltage controlled current device.

These are two types:

(i) Junction field-effect transistors (JFET)

(ii) Metal–oxide–semiconductor field-effect transistor (MOSFET)



JFET

A junction field-effect transistor is a three-terminal semiconductor device in which current conduction is by majority type of carriers, that is, electrons or holes. JFET has high input impedance and low noise level.

Construction of JFET

A junction field-effect transistor is a three-terminal semiconductor device in which current conduction is by one type of carrier, that is, electrons or holes.

A JFET consists of a p-type or n-type silicon material, containing two p–n junctions at the sides. If the bar is n-type, it is called an n-channel JFET and if the bar is of p-type, it is called a p-channel JFET.

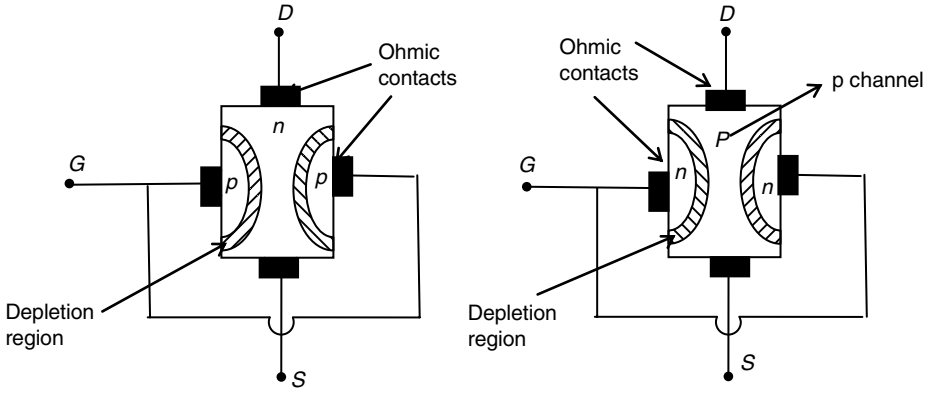


Figure 1 Junction field-effect transistors

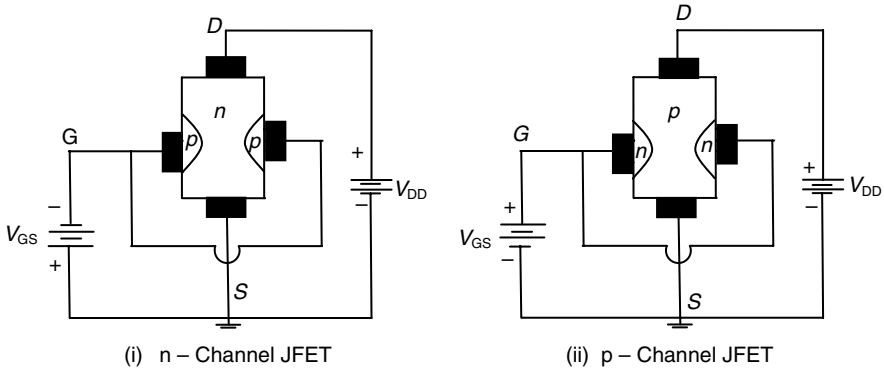


Figure 2 JFET polarities

The input circuit (gate to source) of an JFET is reverse biased and output circuit (drain to source) of a JFET is forward biased, that is, the device has high input impedance and low output impedance.

Working Principle

The two p–n junctions at the sides form two depletion layers. The current conduction by charge carriers (majority carriers) is through the channel between the two depletion layers and out of the drain. The width of the channel, that is, the resistance of this channel can be controlled by changing input voltage V_{GS}.

If the reverse voltage V_{GS} increases, the wider will be the depletion layers and narrower will be the conduction channel, that is, channel width decreases means resistance of the channel increases, and therefore, drain–source current decreases. Otherwise, the reverse will happen, when V_{GS} decreases.

Thus, JFET operates on the principle that width and resistance of the conducting channel can be varied by changing the reverse voltage V_{GS}.

Case (i): For n-channel JFET

$$V_{GS} = 0 \text{ V}, V_{DS} = 0 \text{ V}$$

In this case, drain current $I_D = 0$, because $V_{DS} = 0$ V

Case (ii): When $V_{GS} = 0$ V and V_{DS} is some positive value

As the voltage V_{DS} is increased from 0 V to a few volts, the current will increase as determined by ohm's law and the characteristics plot of I_D V_S V_{DS} shown in Figure 4.

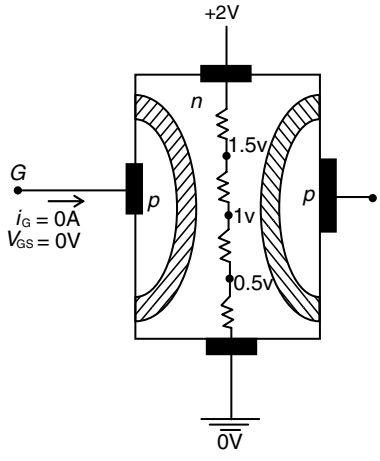


Figure 3 Varying reverse bias potential across the p–n junction of an n-channel JFET

I–V Characteristics

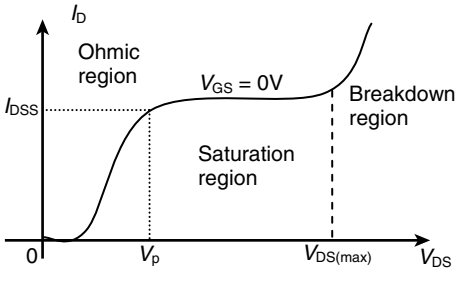


Figure 4 – I_D Vs V_{DS} for V_{GS} = 0 V

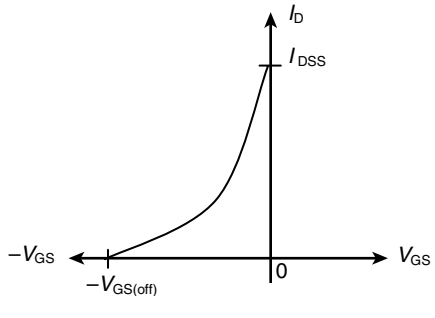
The ohmic relationship between V_{DS} and I_D continues till V_{DS} reaches a certain critical value is called pinch off voltage (V_p).

If the drain voltage exceeds $V_{DS(max)}$, JFET enters into breakdown region.

The region between V_P and $V_{DS(max)}$ is called constant current region because when V_{DS} equal to V_P, the channel is effectively closed and does not allow further increase in drain current.

Case (iii): If $V_{GS} < 0$ and V_{DS} = constant

If the reverse voltage V_{GS} on the gate is continuously increased, a state is reached when the two depletion layers touch each other at $|VGS(off)| = |V_P|$ and the channel is cut-off.



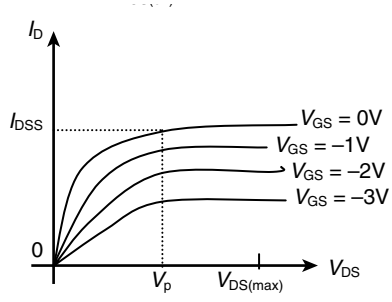


Figure 5 n-channel JFET characteristics

Shorted Gate Drain Current (I_{DSS})

It is the drain current with source, short circuited to gate ($V_{GS} = 0$) and drain voltage (V_{DS}) equal to pinch off voltage. It is the maximum drain current (I_{DSS}). The region between V_P and $V_{DS(max)}$ (breakdown voltage) is called constant current region or saturation region. JFET behaves as a constant current device. For proper working of JFET, it must be operated in the saturation region or active mode.

Pinch Off Voltage (V_P)

It is the minimum drain–source voltage at which the drain current becomes constant. For values of V_{DS} greater than V_P, the drain current is almost constant. Because when V_{DS} is equal to V_P, the channel is effectively closed and does not allow further increase in drain current. However, V_{DS} should not exceed $V_{DS(max)}$; otherwise, JFET may breakdown.

Gate–source Cut-off Voltage $V_{GS(off)}$

It is the gate–source voltage where the channel is completely cut-off and the drain current becomes zero. As the reverse gate–source voltage is increased, the cross-sectional area of the channel decreases. This in turn decreases the drain current. At some gate to source voltage, the depletion region is increased and touch each other. In this condition, the channel is cut-off and the drain current reduces to zero.

$$V_P = |V_{GS(off)}|$$

Parameters of FET

Drain Current (I_D)

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \text{ Amp}$$

where I_D is the drain current at given V_{GS}; I_{DSS} is the short-circuit gate drain current; V_{GS} is the gate–source voltage; and V_P is the gate–source cut-off voltage (or) pinch off voltage.

Drain Resistance (r_d)

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}; \text{ at constant } V_{GS}$$

The drain resistance of a JFET has a large value range from 10 kΩ to 1 MΩ.

Transconductance (g_m)

It is the ratio of change in drain current (ΔI_D) to the change in gate–source voltage (ΔV_{GS}) at constant drain–source voltage.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}.$$

Amplification Factor (λ)

It is the ratio of change in drain–source voltage (ΔV_{DS}) to the change in the gate–source voltage (ΔV_{GS})

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at constant } I_D.$$

Relationship among JFET Parameters

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D}$$

$$\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} = r_d \times g_m$$

Therefore, $\mu = g_m r_d$

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_P}\right]$$

where

$$g_{mo} = \frac{2I_{DSS}}{|V_P|} \text{ or } \frac{-2I_{DSS}}{V_P}$$

or

$$g_m = g_{mo} \cdot \sqrt{\frac{I_D}{I_{DSS}}}$$

DC drain resistance, $R_{DS} = \frac{V_{DS}}{I_D}$

Voltage gain $A_V = -g_m R_D$

Solved Examples

Example 1

A JFET has $V_p = -4.5$ V, $I_{DSS} = 10$ mA, and $I_D = 2.5$ mA. Determine the transconductance

Solution

$$g_m = \frac{-2\,I_{DSS}}{V_p}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$V_{GS} = V_P\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right] = 2.22 \text{ mA} \mid \text{V}$$

Example 2

For an n-channel JFET $I_{DSS} = 8.7$, mA, $V_p = -3$ V, and $V_{GS} = -1$ V. Find the values of

(a) I_D (b) g_{m0} (c) g_m

Solution

(a) $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 = 3.8667$ mA

(b) $g_{m0} = \frac{-2\,I_{DSS}}{V_P} = 5.8$ mA / V

(c) $g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = 3.867$ mA|V

Example 3

For an n-channel JFET, $I_{DSS} = 8$ mA, $V_p = -4$ V, and $V_{GS} = -1$ V. Determine I_D, g_{mo}, and g_m.

Solution

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 8 \times 10^{-3}\left(1 - \frac{(-1)}{(-4)}\right)^2$$

$I_D = 4.5$ mA

$$g_{mo} = \frac{-2\,I_{DSS}}{V_p} = 4 \text{ mA/V}$$

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_p}\right) = 3 \text{ mA/V}.$$

Example 4

In a JFET, the drain current is changed by 0.25 mA when the gate–source voltage is changed by 0.25 V, keeping drain–source voltage constant. Calculate the transconductance of the JFET.

Solution

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\Big|_{V_{DS} = \text{constant}} = \frac{0.25 \times 10^{-3}}{0.125}$$

$g_m = 2$ mA | V.

Example 5

A JFET has $g_m = =10$ ms, $I_{DSS} = 10$ μA. Calculate V_{GS} (OFF).

Solution

$$g_m = g_{mo} = \frac{-2\,I_{DSS}}{V_P} = \frac{-2\,I_{DSS}}{V_{GS(OFF)}}$$

$$10 \times 10^{-3} = \frac{-2 \times 10 \times 10^{-6}}{V_{GS}\,(OFF)}$$

V_{GS} (OFF) = –2 mV

Example 6

A FET has a drain current of 4 mA. If $I_{DSS} = 6$ mA and V_{GS} (OFF) = –6 V. Find the values of V_{GS} and V_p.

Solution

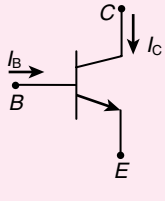
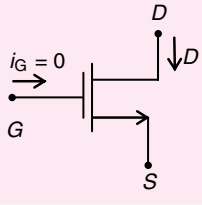
$$I_D = 4 \text{ mA};\ I_{DSS} = 6 \text{ mA}$$

$$V_{GS} = V_{GS}(\text{OFF})\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

$$= -6\left[1 - \sqrt{\frac{4\text{ mA}}{6\text{ mA}}}\right] = -1.1 \text{ V}$$

Pinch off voltage, $V_p = V_{GS}(\text{OFF}) = -6$ V

Relationship Between BJT and JFET

S. No	BJT	JFET
(i)		
(ii)	$I_C = \beta I_B$	$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$
(iii)	$I_C \approx I_E$	$I_D = I_S$
(iv)	$V_{BE} = 0.7$ V	$I_G \approx 0$ A
(v)	Current controlled (I_B) current device (I_C)	Voltage controlled (V_{GS}) current device (I_D)

Comparisons of JFET and BJT

1. FET is a unipolar device, that is, operation depends only on the flow of majority carriers. BJT operations depend on both minority and majority charge carriers.
2. FET is a voltage controlled device and BJT is a current controlled device.
3. FET is less noisier than BJT (minority carriers more noisier)
4. FET is smaller than the BJT.
5. BJTs are faster than the FETs.
6. The input circuit of FET is reverse biased. (i.e., input impedance higher $R_{in} \approx 100$ mΩ). FET offers a larger input impedance and lower output impedance. Therefore, FET can act as an excellent buffer amplifier but the BJT has low input impedance because its input is forward biased.
7. FET does not suffer from minority charge carrier storage effects, and it has 'higher switching speeds and cut-off frequency' BJT has low switching speed and cut-off frequencies.
8. BJTs are cheaper than FETs.
9. FET amplifiers have low gain bandwidth product due to the junction capacitance (disadvantage).
10. FET has a negative (zero) temperature coefficient at high current levels, and it prevents the FET thermal runaway. The BJT has a 'positive' temperature coefficient at high current levels that leads to thermal breakdown.
11. No current enters the gate of JFET, that is, $I_G = 0$ A. However, typical BJT base current I_B be a few microamperes.
12. In JFET, there are no junctions as in an ordinary transistor. The conduction is through an n-type or p-type semiconductor material.

Example 7

A JFET has $I_{DSS} = 16$ mA and $V_P = -4$ V. $V_{GS} = -2$ V, the value of drain current is

(A) 8 mA. (B) 4 mA.
(C) 16 mA. (D) 6 mA.

Solution

We know $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

$$= 16\left[1 - \frac{(-2)}{(-4)}\right]^2 \times 10^{-3} = 16 \times 10^{-3} \times 0.25 = 4 \text{ mA}$$

Example 8

The transconductance of a JFET used as a voltage amplifier is 2,500 $\mu\Omega^{-1}$ and drain resistance is 15 kΩ. The voltage gain of the amplifier is

(A) 25. (B) 30. (C) 37.5.(D) 40.

Solution

Given $g_m = 2500 \times 10^{-6}\ \Omega^{-1}$

$R_D = 15 \times 10^3\ \Omega$

Voltage gain $A_V = g_m R_D$

$= 2{,}500 \times 10^{-6} \times 15 \times 10^3 = 37.5$

Example 9

In a p-channel JFET, the charge carriers are

(A) electrons.
(B) holes.
(C) both electrons and holes.
(D) either e^-s or holes.

Solution: (B)

Example 10

If the reverse bias voltage is increased, then the width of the conducting channel of JFET is

(A) increased. (B) decreased.
(C) remains same. (D) None of the above

Solution: (B)

Example 11

The input control parameter of JFET is
(A) source voltage. (B) gate voltage.
(C) drain voltage. (D) None of these

Solution: (B)

Example 12

The gate voltage in a JFET at which drain current becomes zero is called
(A) Breakdown (B) active.
(C) cut-off. (D) saturation.

Solution: (C)

Example 13

In a common source JFET amplifier, the output voltage is
(A) in phase with the input.
(B) 90° out of phase.
(C) 180°out of phase with input.
(D) None of the above

Solution: (C)

Example 14

The constant current region of a JFET lies between
(A) cut-off and saturation.
(B) cut-off and pinch off.
(C) pinch off and breakdown regions.
(D) 0 and I_{DSS}.

Solution: (C)

Example 15

The transconductance of a JFET ranges from
(A) 0.5 to 30 mA/V.
(B) 100 to 500 mA/V.
(C) 500 to 750 mA/V.
(D) Above 750 mA/V.

Solution: (A)

Introduction to MOSFET

The main drawback of JFET is that its gate must be reverse biased for proper operations of the device. This means it can only have negative gate operation for n-channel and positive gate operation for p-channel. The name MOSFET stands for 'Metal–oxide–semiconductor field effect transistor'. The insulating layer between the gate and the channel has resulted in another name for the device insulated gate FET (IGFET).

MOSFETs are broadly classified into two categories: depletion-mode MOSFET or

D-MOSFET and enhancement-mode MOSFET or E-MOSFET.

D-MOSFET

Construction of the n-channel Depletion-Mode MOSFET

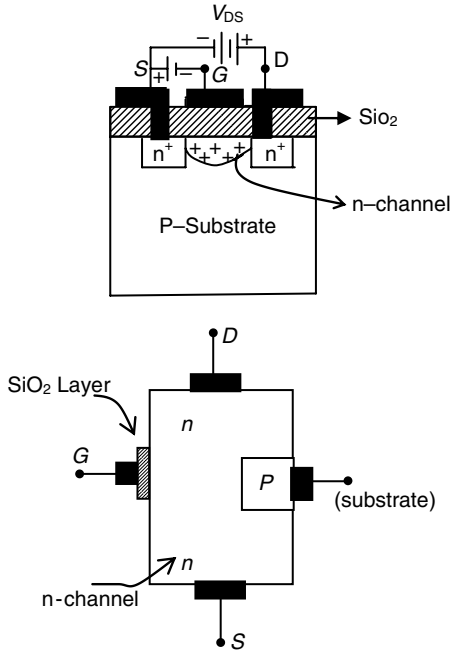


Figure 6 n-channel D-MOSFET

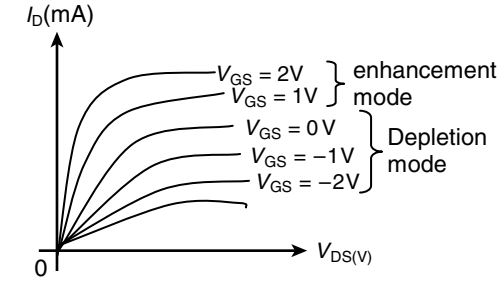
The D-MOSFET can be operated in both the depletion mode and the enhancement mode. The device consists of a p-type substrate in which there are diffused two heavily doped n+-type semiconductor blocks. In between the blocks is a lightly doped n-type channel. The majority carrier e's flowing from source to drain and they must pass through the narrow channel between the gate and the p-type region.

A thin layer of metal oxide (SiO_2) is deposited over a small portion of the channel. A metallic gate is deposited over the oxide layer. An SiO_2 is an insulator, and therefore, gate is insulated from the channel. Since the gate is insulated from the channel, we can apply either negative (or) positive voltage to the gate. Since D-MOSFET can be operated in both depletion-mode and enhancement-mode JFET can be operated only in depletion mode. If a 'positive' potential is applied to the drain, electrons of the n-type drain block are attracted towards the positive terminal. If a 'negative' voltage is applied to the gate, positive charge carriers would be induced in the n-type channel. There tends to join with free e's present in the channel, creating a depletion region and increasing the channel resistance. Thus, the MOSFET is termed as depletion-mode MOSFET.

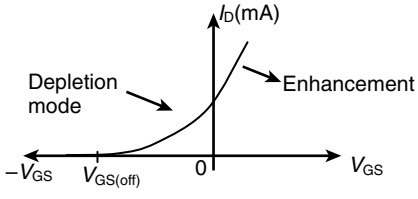
If the gate is given positive bias with respective source, the number of charge carriers, that is, e^-s in the n-channel further increases with the result that the drain current increases. It means that a 'positive' gate bias the depletion-mode MOSFET can be operated as enhancement-mode MOSFET.

Transfer Characteristics of D-MOSFET

The drain and transfer characteristics of an n- channel depletion–enhancement mode MOSFET.



(i) Drain characteristic

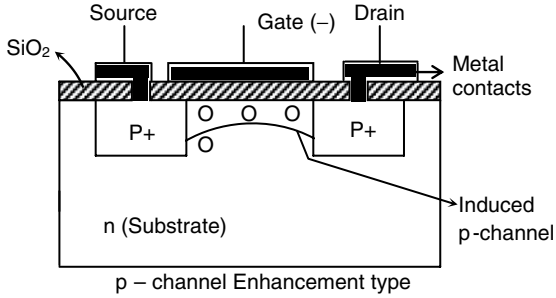


(ii) Transfer characteristics

Enhancement-Mode MOSFET or E-MOSFET

There are two types: enhancement p-channel and n-channel types.

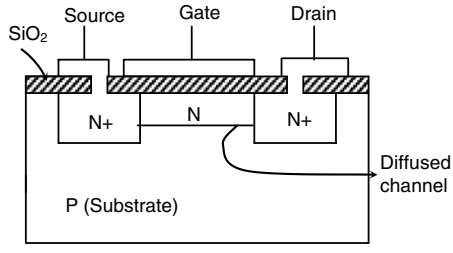
p-channel E-MOSFET



p – channel Enhancement type

A lightly doped n-type substrate into which two highly doped p^+ regions are diffused. The p+ regions act as source and drain. A thin layer of SiO_2 is grown over the surface of the structure and holes are cut into the oxide layer, allowing contact with the source and drain. The gate metal area is overlaid on the oxide, covering the entire channel region. Metal contacts are made to the drain and source. When the gate is given negative supply voltage, positive charges will be induced in the substrate between the source and the drain, forming an inversion layer. Current flows from source to drain through the channel.

n-channel E-MOSFET

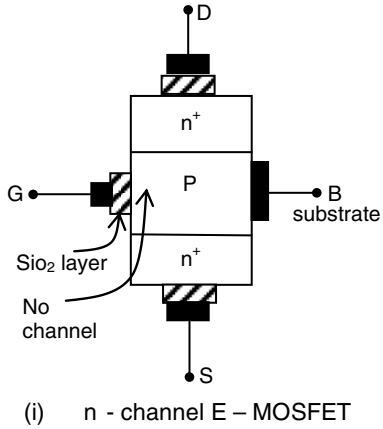


n – Channel E- MOSFET

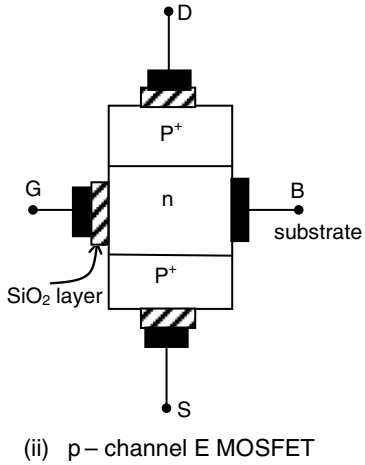
An n-channel diffused between two n^+ regions is a p-substrate. With gate potential is zero, maximum drain current flows. When gate is given negative supply, positive ions are induced into the channel and thus reduces the conductivity. The operation is similar to that of JFET.

$$I_D = I_{DSS} = \left(1 - \frac{V_{DS}}{V_T}\right)^2 \quad \text{for } |V_{DS}| \geq |V_T|$$

E-MOSFET operates only in the enhancement mode and has no depletion mode, and the E-MOSFET has no physical channel from source to drain because the substrate extends completely to the Sio_2 layer. The minimum value of V_{GS} of proper polarity that turn 'ON' the E-MOSFET is called 'threshold voltage' [$V_{GS(Th)}$]. The n-channel device requires positive $V_{GS} \geq V_{GS(th)}$ and the p-channel device requires negative $V_{GS}(\geq V_{GS(th)})$.



(i) n - channel E – MOSFET



(ii) p – channel E MOSFET

1. It does not conduct when gate–source voltage $V_{GS} = 0$. This is also called normally off MOSFET. In these MOSFETs, drain current I_D flows only when $V_{GS} \geq V_{GS(th)}$.

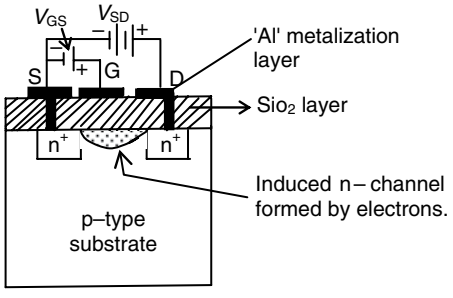


Figure 7 Operation of n-channel E-MOSFET

Case (i) $V_{GS} = 0$ V and V_{DS} = positive voltage

When V_{DS} = positive voltage and no potential is applied to the gate, the two n-regions and one p-substrate form two P–N junctions connected back-to-back with a resistance of the p-substrate. Both the junctions are in reverse biased at the same time. Therefore, only a reverse leakage current flows.

The minimum value of gate–source voltage V_{GS} that is required to form the inversion layer (N-type) is termed the gate–source threshold voltage $V_{GS(th)}$.

$$\text{If } V_{GS} < V_{GS(th)}, \text{ then } I_D = 0\text{A (OFF)}$$

$$V_{GS} \geq V_{GS(th)} \text{ (ON)}$$

An N-type inversion layer connects the source to drain and the drain current I_D is large depending upon the device being used $V_{GS(th)}$ may vary from less than 1 V to more than 5 V.

Therefore, JFET and D-MOSFET are classified as the depletion-mode devices because their conductivity depends on the action of depletion layers. E-MOSFET is classified as an enhancement-mode device because its conductivity depends on the action of the inversion layer. Further, depletion-mode devices are normally ON, when $V_{GS} = 0$ V. While enhancement-mode devices are normally OFF when $V_{GS} = 0$ V.

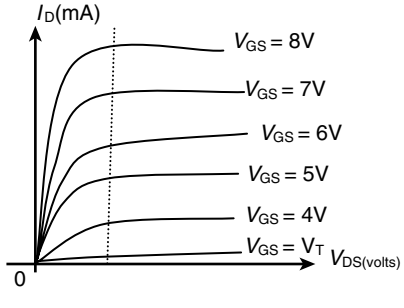


Figure 8 Drain characteristic of an n-channel enhancement MOSFET

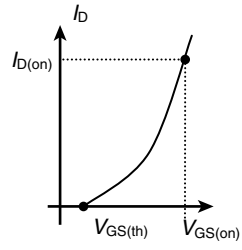


Figure 9 Transconductance curve for n-channel E-MOSFET

Drain Current Relationship

$$I_D = K[V_{GS} - V_T]^2$$

where $V_T = V_{GS(th)}$ = threshold voltage

$$K = \frac{I_{D(on)}}{[V_{GS(on)} - V_{GS(th)}]^2}$$

Increasing order of input impedance:

BJT < op-amp < JFET < MOSFET

Relationship between I_D and V_{GS}

MOSFET in triode region

$$V_{GS} \geq V_{th}$$

$$I_D = \mu_n C_{ox} \cdot \frac{W}{L}\left[[V_{GS} - V_T] \cdot V_{DS} - \frac{V_{DS}^2}{2}\right]$$

where $K^1_n = \mu_n c_{ox}$

$\Rightarrow$ transconductance parameter

$\frac{W}{L} \Rightarrow$ aspect ratio

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$I_D = K_n^1 \frac{W}{L}\left[(V_{GS} - V_T).V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$I_D = K\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

Where $K = \frac{\mu_n C_{ox} W}{L}$

(ii) MOSFET in saturation region

$$V_{GS} \geq V_T \text{ and } V_{DS} \geq (V_{GS} - V_T)$$

Let $V_{DS(sat)} = V_{GS} - V_T$

Therefore, $I_D = \frac{K_n^1}{2}\frac{W}{L}\left[(V_{GS} - V_T)^2\right] = K(V_{GS} - V_T)^2$

where $K = \frac{\mu_n C_{ox} W}{2L}$ for n-channel E-MOSFET.

Body Effect

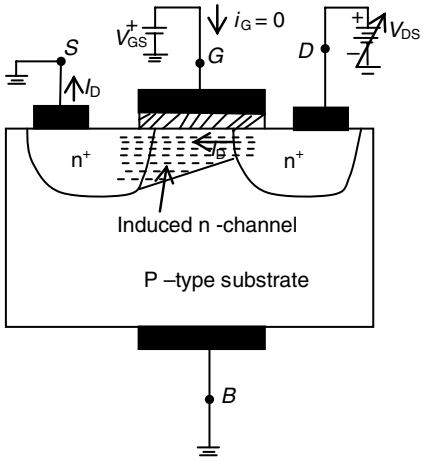


Figure 10 Enhancement n-mos transistor as V_{DS} is increased

In many applications, the source terminal is connected to the substrate (or body) terminal B, which results in the p–n junction between the substrate and the induced channel having a constant zero (cut-off) bias. In such a case, the substrate does not play any role in circuit operation and its existence can be ignored altogether.

In integrated circuits, the substrate is usually common to many MOS transistors. In order to maintain the cut-off condition for all the substrate-to-channel junctions, the substrate is usually connected to the most negative power supply. In an n-mos circuit, (the most positive in a p-mos circuit). The resulting reverse bias voltage between the source and the body (V_{SB} in an n-channel) will have an effect on device operation.

The reverse bias voltage will widen the depletion region, and this in turn reduces the channel depth. To return the channel to its former state, V_{GS} has to be increased. The effect of V_{SB} on the channel can be represented as a change in V_T.

$$V_T = V_{TO} + \gamma\left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right]$$

where V_{T0} is the threshold voltage for $V_{SB} = 0$; ϕ_f is the constant ($2\phi_f \approx 0.6$ V); γ is $\frac{\sqrt{2q\ N_A \varepsilon_s}}{C_{ox}}$; and V_T is the threshold voltage.

From the equation, it indicates that an incremental change in V_{SB} gives rise to an incremental change in V_T. This means that there is an incremental change in I_D, even though V_{GS} = constant.

Since the body voltage controls i_D, then the body acts as another gate for the MOSFET, and this is known as the body effect.

NOTE

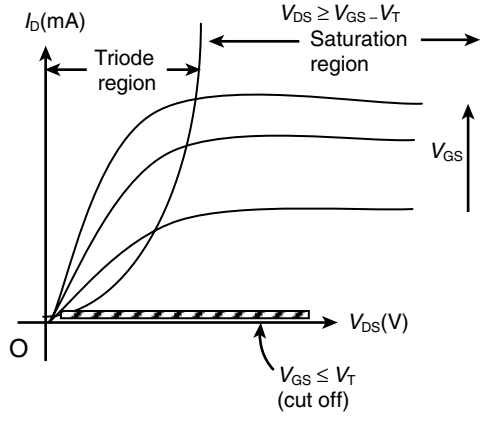
Both V_T and K are temperature sensitive, the magnitude V_T decreases by about 2 mV/°C rise in temperature and K^1 decreases with temperature.

Therefore, $V_T \downarrow \Rightarrow I_D \uparrow K^1 \downarrow \downarrow$ (more decrement)

i.e., $I_D \downarrow$ (overall effect)

The overall observed effect of a temperature increases with a decrease in drain current.

Summary of the Mosfet Current–Voltage Characteristics



n-mos Transistor

(i) **Conditions for triode region**.

$V_{GS} \geq V_T$ (MOSFET ON)

$V_{DS} < V_{GS} - V_T$(continuous channel)

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

***I–V* relationships:**

$$I_D = \mu_n .C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{Ds}^2\right]$$

For $V_{DS} << 2(V_{GS} - V_T)$

$$r_{ds} = \frac{V_{DS}}{I_{DS}} = \frac{1}{\left[\mu_n\ C_{ox} . \frac{W}{L}(V_{GS} - V_T)\right]}$$

(ii) **Conditions for operation in the saturation region**

$V_{GS} \geq V_T$,

$$V_{DS} \geq V_{GS} - V_T$$

$$V_{DS(sat)} = V_{GS} - V_T$$

***I–V* relationships:**

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

If $\lambda = 0$

$$I_{Dsat} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)^2$$

Threshold voltage:

$$V_T = V_{TO} + \gamma \left(\sqrt{2\phi_f + |V_{SB}|} - \sqrt{2\phi_f}\right)$$

Parameters:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \text{ (F/m}^2\text{)}$$

$$K^1_n = \mu_n C_{ox} \text{ (A/V}^2\text{)}$$

$$\lambda = \frac{1}{V_A} \text{ (V}^{-1}\text{)}$$

$$\gamma = \frac{\sqrt{2q\ N_A\ \varepsilon_s}}{C_{OX}\left(V^{1/2}\right)}$$

Constants:

$$\varepsilon_0 = 8.854 \times 10^{-12} \text{ F/m}$$
$$\varepsilon_{ox} = 3.9\varepsilon_0$$
$$\varepsilon_s = 11.7\varepsilon_0$$
$$Q = 1.6 \times 10^{-19} \text{ C}$$

pmos Transistors

Conditions for triode region:

$V_{GS} \le V_T$ (ON state)

$V_{DS} \ge V_{GS} - V_T$ (continuous channel)

$$I_D = K^1_P \frac{W}{L}\left[\left(V_{GS} - V_T\right).V_{DS} - \frac{1}{2}V^2_{DS}\right]$$

$$K^1_P = \mu_P C_{ox}.$$

Conditions for saturation region:

$V_{DS} \le V_{GS} - V_T$ (pinch off channel)

$$I_D = \frac{1}{2}.K^1_P \frac{W}{L}\left[V_{GS} - V_T\right]^2\left(1 + \lambda.V_{DS}\right)$$

where V_{GS}, V_T, λ, and V_{DS} all are negative.

If $\lambda = 0$

$$I_D = \frac{1}{2}\mu_P\ .\ C_{ox}\ .\frac{W}{L}\left[V_{SG} - |V_T|\right]^2$$

Example 16

The threshold voltage of an n-channel MOSFET can be increased by

(A) increasing the channel dopant concentration.
(B) reducing channel dopant concentration.
(C) reducing the gate-oxide thickness.
(D) reducing the channel length.

Solution: (C)

Example 17

An MOS capacitor made using p-type substrate is in the accumulation mode. The dominant charge in the channel is due to the presence of

(A) holes.
(B) electrons.
(C) positively charged ions.
(D) negatively charged ions.

Solution: (A)

Example 18

The drain of an n-channel MOSFET is shorted to the gate so that $V_{GS} = V_{DS}$. The threshold voltage (V_T) of MOSFET is 2 V. If the drain current I_D is 2.5 mA for $V_{GS} = 3$ V, then for $V_{GS} = 5$ V I_D is

(A) 4 mA. (B) 9 mA.
(C) 15 mA. (D) 22.5 mA.

Solution

If $V_{GS} = V_{DS} \Rightarrow$ MOSFET in saturation region,

$$I_D = \frac{k_n}{2}\left(V_{GS} - V_T\right)^2$$

$$I_D = 2.5 \text{ mA}$$

$$V_{GS} = 3 \text{ V} ; V_T = 2 \text{ V}$$

$$2.5 \times 10^{-3} = \frac{k_n}{2}(3-2)^2$$

$$K_n = 5 \times 10^{-3} \text{ A/V}^2$$

$$K_n = 5 \text{ mA/V}^2$$

$$I_D = \frac{K_n}{2}\left(V_{GS} - V_T\right)^2$$

$V_{GS} = 5$ V, then

$$I_D = 2.5 \times 10^{-3}(5-2)^2$$

$$I_D = 22.5 \text{ mA}$$

Example 19

In the following circuit for the MOS transistors, $\mu_n C_{ox}$ = 150 μA/V^2, and the threshold voltage $V_T = 1$ V. The voltage V_0 at the source of the upper transistor is

(A) 2 V. (B) 3 V. (C) 4 V (D) 5 V

Solution

From the figure,

$$I_{DS1} = I_{DS2}$$

$$\frac{K_{n1}}{2}\left(V_{GS1} - V_T\right)^2 = \frac{K_{n2}}{2}\left(V_{GS2} - V_T\right)^2,$$

where

$$V_{GS1} = 5 - V_0$$

$$\frac{1}{2}\left(150 \times 10^{-6}\right)(8)\left(5 - V_0 - 1\right)^2$$

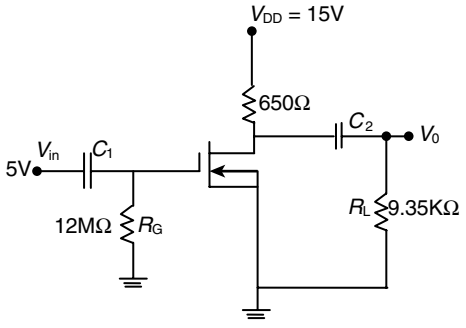
$$= \frac{1}{2}.\left(150 \times 10^{-6}\right)(2)\left(V_0 - 1\right)^2$$

$$2(5 - V_0 - 1) = (V_0 - 1) \Rightarrow 8 - 2V_0 = V_0 - 1$$

$$3V_0 = 9 \Rightarrow V_0 = 3 \text{ V}$$

Direction for questions 20 and 21:

The D-MOSFET used in the following amplifier has an I_{DSS} = 10 mA and g_m = 3.5 mA/V.



Example 20

The DC drain-to-source voltage V_{DS} is
(A) 5 V. (B) 7.5 V.
(C) 8.5 V. (D) 10 V.

Solution

The input signal is capacitively coupled to the gate.
For DC value of $V_{GS} = 0$ V (C is the open circuit)

$$I_D = I_{DSS} = 10 \text{ mA}$$

$$V_{DS} = V_{DD} - I_D R_D = 15 - 10 \times 10^{-3} \times 650 = 8.5 \text{ v}$$

Example 21

The AC output voltage for $V_{in} = 450$ mA is
(A) 0.96 V. (B) 1.2 V.
(C) 1.5 V. (D) none of the above

Solution

$$R_{AC} = R_D \parallel R_L = 650\ \Omega \parallel 9.35\ \text{k}\Omega$$

$$= \frac{6.077 \times 10^6}{10 \times 10^3} = 608\ \Omega$$

$$V_{out} = A_v V_{in} = (g_m R_{AC}) \cdot V_{in}$$

$$= 3.5 \times 10^{-3} \times 608 \times 450 \times 10^{-3} = 0.96 \text{ v}$$

Example 22

The MOSFET differs from a JFET mainly because
(A) the JFET has a p–n junction.
(B) the MOSFET has two gates.
(C) of power rating.
(D) None of the above

Solution: (A)

Example 23

The p-channel D-MOSFET with a negative V_{GS} is operating in
(A) the depletion mode.
(B) the enhancement mode.
(C) cut-off region.
(D) saturation region

Solution: (B)

Direction for questions 24 and 25:

Consider a process technology for which $L_{min} = 0.5$ mm, $t_{ox} = 10$ nm, $\mu_n = 500$ cm^2/Vs, and $V_T = 0.7$ V

Example 24

Find C_{ox} and K_n
(A) 3.45×10^{-3} F/m^2, 172.5 mA/V^2
(B) 5.5×10^{-3} F/m^2, 172.5 μA/V^2
(C) 3.45×10^{-3} F/m^2, 172.5 μA/ V^2
(D) 3.45×10^{-6} F/m^2, 172.5 mA/V^2

Solution

We know

$$C_{ox} = \frac{\varepsilon_{0x}}{t_{0x}} = \frac{3.95.\varepsilon_0}{t_{0x}} = \frac{3.45 \times 10^{-11}}{10 \times 10^{-9}} = 3.45 \times 10^{-3} \text{ F/m}^2.$$

$$K_n = \mu_n C_{ox} = 500 \times \frac{cm^2}{V - s} \times 3.45 \times 10^{-3} \text{ F/m}^2$$

$$= 500 \times 10^{-4} \frac{m^2}{V - \text{sec}} \times 3.45 \times 10^{-3} \text{ F/m}^2$$

$$= 500 \times 3.45 \times 10^{-7} \text{A} / \text{V}^2$$

$$K_n = 172.5\ \mu\text{A/V}^2.$$

Example 25

For an MOSFET with $\frac{W}{L} = 5$, calculate the values of V_{GS} and $V_{DS(min)}$ to operate the transistor in the saturation region with a DC current $I_D = 80$ μA.
(A) $V_{GS} = 1.13$ V, $V_{DS} = 0.43$ V
(B) $V_{GS} = 0.43$ V, $V_{DS} = 1.13$ V
(C) $V_{GS} = 2.25$ V, $V_{DS} = 1.55$ V
(D) None of the above

Solution

We know $I_D = \frac{K_n}{2} \cdot \frac{W}{L} (V_{GS} - V_T)^2$

$$I_D = 80\ \mu\text{A}$$

$$80 \times 10^{-6} = \frac{172.5}{2} \times 10^{-6} \times 5 (V_{GS} - V_T)^2$$

$$(V_{GS} - V_T)^2 = 0.1855$$

$$V_{GS} - V_T = V_{DS(min)} = 0.43 \text{ V}$$

$$V_{GS} = 0.43 + 0.7 = 1.13 \text{ V}$$

Example 26

The value of V_{GS} required to cause the device to operate as a 1.25 kΩ resistor for very small V_{DS} is
(A) $V_{GS} = 1.2$ V (B) $V_{GS} = 1.8$ V
(C) $V_{GS} = 1.63$ V (D) $V_{GS} = 2$ V

Solution

For the MOSFET in the triode region, V_{DS} very small

$$I_D = K_n \cdot \frac{W}{L}(V_{GS} - V_T)V_{DS} \quad (\text{neglect } \frac{1}{2}V^2{}_{DS})$$

We know $r_{ds} = \frac{V_{DS}}{i_D}$, small V_{DS}

$$r_{ds} = \frac{1}{K_n\left(\frac{W}{L}\right)(V_{GS} - V_T)}$$

$$1{,}250 = \frac{1}{172.5\times10^{-6}(V_{GS} - V_T)\times5}$$

$$V_{GS} - V_T = 0.9275$$

$$V_{GS} = 1.63 \text{ V}$$

Example 27

An n-channel JFET has I_{DSS} = 1 mA and V_p = –4 V. Its transconductance g_m (mA/V) for an applied gate to source voltage V_{GS} of –3 V is

Solution

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right) = \frac{2\times1\times10^{-3}}{4}\left(1 - \frac{-3}{-4}\right)$$

$$= \frac{2\times1\times10^{-3}}{4\times4} = 0.125 \text{ mA/V}.$$

Example 28

An ideal p-channel MOSFET has c_{ox} = 8 × 10^{-8} F/cm^2, μ_p = 300 cm^2/Vs, ℓ = 2 µm, t_{ox} = 250 A°, V_{TP} = −0.8 V, w = 15 µm. If transistor is operating in non-saturation region at V_{SD} = 0.6 V, value of g_m is

Solution

$$I_D = \frac{\mu C_{ox} w}{2L}\left(2(V_{GS} + V_T)V_{SD} - V_{SD}^2\right)$$

$$I_D = \frac{300\times8\times10^{-8}\times15\times10^{-4}}{2\times2\times10^{-4}}$$

$$\left[2(V_{SG} + V_T)V_{SD} - V_{SD}^2\right]$$

$$= 9\times10^{-5}\left[2(V_{SG} + V_T)V_{SD} - V_{SD}^2\right]$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = 9\times10^{-5}\times2\times V_{SD}$$

$$= 0.6\times9\times10^{-5}\times2 = 0.108 \text{ ms}.$$

Example 29

For a given JFET, I_{DSS} = 15 mA, V_P = −4V, V_{DS} = 10 V. The value of resistance R_S for a drain current of I_{DS} = 7 mA is

Solution

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$7\times10^{-3} = 15\times10^{-3}\left(1 - \frac{(V_{GS})}{-4}\right)$$

$$0.6831 = 1 - \frac{V_{GS}}{-4}$$

$$V_{GS} = 0.3168\times4 = -1.2674$$

$$V_{GS} = -I_{DS}R_s$$

$$R_s = \frac{1.2674}{7\text{mA}} = 181.05\ \Omega.$$

Example 30

A JFET fixed bias configuration has an operating point defined by V_{GSQ} = –2 v and I_{DQ} = 5.625 mA with I_{DSS} = 10 mA and V_P = –8 V. Y_{os} = 40 µs. Determine the value of A_v and R_d.

Solution

$$g_m = \frac{2I_{DSS}}{|v_p|} = \frac{2\times10\text{mA}}{8\text{v}} = 2.5\text{ms}$$

$$g_m = g_{mo}\left(1 - \frac{V_{gsQ}}{V_p}\right) = 2.5 \text{ ms}$$

$$\left(1 - \frac{-2}{-8}\right) = 1.88\text{ms}$$

$$A_v = -g_m R_D = -1.88\text{ms}\times2\text{k}\Omega = -3.76$$

$$R_d = \frac{1}{y_o} = \frac{1}{40\mu\text{s}} = 25\text{k}\,.$$

Example 31

Consider an n-channel depletion-mode MOSFET having the parameters V_{TN} = −1.5 V and K_n = 1 mA/V^2. If V_{GS} = 0 V and V_{DS} = 0.3 V, then I_D is

Solution

$$V_{DS(sat)} = V_{GS} - V_{TN}$$

$$= 0 - (-1.5) = 1.5 \text{ V}.$$

$$V_{DS} < V_{DS(sat)}$$

Biased in non-saturated region

$$I_D = kn\left[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2\right]$$

$$= 1\left[2(0 - -1.5)0.3 - (0.3)^2\right]$$

$$= 1\left[2(1.5)0.3 - (0.3)^2\right]$$

$$= \left[0.9 - 0.09\right] = 0.81\text{mA}\,.$$

Direction for questions 32 and 33:

Consider an n-channel Si JFET with the parameters N_a = 5 × 10^{15}/cm^3, N_d = 10^{18}/cm^3. a = 0.3 µm, L = 6 µm, w = 25 µm, μ_n = 1,000 cm^2/Vs. V_{GS} = 0.

Example 32

The pinch off current I_{D1} is

Solution

$$I_{D1} = \frac{\mu (eNa)^2 wa^3}{6\varepsilon L}$$

$$\frac{1000 \times \left(0.6 \times 10^{-19} \times 5 \times 10^{15}\right)^2 \times 25 \times 10^{-4} \times \left(0.3 \times 10^{-4}\right)^3}{6 \times \left(11.7 \times 8.85 \times 10^{-14} \times 6 \times 10^{-4}\right)}$$

$$= \frac{1000 \times 6.4 \times 10^{-7} \times 6.75 \times 10^{-17}}{3727.62 \times 10^{-18}}$$

$$= \frac{4.32 \times 10^{-20}}{3727.62 \times 10^{-18}} = 1.15 \times 10^{-5} = 0.015 \text{ mA}.$$

Example 33

Maximum drain current $I_{DI(sat)}$ is

Solution

$$I_{D1}(\max) = I_{D1}\left[1 - \frac{3V_{bi}}{V_{po}}\left(1 - \frac{2}{3}\sqrt{\frac{V_{bi}}{V_{po}}}\right)\right]$$

$$V_{po} = \frac{ea^2 Na}{2\varepsilon_o}$$

$$= \frac{\left(1.6 \times 10^{-19}\right)\left(5 \times 10^{15}\right) \times \left(3 \times 10^{-4}\right)^2}{2\left(11.7 \times 8.85 \times 10^{-14}\right)} = 0.347 \text{ V}$$

$$V_{bi} = 0.0259 \ln\left(\frac{\left(5 \times 10^{15} \times 10^{18}\right)}{\left(1.5 \times 10^{10}\right)^2}\right)$$

$$= 0.0259\, \ell n \left(\frac{5 \times 10^{33}}{2.25 \times 10^{20}}\right)$$

$$= 0.0259\, \ell n \left(2.22 \times 10^{13}\right) = 0.79593 \text{ V}$$

$$I_{Di\ \max} = 0.15\left(1 - \left(3 \times \frac{0.795}{0.347}\right)\right)\left(1 - \frac{2}{3}\sqrt{\frac{0.796}{0.347}}\right)$$

$$= 3.2 \text{ mA}.$$

Direction for questions 34 and 35:

An n-channel JFET has a pinch off voltage of −3.5 V and $I_{DSS} = 6$ mA.

Example 34

At what value of V_{GS}, will I_{DS} equal to 2 mA?

Solution

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$V_{GS} = -3.5\left(1 - \sqrt{\frac{2 \times 10^{-3}}{6 \times 10^{-3}}}\right)$$

$$= -3.5\ (0.42264) = -1.4792 \text{ V}.$$

Example 35

Find the value of g_m at this I_{DSS}.

Solution

$$g_m = \frac{-2I_{DSS}}{V_P} \times \left(1 - \frac{V_{GS}}{V_P}\right)$$

$$g_m = \frac{-2 \times 6 \times 10^{-3}}{-3.5}\left(1 - \frac{1.4772}{3.5}\right]$$

$$= \frac{-2 \times 6 \times 10^{-3} \times 0.57737}{-3.5} = 1.97 \text{ ms}.$$

Introduction to IC Technology

The growth of electronics started with invention of vacuum tubes and associated electronic circuits. This activity is termed as vacuum tube electronics; subsequently, the evolution of solid state devices and consequent development of integrated circuits are responsible for the present status of communication, computation, and instrumentation.

Integrated Circuit

It is a circuit where all discrete components such as passive as well as active elements are fabricated on a single crystal chip.

Small-scale Integration (SSI)

The technology was developed by integrating the number of transistors of 1–100 on a single chip. For example, gates, flip-flops, op-amps, etc.

Medium-scale Integration (MSI)

The technology was developed by integrating the number of transistors of 100–1,000 on a single chip. For example, counters, MUX, adders, 4-bit microprocessor, etc.

Large-scale Integration (LSI)

The technology was developed by integrating the number of transistors of 1,000–10,000 on a single chip. For example, 8-bit microprocessor, ROM, RAM, etc.

Very Large-scale Integration (VLSI)

The technology was developed by integrating the number of transistors of 10,000–1 million on a single chip. For example, 16–32 bit microprocessors, peripherals, CMOS technology, etc.

Ultra-scale Integration (ULSI)

Number of transistors on a single chip: 1 million–10 millions. For example, special purpose processors.

Giant-scale Integration (GSI)

The technology was developed by integrating the number of transistors of above 10 millions on a single chip. For example, embedded system and system-on-chip.

Uses of VLSI

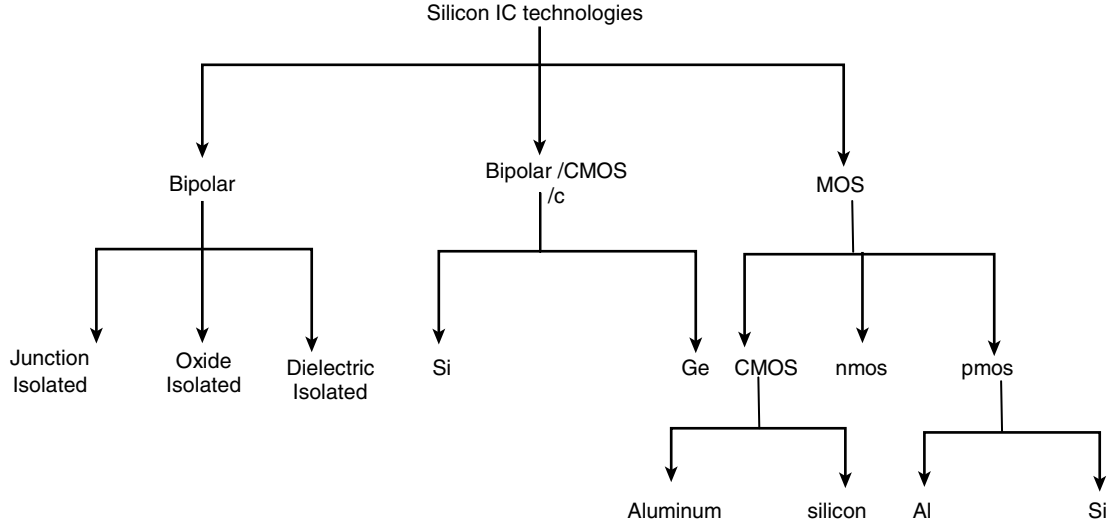
1. Simplicity of operations.
2. Small size
3. Consumes less power than discrete components
4. High reliability
5. High operating speed
6. High productivity and high functionality
7. Design security.
8. Easy to design and manufacture

Applications of VLSI Chips

1. Digital signal processors
2. Wireless LAN
3. Voice and data communication networks
4. Multimedia information system internet
5. Medicine\.

Moore's Law

The number of transistors on a chip is doubled every 18 to 24 months, and Moore also predicted that semiconductor technology will double its effectiveness every 18 months.



Example 36

Thin-gate oxide in a CMOS process is preferably grown using

(A) wet oxidation (B) dry oxidation
(C) epitaxial (D) ion implantation

Solution: (B)

Photolithography

Photolithography is the means by which the following steps are applied to selected areas of the silicon wafer.

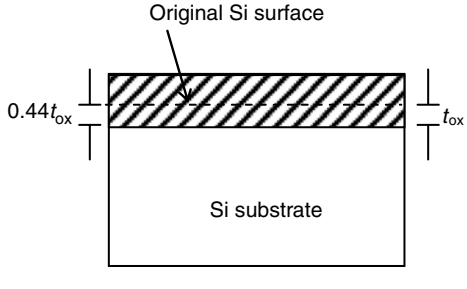
It involves two processes namely making of a photographic mask and photo etching. The making of photographic mask involves the following sequence of operations: first, the preparation of initial artwork, and second, its reduction. The initial layout or artwork is done at a scale of several hundred times larger than the final dimensions of the finished monolithic circuit.

Photo etching is used for the removal of SiO_2 from desired regions so that the desired impurities can be diffused.

Oxidation

Oxidation is the process by which a layer of silicon dioxide is grown on the surface of a silicon wafer. SiO_2 has the property of preventing the diffusion of almost all impurities through it. It serves two very important purposes.

1. SiO_2 has an extremely hard protective coating and it is unaffected by almost all reagents, except hydrofluoric acid.
2. By selective etching of SiO_2, the diffusion of impurities through carefully defined windows in the SiO_2 can be accomplished to fabricate various components.



Uses

1. protect the underlying material forming contamination
2. provide isolation between two layers.
3. very thin oxides (100 A° to 1,000 A°) are grown using dry oxidation techniques, while thick oxides (>1,000 A°) are grown using wet oxidation techniques.

Epitaxial Growth

The basic chemical reaction used for the epitaxial growth of pure silicon is the hydrogen reduction of silicon tetrachloride:

$$SiC_4 + 2H_2 \rightleftharpoons Si + 4HCl$$

Diffusion

Diffusion is the movement of impurity atoms at the surface of the silicon into the bulk of the silicon; further, they always move in the direction from higher concentration to lower concentration.

Diffusion is typically done at high temperatures: 800°C–1,500°C. This uses a high temperature furnace having a flat temperature profile over a useful length. A quartz boat containing about 20 cleaned wafers is pushed into the hot zone with temperature maintained at about a 1,000°C. A carrier gas like dry oxygen is normally used for sweeping the impurity to the high temperature zone.

Ion Implantation

In this process, silicon wafers are placed is a vacuum chamber and are scanned by ions (boron for P-type and accelerated by energies between 20 kV to 250 kV). As the ions strike the silicon wafers, they penetrate some small distance into the wafer.

Ion implantation is the process by which impurity ions are accelerated to a high velocity and physically lodged into the target material.

1. Ion implantation is a lower temperature process when compared to diffusion.
2. Annealing is required to activate the impurity atoms and repair the physical damage to the crystal lattice. This step is done at 500°C–800°C.
3. Thermal annealing is a high temperature process, which
   (a) allows doping impurity to diffuse further into the bulk.
   (b) repairs lattice damage caused by the collisions with doping ions.

Deposition

Deposition is the means by which various materials are deposited on the silicon wafer. For example, silicon triode, Sio_2, aluminium, polysilicon, etc.

Etching

Etching is the process of selectively removing a layer of material. When etching is performed, the etchant may remove portions or all of the following layers:

1. desired material
2. underlying layer
3. making layer

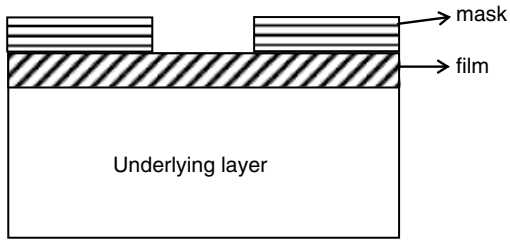


Figure portion of the top layer ready for etching.

There are basically two types of etches:

1. Wet etch that uses chemicals
2. Dry etch that uses chemically active ionized gases.

Isolation Techniques

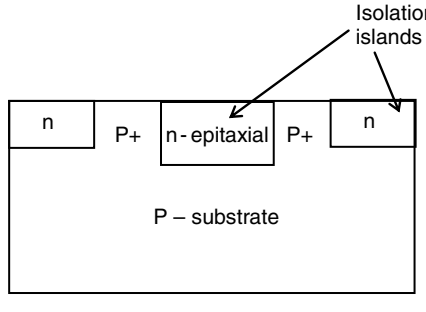
Electrical isolation is provided between different components and interconnections. P–N junction isolation and dielectric isolation are two types of isolation techniques.

Since a number of components are fabricated on the same IC chip, it becomes necessary to provide electrical isolation between different components and interconnections. The commonly used techniques are as follows:

1. P–N junction isolation
2. Dielectric isolation

P–N junction isolation

In this technique, p^+-type impurities are selectively diffused into the n-type epitaxial layer so as to reach P-type substrate, as shown in the figure. This produces islands surrounded by p-type moats. It can be seen that these regions are separated by two back-to-back p–n junction diodes.



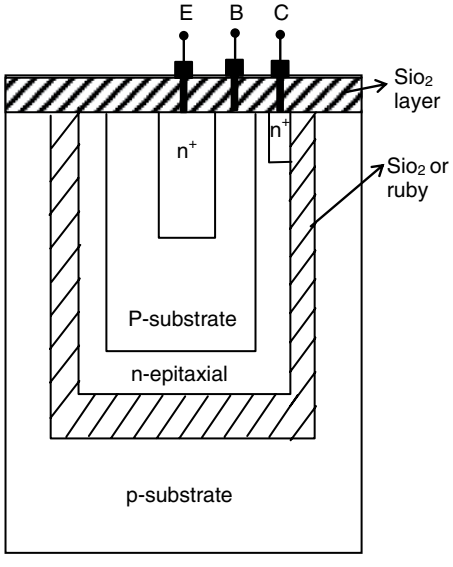
If the p-type substrate material is held at the most negative potential in the circuit, the diodes will be reverse biased providing electric isolation between the islands. The different components are fabricated in these isolation islands.

The concentration of the acceptor atoms in the region between isolation islands is usually kept much higher (P^+) than the p-type substrate; this prevents the depletion region of the reverse biased diode from penetrating more into p^+ region and possibly connecting the isolation islands.

Dielectric Isolation

A layer of solid dielectric such as silicon dioxide or ruby completely surrounds each component, thereby producing isolation, both electrical and physical.

This isolating dielectric layer is thick enough so that its associated capacitance is neglected. It is also possible to fabricate both npn and pnp transistors within the same silicon substrate since this method requires additional fabrication steps. It becomes more expensive.



Dielectric isolation

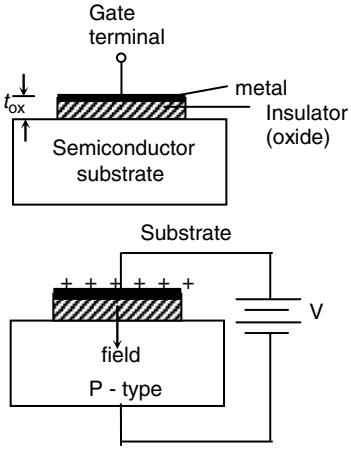
This technique is mostly used for fabricating professional grade ICs required for specialized applications, that is, aerospace and military, where higher cost is justified by superior performance.

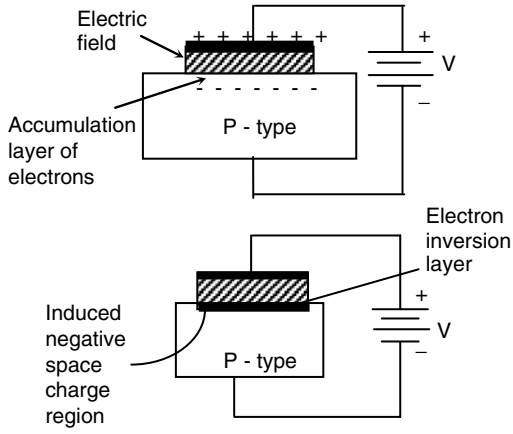
Metallization

The purpose of this process is to produce a thin metal film layer that will serve to make interconnections of the various components on the chip. A film of thickness of about 1 μm and conduction width of about 2–25 μm are commonly used.

MOS Capacitor

The metal–oxide–semiconductor (MOS) capacitor is the heart of the MOSFET. The metal may be aluminium or some other type of metal. In most cases, the metal is replaced by a high-conductivity polycrystalline silicon layer deposited on the oxide.





An MOS capacitor with P-type semiconductor substrate is shown in the figure. The top metal terminal, also known as the gate, is at the positive voltage with respect to the semiconductor substrate.

A positive charge will exist on the top of the metal plate and an electric field will be induced in the direction shown in the figure. If the electric field penetrates the semiconductor, holes in the P-type material will experience a force away from the oxide–semiconductor interface.

As the holes are pushed away from the interface, a negative space charge region is produced because of the fixed capacitor impurity atoms. The negative charge in the induced depletion region corresponds to the negative charge on the bottom plate of the MOS capacitor.

When a larger positive voltage is applied to the gate, the magnitude of the induced electric field increases. Minority carrier electrons are attracted to the oxide–semiconductor. This region of minority carrier electrons is known as electron inversion layer. The magnitude of the charge in the inversion layer is a function of the applied gate voltage.

Example 37

Find the maximum width of the depletion region for an ideal MOS capacitor on P-type Si with $N_a = 10^{16}/cm^3$

Solution

$$W_m = 2\sqrt{\frac{\varepsilon_s \phi_F}{qN_a}}$$

$$\phi_F = \frac{KT}{q}\ln\frac{N_a}{ni}$$

$$= 0.0259 \ln \frac{10^{16}}{1.5\times10^{10}}$$

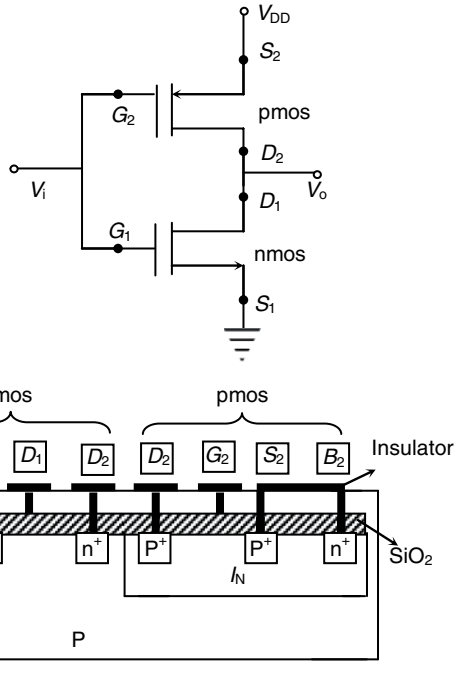
$$= 0.347 \text{ V}$$

$$W_m = 2\left[\frac{(11.8)(8.85\times10^{-14})0.347}{(1.6\times10^{-19})(10^{16})}\right]^{1/2}$$

$$= 3.01 \times 10^{-5} \text{ cm}$$

$$W_m = 0.301 \text{ μm}$$

Complementary MOSFET (CMOS) Fabrication



It is possible to fabricate n-mos and p-mos enhancement devices on the same silicon chip. The gate used is polysilicon gate. An n-type 'well' or 'tub' is diffused into the P-type substrate. The pmos transistor is fabricated within this well.

The n-type region forms the substrate or body B_2 for the pmos transistor. There are two additional steps required in the fabrication of p-mos transistor when compared to nmos transistor, such as the formation of n-region and ion implantation of p-type source and drain regions.

It can be seen that B_1 is tied to S_1 and is connected to the lowest voltage (GND), whereas B_2 is tied to S_2 and held at supply voltage V_{DD}.

Since B_1 is P-type and B_2 is n-type, both the source substrate diodes (B_1–S_1 and B_2–S_2) are reverse biased, and they cut-off. Thus, isolation between nmos and pmos transistor is automatically achieved.

The p-channel transistor has a negative threshold voltage, and the n-channel transistor has a positive threshold voltage. Therefore, a zero input voltage ($V_i = 0$) gives zero gate voltage for the n-channel device, but the voltage between the gate and the source of the p-channel device is $-V$.

Thus, the p-channel device is ON, and the n-channel device is OFF and the full voltage V is measured at V_{out}. Alternatively, a positive value of V_i turns the n-channel device is essentially zero. Thus, the circuit operates as an inverter.

Since the transistor are connected is series, no drain current flows, except for a small charging current during the switching process from one state to the other. Therefore, the power dissipation is very small.

Exercises

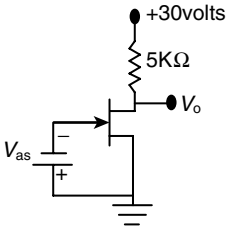
Practice Problems I

Direction for questions 1 to 27: Select the correct alternative from the given choices.

1. Find the resistivity of a p-channel Ge JFET with half channel height of 2 μm and pinch off voltage of 3.94 V. (Consider $\mu_p = 1{,}800\ cm^2/Vs$ $\varepsilon_r = 16$)

(A) 0.02 Ωcm (B) 0.2 Ωcm
(C) 0.02 Ωm (D) 0.2 Ωm

2.



For the given n-channel JFET, $I_{Dss} = 6$ mA and $I_D = 2.5$ mA, when $V_{GS} = -1$ V.

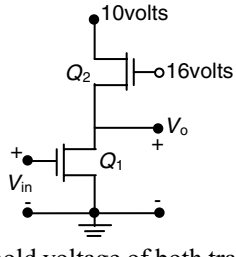
Calculate V_{GS} for a drain current of 3 mA is

(A) –0.71 V (B) –0.79 V
(C) –0.86 V (D) –0.69 V

3. Consider an n-channel silicon JFET with a = 4 μm, W = 120 μm, and L = 6 μm. Find drain to source resistance for $V_{GS} = 0$ V, if channel resistivity is 10 Ωcm.

(A) 425 Ω (B) 625 Ω
(C) 475 Ω (D) 675 Ω

4.



Assume threshold voltage of both transistors is 2 V and $\beta_1 = \beta_2$. Find V_o when $V_{in} = 6$ V.

(A) 5 v (B) 13.25 v (C) 8.35 v (D) 3.25 v

5. Consider an MOSFET with V_T = 0.7 v, W = 8 μm, L = 0.8 μm, and $K = 194\ \mu A/v^2$.

The value of $V_{DS_{min}}$ need to operate the transistor in saturation region with a DC current I_D = 100 μA.

(A) 1.02 v (B) 0.7 v
(C) 0.32 v (D) 1.72 v

6. Consider an MOSFET with V_T = 0.7 V, W = 8 μm, L = 0.8 μm, and K = 194 μA/v^2.

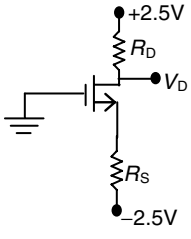
The value of V_{Gs} required to cause the device to operate as a 100-Ω resistor for very small V_{DS}.

(A) 1.02 v (B) 1.2 v (C) 0.52 v (D) 1.52 v

7. An n-mos enhancement transistor with V_T = 0.7 v conducts a current of I_D = 100 μA when V_{GS} = V_{DS} = 1.2 v. Find the value of I_D for V_{Gs} = 1.5 v and V_{DS} = 3 v.

(A) 128 μA (B) 100 μA
(C) 256 μA (D) 200 μA

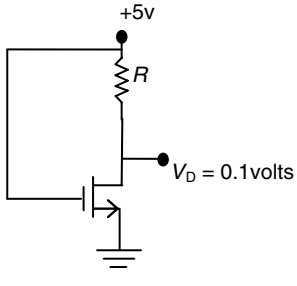
8.



Assume V_T = 1 v, K = 60 μA/V^2 and $\frac{W}{L}=\frac{120}{3}$. Find the value of R_S and R_D so that the transistor operates at I_D = 0.3 mA and V_D = 0.4 V.

(A) 7 kΩ and 3.3 kΩ (B) 3.3 kΩ and 7 kΩ
(C) 5 kΩ and 3.3 kΩ (D) 3.3 kΩ and 5 kΩ

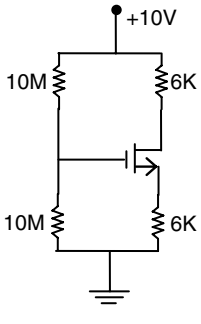
9.



Assume V_T = 1 V and $K.\frac{W}{L}=1\,\text{mA/V}^2$. Find the value of R to obtain a drain voltage of 0.1 V.

(A) 11.4 kΩ (B) 12.4 kΩ
(C) 10.5 kΩ (D) 9.6 kΩ

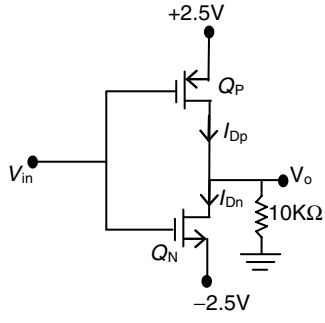
10.



Let V_T = 1 V, $K.\frac{W}{L}=1\,\text{mA/V}^2$. Find the region of operation and drain current.

(A) Active, 0.89 mA (B) saturation, 0.89 mA
(C) Active, 0.5 mA (D) saturation, 0.5 mA

11.



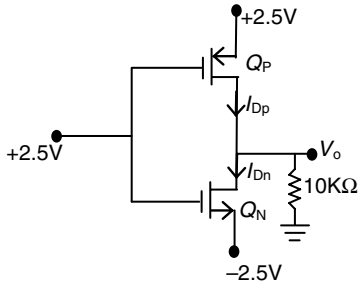
Assume both n-mos and p-mos has same

$K.\frac{W}{L}=1\,\text{mA/V}^2$ and $V_{t_n}=-V_{t_p}=1V$.

Find I_{DN} and I_{DP} when V_{in} = 0 volts.

(A) 1.125 mA, 0 mA (B) 0 mA, 1.125 mA
(C) 1.125 mA, 1.125 mA (D) 0 mA, 0 mA

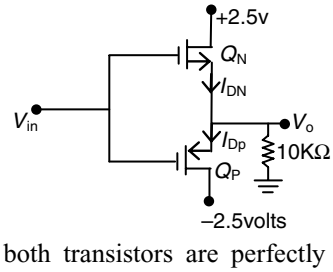
12.



Assume V_T = 1 volts, $K.\frac{W}{L}=1\,\text{mA/V}^2$ for both. Find V_o when V_{in} = + 2.5 volts.

(A) –2.44 volts (B) + 2.44 volts
(C) 5 volts (D) 0 volts

13.



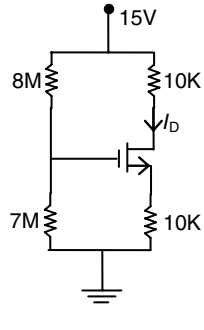
Assume both transistors are perfectly matched with

$K.\frac{W}{L}=1\text{mA/v}^2$ *and* $V_{t_n}=-V_{t_p}=1\text{volt}$.

Find V_o when V_{in} = + 2.5 v.

(A) –1.04 V (B) +1.0 4 V
(C) 0 V (D) +2.5 V

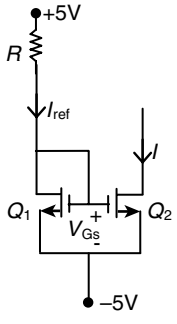
14.



Assume the MOSFET has V_T = 1 volt and $K.\frac{W}{L}=1\,\text{mA/V}^2$. If the current flowing is I_D = 0.5 mA initially, calculate the percent change in the value of I_D when the MOSFET is replaced with another having same $K.\frac{W}{L}$ but $V_T = 1.5$ volts.

(A) decreases by 9% (B) increases by 9%
(C) remains same (D) none of the above

15.



Assume V_T = 1 volt, $K.\left(\frac{W}{L}\right)_1 = 0.8\,\text{mA/V}^2$ and two transistors Q_1 and Q_2 having equal length but widths related by $W_2 = 5\ W_1$. Find the value of R to obtain $I = 0.5$ mA.

(A) 45 kΩ (B) 85 kΩ
(C) 65 kΩ (D) 55 kΩ

16. For a CMOS inverter with matched MOSFETS having $V_{t_n} = -V_{t_p} = 1\text{volt}$ and $V_{DD} = 5\text{volts}$
Find noise margin for high level.

(A) 2.1 volts (B) 2.5 volts
(C) 2.9 volts (D) 2 volts

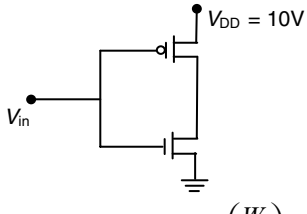
17. For a CMOS inverter with matched MOSFETS having, $V_{t_n} = -V_{t_p} = 1\text{volt}$ and $V_{DD} = 5\text{volts}$ find noise margin for low level.

(A) 2.1 v (B) 2.9 v (C) 2.5 v (D) 2 v

18. A 1.2 μm CMOS inverter uses $L_n = L_p = 1.2$ μm, $W_n = 1.8$ μm, $k_n = 80\ \mu\text{A/V}^2$, $k_p = 27\ \mu\text{A/V}^2$, $V_{t_n} = 0.8$ volts, and $V_{DD} = 5$ v. Calculate the value of output resistance of the inverter, when $V_o = V_{oL}$.

(A) 1 kΩ (B) 1.5 kΩ (C) 2 kΩ (D) 3 kΩ

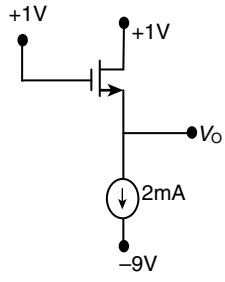
19.



Assume $V_{t_n} = -V_{t_p} = 2\text{volts}, \left(\frac{W}{L}\right)_n = 20, \left(\frac{W}{L}\right)_p = 40$ and $\mu_n C_{ox} = 2\ \mu_p C_{ox} = 20\ \mu\text{A/v}^2$. Find the peak current drawn from V_{DD} during switching.

(A) 1.2 mA (B) 1.8 mA
(C) 0.8 mA (D) 1.6 mA

20.



Assume $V_t = +1$ V, $K.\left(\frac{W}{L}\right) = 1\,\text{mA/V}^2$. Find V_o for the circuit shown.

(A) +2 V (B) −2 V (C) −9 V (D) +1 V

Direction for questions 21 and 22:
For a depletion-mode n-mos transistor with $V_t = -2$ V and $K\left(\frac{W}{L}\right) = 2\,\text{mA/V}^2$.

21. Find the minimum V_{DS} required to operate in the saturation region when $V_{gs} = +1$ V

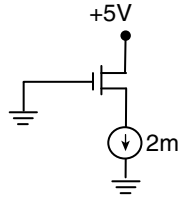
(A) −1 V (B) +1 V (C) 2 V (D) 3 V

22. For a depletion-mode nmos transistor with $V_t = -2$ V and $K\left(\frac{W}{L}\right) = 2\,\text{mA/V}^2$.

The value of drain current I_D, when V_{gs} = +1 V is

(A) 3 mA (B) 6 mA (C) 7.5 mA (D) 9 mA

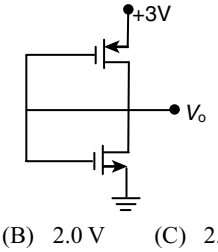
23.



For the depletion-mode MOSFET, assumeand $K\left(\frac{W}{L}\right) = 4\,\text{mA/V}^2$ and $V_t = -2$ V. Find the voltage across the source terminal.

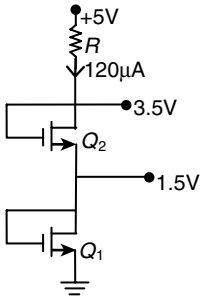
(A) −1 V (B) +1 V (C) −3 V (D) +3 V

24. Assume k_P = 2.5 μA/V², k_n = 10 μA/V², $|V_t|$ = 1 V, L = 10 μm, and W = 30 μm. Find the output voltage V_o, as shown in the following figure.



(A) 4.1 V (B) 2.0 V (C) 2.8 V (D) 4.2 V

25.

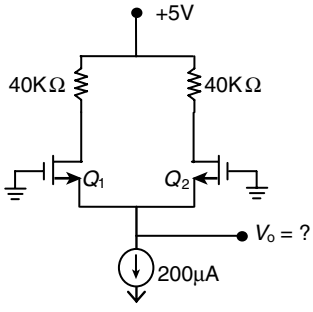


Assume each n-mos transistor has $V_t = 1$ V, $K = 120$ μA/V^2, and $L_1 = L_2 = 1$ μm.

Find the value of gate width of Q_2.

(A) 8 μm (B) 4 μm (C) 2 μm (D) 1 μm

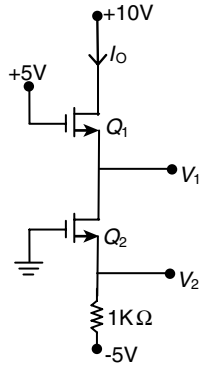
26.



Assume both transistors have $V_t = 1$ V, $K = 100$ μA/V^2, and $\frac{W}{L} = 20$. Find the value of V_o indicated.

(A) 1.32 v (B) 1.68 v
(C) −1.32 v (D) −1.68 v

27. Assume each transistor has $V_t = 1$ V, and $K.\frac{W}{L} = 2\,\text{mA/V}^2$. Find the current flowing through drain of Q_1.



(A) 1.23 mA (B) 2.44 mA
(C) 1.48 mA (D) 2.65 mA

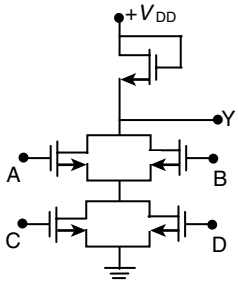
Practice Problems 2

Direction for questions 1 to 18: Select the correct alternative from the given choices.

1. Find the pinch off voltage of a silicon n-channel JFET with half channel height of 2 μm and donor concentration of 7×10^{14} atoms/cm^3

(A) 3.1 v (B) 4.1 v (C) 2.1 v (D) 1.1 v

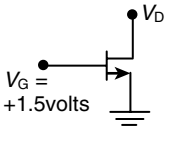
2. The logic function realized by the given circuit is _____



(A) $\overline{(A+C)(B+D)}$ (B) $\overline{(A+C)}+\overline{(B+D)}$

(C) $\overline{(A+B)}+\overline{(C+D)}$ (D) $\overline{A+B+C+D}$

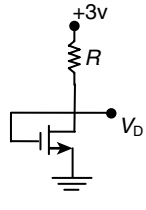
3.



For the given nmos enhancement with $K = 100$ μA/v^2, $W = 10$ μm, $L = 1$ μm, and $V_T = 0.7$ v. Find the region of operation and drain current when $V_D = 0.9$ v.

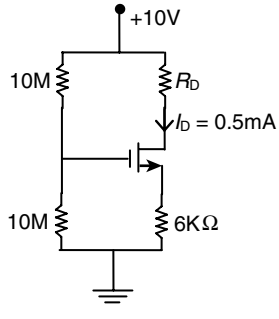
(A) Triode region, 275 μA
(B) saturation, 320 μA
(C) Triode, 320 μA
(D) saturation, 275 μA

4. Find the value of aspect ratio (W/L) and R to obtain drain current of 160 μA and V_{DS} of 1 v.
Assume $V_T = 0.6$ v
$K = 200$ μA/V^2



(A) 8 and 25 kΩ (B) 10 and 25 kΩ
(C) 10 and 12.5 kΩ (D) 8 and 12.5 kΩ

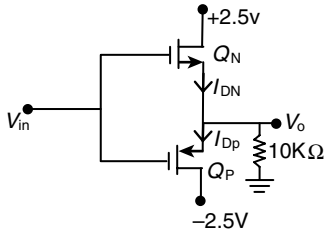
5.



Let V_T = 1 volt and $K.\frac{W}{L}=1\text{mA}/\text{V}^2$. Find the largest value that R_D can have, while the transistor remains in saturation with 0.5 mA of drain current.

(A) 8 kΩ (B) 10 kΩ (C) 12 kΩ (D) 16 kΩ

6.

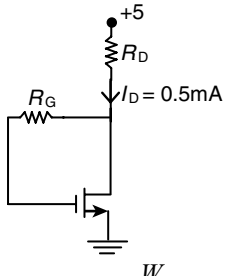


Assume both transistors are perfectly matched with $K.\frac{W}{L}=1\text{mA}/\text{V}^2$ and $V_{t_n}=V_{t_p}=1\text{V}$

Find I_{D_N} and I_{D_P} when $V_{in}=0$ volts.

(A) 0 mA, 0 mA
(B) 0 mA, 0.104 mA
(C) 0.104 mA, 0 mA
(D) 0.104 mA, 0.104 mA

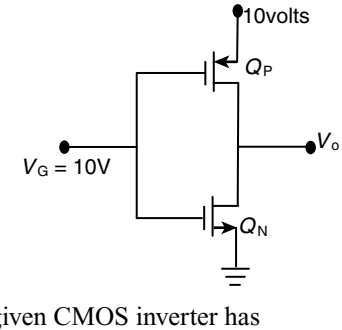
7.



Assume V_T = 1 volt, $K.\frac{W}{L}=1\text{mA}/\text{v}^2$. Find the value of R_D.

(A) 3 kΩ (B) 6 kΩ (C) 9 kΩ (D) 7.5 kΩ

8.



The given CMOS inverter has

$V_{t_n}=-V_{t_p}=2\text{ volts},\left(W/L\right)_p=40,\left(W/L\right)_n=20,$

$\mu_n C_{ox}=20\ \mu\text{A/V}^2$.

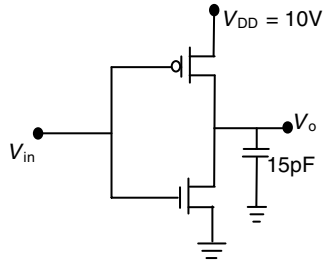
Find the maximum current that the inverter can sink, while V_O = 0.5 v.

(A) 0 mA (B) 1.25 mA
(C) 1.55 mA (D) 1.75 mA

9. A 1.2 µm CMOS inverter uses $L_p = L_n$ = 1.2 µm and W_N = 1.8 µm. Find the value of W_p that would result in Q_N and Q_P being matched. Assume K_n = 80 µA/V², K_P = 27 µA/V², V_{t_n} = 0.8 volts V_{t_n} = 0.8 volts, and V_{DD} = 5 v.

(A) 1.8 µm (B) 3.6 µm
(C) 5.4 µm (D) 7.2 µm

Direction for questions 10 and 11:



Assume $V_{t_n}=-V_{t_p}=2\text{V},\left(\frac{W}{L}\right)_n=20;\left(\frac{W}{L}\right)_p=40,\ K_n=2\ k_p$ = 20 µA/V².

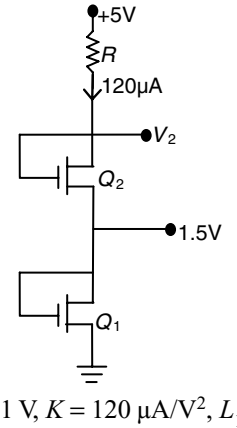
10. Find the dynamic power dissipation, when the inverter is switched at a frequency of 2 MHz.

(A) 3 mW (B) 30 mW
(C) 6 mW (D) 15 mW

11. Average current drawn from the power supply is _____

(A) 0.3 mA (B) 0.6 mA
(C) 3 mA (D) 30 mA

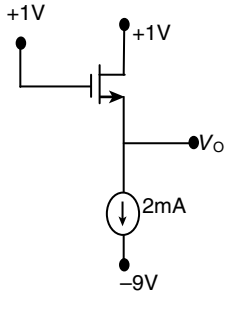
12.



Assume V_t = 1 V, K = 120 µA/V², $L_1 = L_2$ = 1 µm, W_1 = 8 µm, and W_2 = 2 µm. Find the value of R indicated.

(A) 25 kΩ (B) 12.5 kΩ
(C) 1.25 kΩ (D) 2.5 kΩ

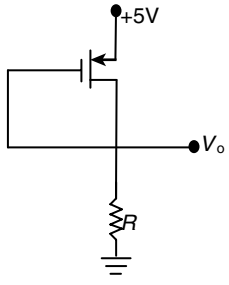
13.



Assume $V_t = +1$ V $K.\left(\frac{W}{L}\right) = 1\,\text{mA/V}^2$. Find V_o for the circuit shown.

(A) +2 V (B) −2 V (C) −9 V (D) +1 V

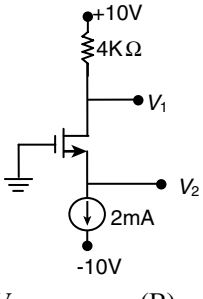
14.



For the pmos transistor, assume $V_t = -0.7$ volts, $K_P = 60$ μA/V^2, and $L = 0.8$ μm. Find the value of W in order to establish a drain current of 115 μA and a voltage V_D of 3.5 v.

(A) 0.8 μm (B) 2.4 μm (C) 4.8 μm (D) 3.6 μm

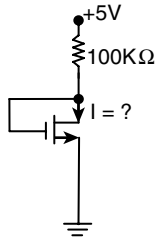
15. Assume $V_t = 2$ V, $K.\frac{W}{L} = 1\,\text{mA/V}^2$. Find V_1 and V_2 labelled as shown in the following figure.



(A) 2 V and 4 V (B) –2 V and −4 V
(C) 2 V and –4 V (D) –2 V and 4 V

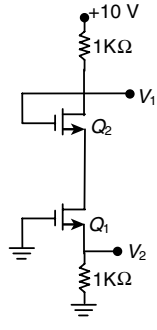
16. Assume $V_t = 1$ volt, $K.\left(\frac{W}{L}\right) = 0.4\,\text{mA/V}^2$.

Find the value of drain current.



(A) 0.024 mA (B) 0.036 mA
(C) 0.048 mA (D) 0.072 mA

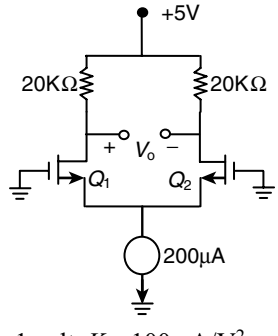
17.



Assume each nmos has $V_t = 1$ V and $K.\frac{W}{L} = 2\,\text{mA/V}^2$. Find the voltage V_1 shown in figure.

(A) 5.71 V (B) 6.25 V (C) 2.52 V (D) 5.23 V

18.

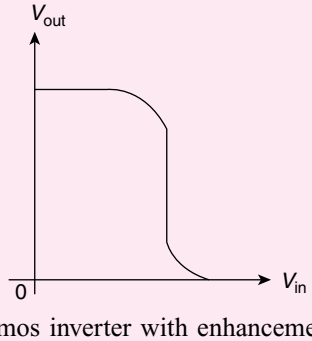


Assume $V_t = 1$ volt, $K = 100$ μA/V^2, and $W/L = 10$. Find the value of V_o as shown in the figure.

(A) 1 V (B) 3 V (C) 2 V (D) 0 V

Previous Years' Questions

1. Given figure is the voltage transfer characteristic of **[2004]**



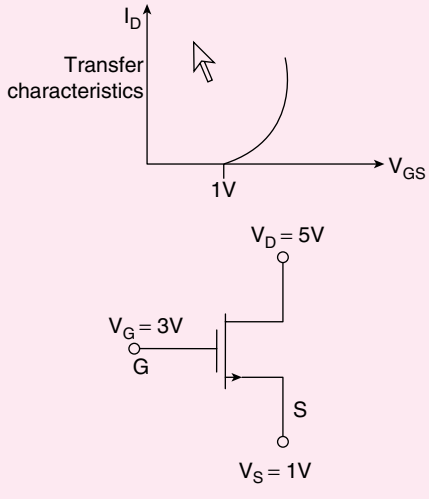
(A) an nmos inverter with enhancement-mode transistors as load
(B) an n-moS inverter with depletion-mode transistor as load
(C) a CMOS inverter
(D) a BJT inverter

2. Consider the following statements S_1 and S_2.
S_1: The threshold voltage (V_T) of an MOS capacitor decreases with an increase in gate oxide thickness.
S_2: The threshold voltage (V_T) of MOS capacitor decreases with an increase in substrate doping concentration.
Which one of the following is correct? **[2004]**
(A) S_1 is false and S_2 is true
(B) Both S_1 and S_2 are true
(C) S_1 is true and S_2 is false
(D) Both S_1 and S_2 are false

3. The drain of an n-channel MOSFET is shorted to the gate so that $V_{GS} = V_{DS}$. The threshold voltage (V_T) of MOSFET is 1 V. If the drain current (I_D) is 1 mA for $V_{GS} = 2$ V, then for $V_{GS} = 3$ V, I_D is **[2004]**

(A) 2 mA (B) 3 mA
(C) 9 mA (D) 4 mA

4. For an n-channel MOSFET and its transfer curve shown in the figure, the threshold voltage is **[2005]**



(A) 1 V and the device is in active region
(B) –1 V and the device is in saturation region
(C) 1 V and the device is in saturation region
(D) –1 V and the device is in active region

5. An MOS capacitor made using p-type substrate is in the accumulation mode. The dominant charge in the channel is due to the presence of **[2005]**

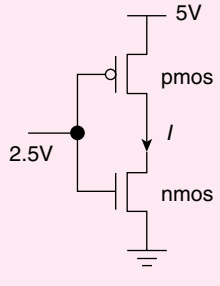
(A) holes
(B) electrons
(C) positively charged ions
(D) negatively charged ions

6. In the CMOS inverter circuit shown, if the transconductance parameters of the n-mos and p-mos transistors are k_n =

$$k_P = \mu_n C_{ox} \frac{W_n}{L_n} = \mu_P C_{ox} \frac{W_p}{L_p} = 40\ \mu A/V^2$$

and their threshold voltages are

$V_{THn} = |V_{TH_p}| = 1$, the current I is



[2007]

(A) 0 A (B) 25 µA
(C) 45 µA (D) 90 µA

7. The gate oxide thickness in the MOS capacitor is **[2007]**

(A) 50 nm (B) 143 nm
(C) 350 nm (D) 1 µm

8. The maximum depletion layer width in silicon is **[2007]**

(A) 0.143 µm (B) 0.857 µm
(C) 1 µm (D) 1.143 µm

9. Consider the following statement about the *C–V* characteristic plot:

S_1: The MOS capacitor has an n-type substrate

S_2: If positive charges are introduced in the oxide, the *C–V* plot will shift to the left,

Then, which of the following is true? **[2007]**

(A) Both S_1 and S_2 are true
(B) S_1 is true and S_2 is false
(C) S_1 is false and S_2 is true
(D) Both S_1 and S_2 are false

10. A silicon wafer has 100 nm of oxide on it and is inserted in a furnace at a temperature above 1,000°C for further oxidation in dry oxygen. The oxidation rate **[2008]**

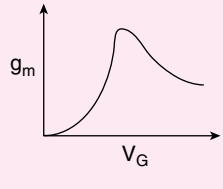
(A) is independent of current oxide thickness and temperature
(B) is independent of current oxide thickness but depends on temperature
(C) slows down as the oxide grows
(D) is zero as the existing oxide prevents further oxidation

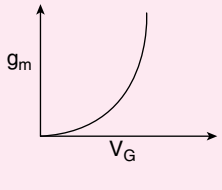
11. The drain current of an MOSFET in saturation is given by $I_D = K(V_{GS} - V_T)^2$, where K is a constant. The magnitude of the transconductance g_m is **[2008]**

(A) $\frac{K(V_{GS} - V_T)^2}{V_{DS}}$ (B) $2\,K(V_{GS} - V_T)$

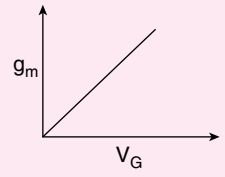
(C) $\frac{I_D}{V_{GS} - V_{DS}}$ (D) $\frac{K(V_{GS} - V_T)^2}{V_{GS}}$

12. The measured transconductance g_m of an n-mos transistor operating in the linear region is plotted against the gate voltage V_G at constant drain voltage V_D. Which of the following figures represent the expected dependence of g_m on V_G? **[2008]**

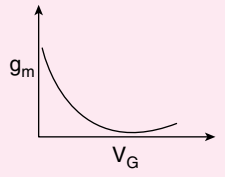
(A) 

(B) 

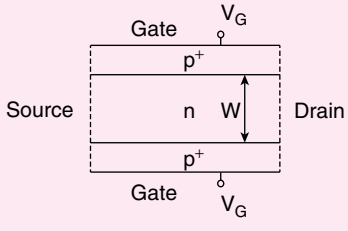
(C)



(D)



13. The cross-section of a JFET is shown in the following figure. Let V_G be −2 V and let V_p be the initial pinch off voltage. If the width W is doubled (with other geometrical parameters and doping levels remaining the same), then the ratio between the mutual transconductances of the initial and the modified JFET is **[2008]**



(A) 4

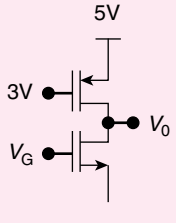
(B) $\frac{1}{2}\left(\frac{1-\sqrt{2/V_p}}{1-\sqrt{1/(2V_p)}}\right)$

(C) $\frac{1-\sqrt{2/V_p}}{1-\sqrt{1/(2V_p)}}$

(D) $\frac{1-(2/\sqrt{V_p})}{1-(1/2\sqrt{V_p})}$

Direction for questions 14 and 15:

Consider the CMOS circuit shown, where the gate voltage V_G of the n-MOSFET is increased from zero, while the gate voltage of the p-MOSFET is kept constant at 3 V. Assume that, for both transistors, the magnitude of the threshold voltage is 1 V and the product of the transconductance parameter and the (W/L) ratio, that is, the quantity μC_{ox} (W/L) is 1 mAV^{-2}.



14. For small increase in V_G beyond 1 V, which of the following gives the correct description of the region of operation of each MOSFET? **[2009]**

(A) Both the MOSFETs are in saturation region

(B) Both the MOSFETs are in triode region

(C) n-MOSFET is in triode and p-MOSFET is in saturation region

(D) n-MOSFET is in saturation and p-MOSFET is in triode region

15. Estimate the output voltage V_0 for V_G = 1.5 V. [Hint: use the appropriate current–voltage equation for each MOSFET, based on the answer to Q. 57.] **[2009]**

(A) $4-\frac{1}{\sqrt{2}}V$

(B) $4+\frac{1}{\sqrt{2}}V$

(C) $4-\frac{\sqrt{3}}{2}V$

(D) $4+\frac{\sqrt{3}}{2}V$

16. Thin gate oxide in a CMOS process in preferably grown using **[2010]**

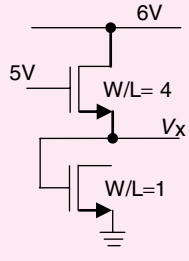
(A) wet oxidation

(B) dry oxidation

(C) epitaxial deposition

(D) ion implantation

17. In the following circuit, for the MOS transistors, $\mu_n C_{ox}$ = 100 μA/V^2 and the threshold voltage V_T = 1 V. The voltage V_x at the source of the upper transistor is **[2011]**



(A) 1 V

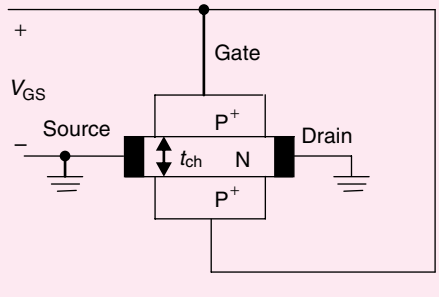
(B) 2 V

(C) 3 V

(D) 3.67 V

Direction for questions 18 and 19:

The channel resistance of an n-channel JFET shown in the following figure is 600 Ω. When the full channel thickness (t_{ch}) of 10 μm is available for conduction, the built-in voltage of the gate P$^+$–N junction (V_{bi}) is −1 V. When the gate–source voltage (V_{GS}) is 0 V, the channel is depleted by 1 μm on each side due to the built-in voltage, and hence, the thickness available for conduction is only 8 μm.



18. The channel resistance when V_{GS} = 0 V is **[2011]**

(A) 480 Ω

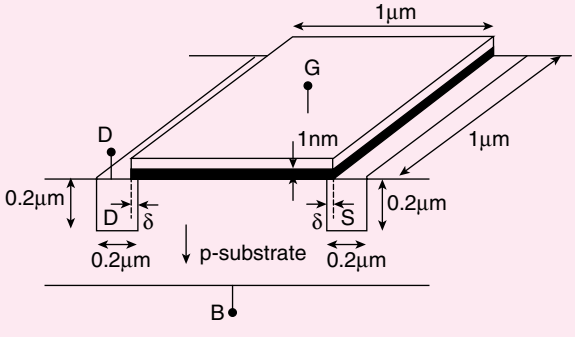
(B) 600 Ω

(C) 750 Ω

(D) 1,000 Ω

19. The channel resistance when $V_{GS} = -3$ V is **[2011]**
(A) 360 Ω (B) 917 Ω
(C) 1,000 Ω (D) 3,000 Ω

Direction for questions 20 and 21:
In the three-dimensional view of a silicon n-channel MOS transistor, as shown in the following figure, $\delta = 20$ nm. The transistor is of width 1 μm. The depletion width formed at every p–n junction is 10 nm. The relative permittivities of Si and SiO_2, respectively, are 11.7 and 3.9, and $\varepsilon_0 = 8.9 \times 10^{-12}$ F/m.



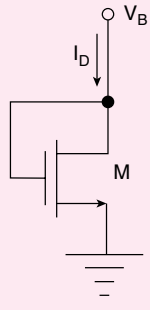
20. The gate–source overlap capacitance is approximately **[2012]**
(A) 0.7 fF (B) 0.7 PF
(C) 0.35 fF (D) 0.24 pF

21. The source–body junction capacitance is approximately **[2012]**
(A) 2 fF (B) 7 fF
(C) 2 pF (D) 7 pF

22. In IC technology, dry oxidation (using dry oxygen) as compared to wet oxidation (using steam or water vapour) produces **[2013]**
(A) superior quality oxide with a higher growth rate
(B) inferior quality oxide with a higher growth rate
(C) inferior quality oxide with a lower growth rate
(D) superior quality oxide with a lower growth rate

23. In an MOSFET operating in the saturation region, the channel length modulation effect causes **[2013]**
(A) an increase in the gate–source capacitance
(B) a decrease in the transconductance
(C) a decrease in the unity-gain cut-off frequency
(D) a decrease in the output resistance

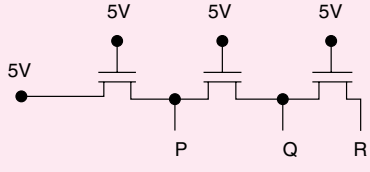
24. The small-signal resistance (i.e., dV_B/dI_D) in kΩ offered by the n-channel MOSFET M shown in the following figure at a bias point of $V_B = 2$ V is (device data for M device transconductance parameter $k_N = \mu_n C'_{ox}(W/L) = 40\mu A/V^2$, threshold voltage $V_{TN} = 1$ V, and neglect body effect and channel length modulation effects) **[2013]**



(A) 12.5 (B) 25 (C) 50 (D) 100

25. If fixed positive charges are present in the gate oxide of an n-channel enhancement type MOSFET, it will lead to **[2014]**
(A) a decrease in the threshold voltage
(B) channel length modulation
(C) an increase in substrate leakage current
(D) an increase in accumulation capacitance

26. In the following circuit employing pass transistor logic, all n-mos transistors are identical with a threshold voltage of 1 V. Ignoring the body effect, the output voltages at P, Q, and R are **[2014]**



(A) 4 V, 3 V, 2 V (B) 5 V, 5 V, 5 V
(C) 4 V, 4 V, 4 V (D) 5 V, 4 V, 3 V

27. A depletion type n-channel MOSFET is biased in its linear region for use as a voltage controlled resistor. Assume threshold voltage $V_{TH} = -0.5$ V, $V_{GS} = 2.0$ V, $V_{DS} = 5$ V, $W/L = 100$, $C_{ox} = 10^{-8}$ F/cm^2, and $\mu_n = 800$ cm^2/Vs. The value of the resistance of the voltage controlled resistor (in Ω) is _____. **[2014]**

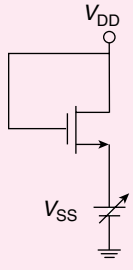
28. In CMOS technology, shallow P-well or N-well regions can be formed using **[2014]**
(A) low pressure chemical vapour deposition
(B) low energy sputtering
(C) low temperature dry oxidation
(D) low energy ion implantation

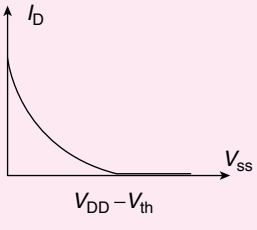
29. In MOSFET fabrication, the channel length is defined during the process of **[2014]**
(A) isolation oxide growth
(B) channel stop implantation
(C) poly-silicon gate patterning
(D) lithography step leading to the contact pads

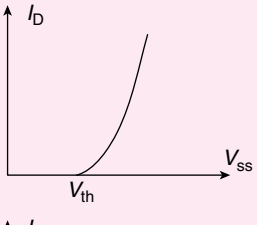
30. The slope of I_D versus V_{GS} curve of an n-channel MOSFET in linear regime is 10^{-3} Ω^{-1} at $V_{DS} = 0.1$ V. For the same device, neglecting channel length modulation, the slope of $\sqrt{I_D}$ versus V_{GS} curve (in $\sqrt{A}/V$) under saturation regime is approximately _____. **[2014]**

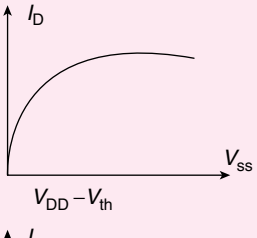
31. An ideal MOS capacitor has boron doping concentration of 10^{15} cm^{-3} in the substrate. When a gate voltage is applied, a depletion region of width 0.5 μm is formed with a surface (channel) potential of 0.2 V. Given that $\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm and the relative permittivities of silicon and silicon dioxide are 12 and 4, respectively, the peak electric field (in V/μm) in the oxide region is_____

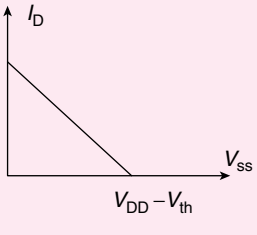
32. For the MOSFET in the circuit shown, the threshold voltage is V_{th}, where $V_{th} > 0$. The source V_{SS} is varied from 0 to V_{DD}. Neglecting the channel length modulation, the drain current I_D as a function of V_{SS} is represented by **[2015]**



(A)


(B)


(C)


(D)


33. In MOS capacitor with an oxide layer thickness of 10 nm, the maximum depletion layer thickness is 100 nm. The permittivities of the semiconductor and the oxide layer are ε_s and ε_{ox}, respectively. Assuming $\varepsilon_s/\varepsilon_{ox} = 3$, the ratio of the maximum capacitance to the minimum capacitance of this MOS capacitor is _____. **[2015]**

34. Which one of the following processes is preferred to form the gate dielectric (SiO_2) of MOSFETs? **[2015]**
(A) Sputtering
(B) Molecular beam epitaxy
(C) Wet oxidation
(D) Dry oxidation

35. The current in an enhancement mode NMOS transistor biased in saturation mode was measured to be 1 mA at a drain-source of 5 V. when the drain-source voltage was increased to 6 V while keeping gate-source voltage same, the drain current increased to 1.02 mA. Assume that drain to source saturation voltage is much smaller than the applied drain-source voltage. The channel length modulation parameter λ (in V^{-1}) is _____. **[2015]**

36. Consider the following statements for a metal oxide semiconductor field effect transistor (MOSFET): **[2016]**

P: As channel length reduces, OFF state current increases.
Q: As channel length reduces, output resistance increases.
R: As channel length reduces, threshold voltage remains constant.
S: As channel length reduces, ON current increase.

Which of the above statements are INCORRECT?
(A) P and Q (B) P and S
(C) Q and R (D) R and S

37. Consider an n-channel metal oxide semiconductor field effect transistor (MOSFET) with a gate to source voltage of 1.8 V. Assume that $\frac{W}{L} = 4$, $\mu_n C_{ox} = 70 \times 10^{-6}$ AV^{-2}, the threshold voltage is 0.3V, and the channel length modulation parameter is $0.09V^{-1}$. In the saturation region, the drain conductance (in micro Seimens) is _____ . **[2016]**

38. A long channel NMOS transistor is biased in the linear region with $V_{DS} = 50$ mV and is used as a resistance. Which one of the following statements is NOT correct? **[2016]**
(A) If the device width W is increased, the resistance decreases.
(B) If the threshold voltage is reduced, the resistance decreases.
(C) If the device length L is increased, the resistance increases.
(D) If V_{GS} is increased, the resistance increases.

39. A voltage V_G is applied across a MOS capacitor with metal gate and p type silicon substrate at $T = 300$k. The inversion carrier density (in number of carriers per unit area) for $V_G = 0.8$V is 2×10^{11} cm^{-2}. For $V_G =$ 1.3 V, the inversion carrier density is 4×10^{11} cm^{-2}. What is the value of the inversion carrier density for $V_G = 1.8$ V? **[2016]**

(A) 4.5×10^{11}cm^{-2}
(B) 6.0×10^{11} cm^{-2}
(C) 7.2×10^{11}cm^{-2}
(D) 8.4×10^{11}cm^{-2}

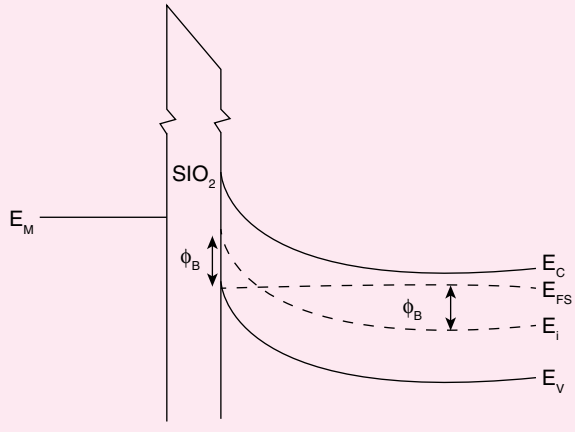
40. Consider a long channel NMOS transistor with source and body connected together. Assume that the electron mobility is independent of V_{GS} and V_{DS}. Given,

$g_m = 0.5\ \mu$ A/V for $V_{DS} = 50$m V and $V_{GS} = 2$V,
$g_d = 8\ \mu$ A/V for $V_{GS} = 2$V and $V_{DS} = 0$ V,

Where $g_m = \dfrac{\partial I_D}{\partial V_{GS}}$ and $g_d = \dfrac{\partial I_D}{\partial V_{DS}}$.

The threshold voltage (in volts) of the transistor is _____. **[2016]**

41. The figure shows the band diagram of a Metal Oxide Semiconductor (MOS). The surface region of this MOS is in: **[2016]**



(A) Inversion (B) Accumulation
(C) Depletion (D) Flat band

42. Figure I and II show two MOS capacitors of unit area. The capacitor in Figure I has insulator materials X(of thickness $t_1 = 1$ nm and dielectric constant $e_1 = 4$) and Y(of thickness $t_2 = 3$ nm and dielectric constant $e_2 = 20$). The capacitor in figure II has only insulator material X of thickness t_{Eq}. If the capacitors are of equal capacitance, then the value of t_{Eq}(in nm) is _____. **[2016]**

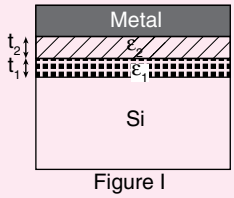


Figure I

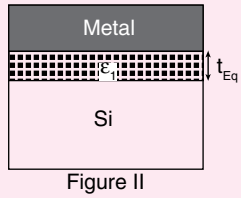


Figure II

Answer Keys

Exercises

Practice Problems 1

1. A	**2.** A	**3.** B	**4.** C	**5.** C	**6.** B	**7.** C	**8.** B	**9.** B	**10.** D
11. C	**12.** A	**13.** B	**14.** A	**15.** B	**16.** A	**17.** A	**18.** C	**19.** B	**20.** B
21. D	**22.** D	**23.** B	**24.** B	**25.** C	**26.** C	**27.** B			

Practice Problems 2

1. C	**2.** C	**3.** B	**4.** C	**5.** C	**6.** A	**7.** B	**8.** C	**9.** C	**10.** A
11. A	**12.** B	**13.** B	**14.** C	**15.** C	**16.** B	**17.** B	**18.** D		

Previous Years' Questions

1. C	**2.** D	**3.** D	**4.** C	**5.** A	**6.** D	**7.** A	**8.** C	**9.** D	**10.** D
11. B	**12.** A	**13.** C	**14.** D	**15.** D	**16.** B	**17.** C	**18.** C	**19.** C	**20.** A
21. A	**22.** D	**23.** D	**24.** B	**25.** A	**26.** C	**27.** 499 to 501		**28.** D	**29.** C
30. 0.0707		**31.** 2.4 V/μm		**32.** A	**33.** 4.33	**34.** D	**35.** 0.022 V^{-1}		**36.** C
37. 28.35×10^{-6} ℧		**38.** D		**39.** B	**40.** 1.2 Volts		**41.** A		
42. 1.6 nm									