Registers

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Shift Registers (SRs)

- Registers are used to store group of bits.
- In register to store N-bit, it requires N flip-flop.
- In shift register each CLK pulse shifts the contents of register one-bit position to the RIGHT or LEFT.
- The "serial input" determines what goes into the left most FF during the shift.
- Depending upon input and output registers can be classified into 4 types.:
  (a) SISO: Serial In Serial Out
  (b) SIPO: Serial In Parallel Out
  (c) PISO: Parallel In Serial Out
  (d) PIPO: Parallel In Parallel Out

SISO (Serial In Serial Out)

4-bit Right-Shift SISO Register

- In right shift SISO register, LSB data is applied at the MSB FF'(D-FF).
- In 'n' bit register, to enter 'n' bit data, it requires 'n' clock pulses in serial form.
- If 'n' bit data is stored in SISO register then output is taken serially for this it required (n – 1) clock pulse.
- SISO register is used to provide 'n' clock pulse delay to the input data.
- If 'T' is the time period of clock pulse, then delay provided by SISO is nT.

4-bit Left-Shift SISO Register

- In this above SISO register MSB data is applied to the LSB FF(D-FF).
- To enter the 'n' bit data in serial form we required 'n' clock pulse.
- To exit or getting output of 'n' bit data as serially we required (n – 1) clock pulse.

SIPO (Serial In Parallel Out)

- For 'n' bit- serial input data to be stored the number of CLK pulse required = n.
- For 'n' bit-parallel output data to be stored the number of CLK pulse required = 0 (there is no need of CLK pulse).

PISO (Parallel In Serial Out)

- To store parallel in data, if we store 'n' bit then the number of CLK pulse required = 1 CLK pulse.
- To store serial out data if we store 'n' bit then the number of CLK pulse required = (n – 1).

Note:

To convert temporal code into spacial code, we use SIPO register. Where as to convert spacial code into temporal code we use PISO register.

PIPO (Parallel In Parallel Out)

- For parallel in data, the number of CLK pulse required = 1 CLK pulse.
- For parallel out data, the number of CLK pulse required = 0 CLK pulse.

Remember:

- All SRs are JK-FFs.
- "PIPO" register is a storage register made up with D-FFs.
- "PIPO" register is not a SR.
- A universal register can perform
  (i) Shift left/Shift right
  (ii) Parallel in/Serial in
  (iii) Parallel out/Serial out in a single register.
- If 'n' shift left operation perform then data will be multiply by 2^n times.
- If 'n' shift right operation perform then data will be divided by 2^n times.

Time delay

A SISO SRs may be used to introduce time delay "Δt" in digital signals

$$\Delta t = N \times T = N \times \frac{1}{f_c}$$

where, N = Number of FFs
T = Time period of CLK pulse
f_C = CLK frequency

- The amount of delay can be controlled by the "f_c" or number of FFs in the SR.

Note:

In terms of Speed: PIPO > PISO > SIPO > SISO

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