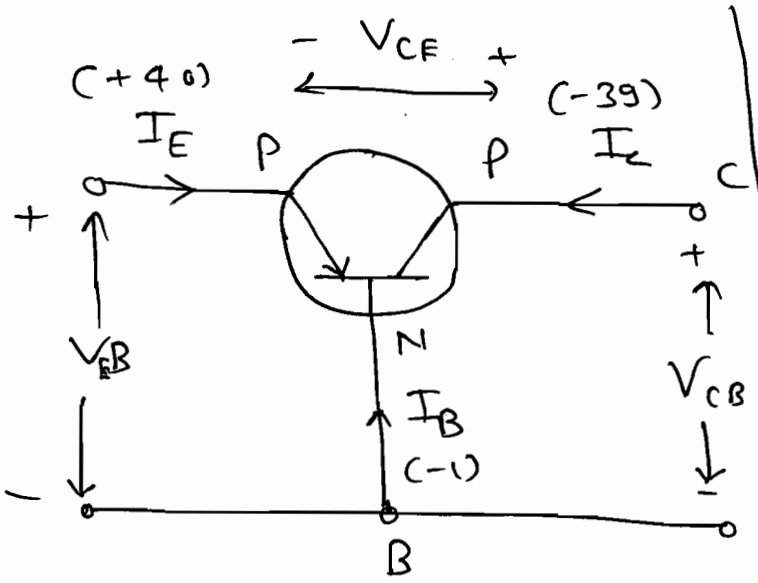
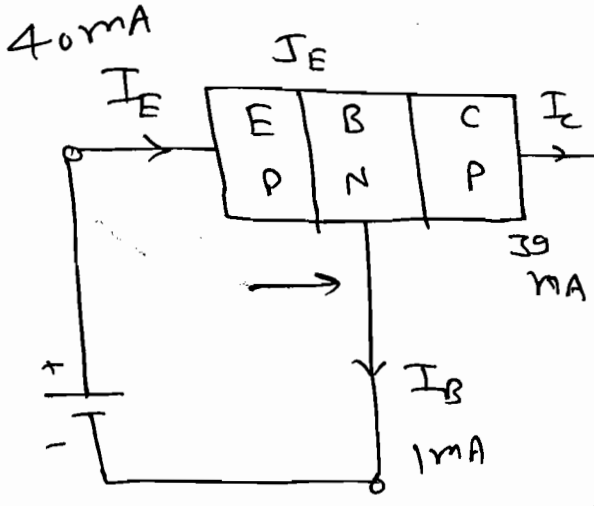
☆ Bipolar Junction Transistor :-

⇒ BJT is a 3 - terminal device found in 1947 at Bell laboratories by Barttain, Brutain and Sikely.

⇒ In the ckt symbol, perpedicular line represents base. out of the two angular line one with arrow represents emitter. The other without arrow represents Collector. The direction of arrow shows the direction of flow of current when emitter jn is FB.

⇒





⇒ KCL:

$$I_E + I_B + I_C = 0.$$

KVL:

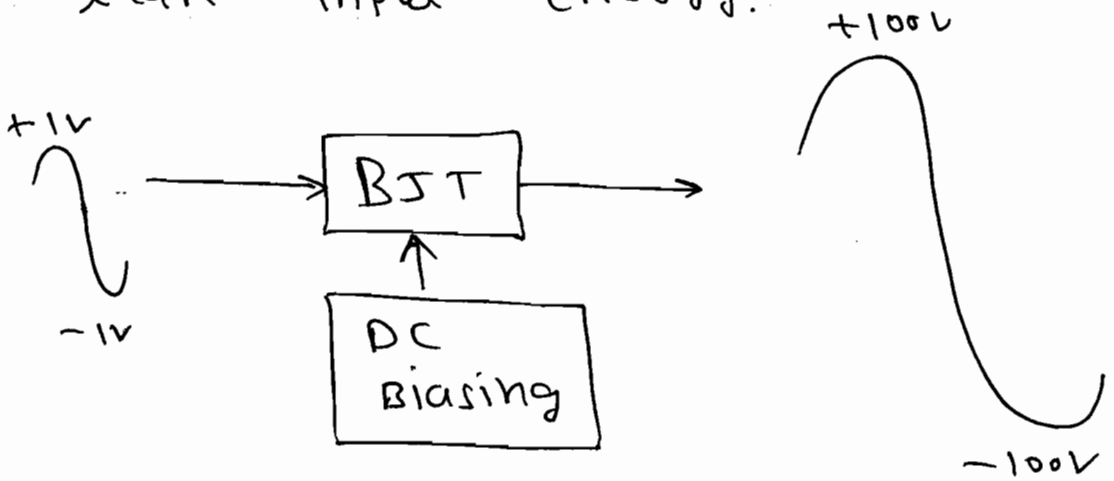
$$V_{CB} = V_{CE} + V_{EB}.$$

→ It has application like, switch, phase shifter, amplifier & oscillator.

⇒ A device is said to be giving amplification service if the following two conditions are satisfied.

① Output should be an exact replica of input.

② Output energy should be greater than input energy.



* Current Components in Common base Configuration:

① $I_E = I_{pE} + I_{nE} \simeq I_{pE}$.

② $-I_{Co} = I_{CBO} = I_{pCo} + I_{nCo}$.

③ $I_C = |-I_{pC1}| + I_{CBO}$.

④ $I_C = |-\alpha I_E| + I_{CBO}$.

⑤ $\alpha = -\dfrac{(I_C - I_{CBO})}{(I_E - 0)} = \dfrac{I_{pC1}}{I_E}$.

⑥ $\alpha_{dc} = -(I_C / I_E)$.

⑦ $\gamma^* = (I_{pE} / I_E) \simeq 1$.

⑧ $\beta^* = (I_{pC1} / I_{pE}) \simeq 1$.

⑨ $\alpha = \beta^* . \gamma^* = (I_{pC1} / I_E) \simeq 1$.

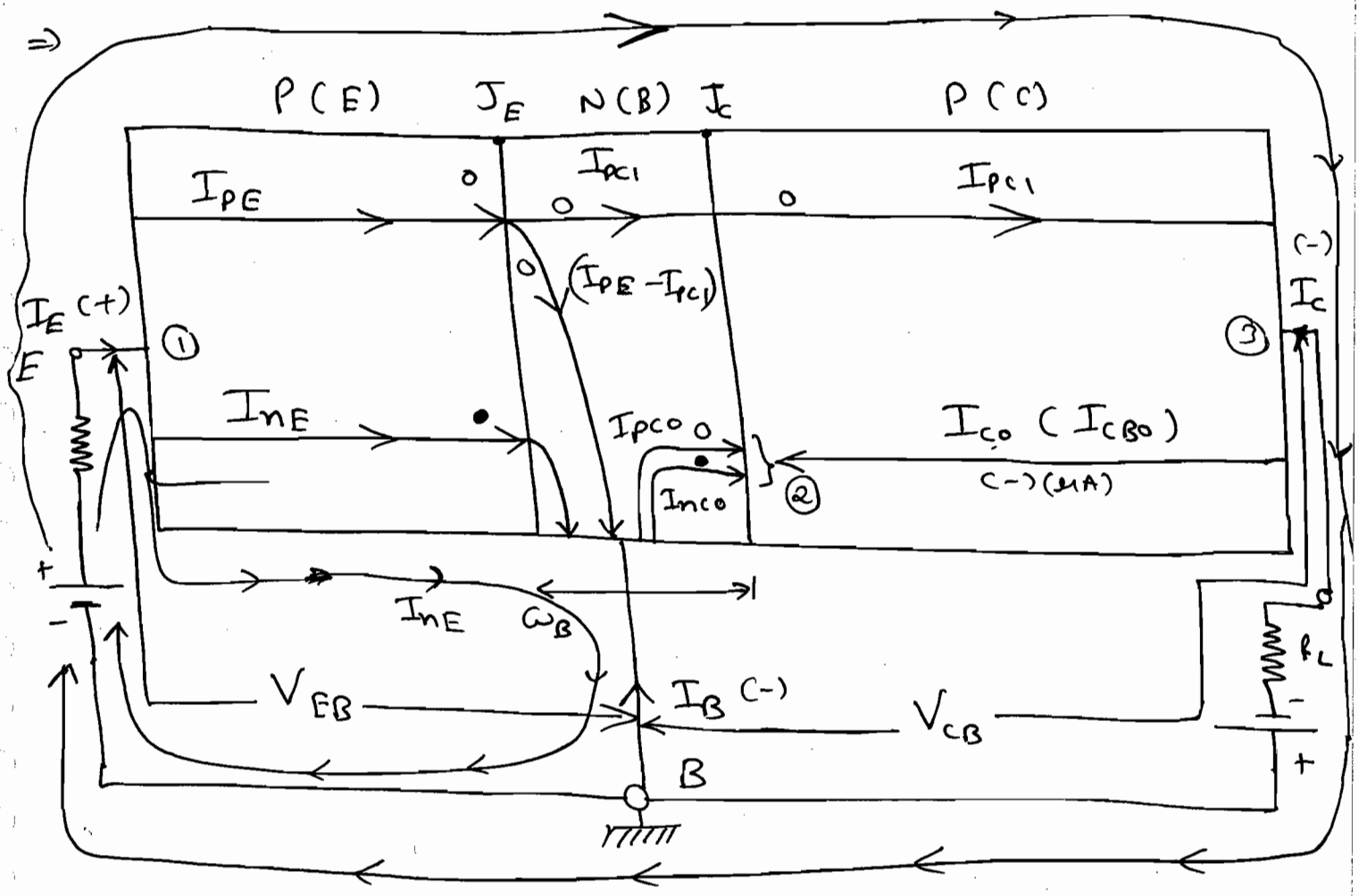
$\Rightarrow$

	E	B	C
Doping	Heavy	Less	Moderate
width	Moderate	Thin	Large

① $W_B (1\mu m) << L_p (100\mu m)$

② $N_D \downarrow\downarrow$

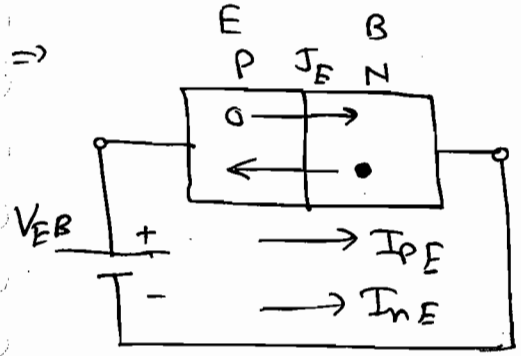
$\rightarrow I_{pC1} \simeq I_{pE}$

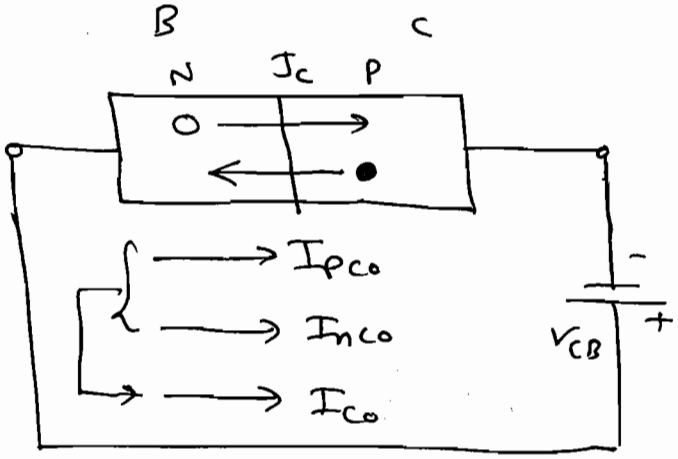


⇒

J_E	J_c	R ∞ (Region of operation)	App.
FB	FB	Saturation	ON switch
RB	RB	Cut - off	OFF switch
FB	RB	Normal Active	Amplifier
RB	FB	Inverse Active	Attenuator

⇒





⇒ J_E is forward bias hence I_{pE} & I_{nE} flow from P to N.

→ I_{pE} is made up of holes out of which few holes recombine in base and go out-of base ($I_{pE} - I_{pc_1}$). Rest of them reach collector (I_{pc_1}).

⇒ J_C is Reverse biased hence I_{pco} & I_{nco} flow from n to p.

→ I_{co}, I_o at J_C flows from N to P but shown P to N hence -ve.

$$I_{CBO} = I_{co} + I_{SL} + I_{AM}$$

→ I_{co} : Current due to thermaly generated minority carriers.

I_{SL} : Current due to surface leakage.

I_{AM} : Current due to avalanch multiplication.

→ By applying KCL at points ①, ② & ③ we get eqn's ①, ② & ③.

→ For the device to act as amplifier load current I_C to be large hence I_{PC_1} to be large. Hence I_{PE} to be large. Hence I_E to be large

→ As input current I_E increases I_{PE}, I_{PC_1} and output current I_C increases hence it is current controlled device.

→ To make I_{PC_1} approximately I_{PE} recombination of holes in base to be decreased for which two conditions are proposed:

① W_B made very much less than L_P.

→ A hole travelles L_P distance before recombination by then it crosses base and enters collector.

② Doping of base is decrease. Hence availability of e^- in base decreases hence hole recombining probability decreases hence hole reaching collector probability increases.

→ A hole in collector is majority carrier hence recombination prob. is less. and it being +very charge gets attracted by -ve supply of collector. hence passes through load.

⇒ I_E is made of I_{pE} and I_{nE}. out of which only I_{pE} flows through load hence to make $I_{pE} >> I_{nE}$ emitter doping heavy dopped.

⇒ Base Current I_B is made up of the following components.

① electron enters into base through base terminal for recombination.

② electrons enter into base through base terminal to give I_{nE} component.

③ electrons leave the base through base terminal to give I_{nCo} component

⇒ I_{pC1} is approximately I_{pE} and I_{pE} approximately I_E hence $I_{pC1} \simeq I_E$.

Hence I_{pC1} replaced by αI_E where

$\alpha < 1$ and closed to 1 $\alpha = 0.95$ to 0.995

Hence eqn - ③ becomes ④.

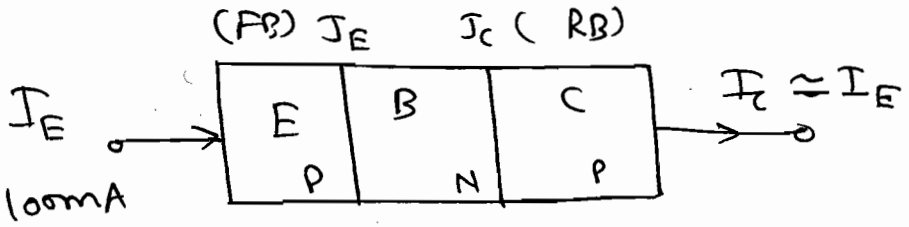
→ From - ③ & ④ we get ⑤ where α is common base forward current transfer ratio (or) CB current gain.

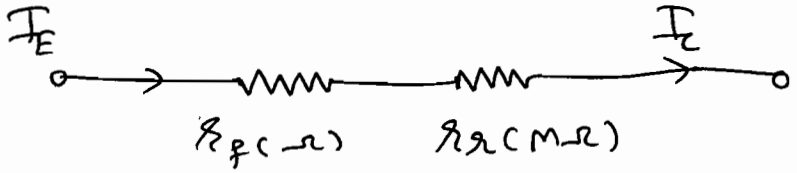
→ In eqn - ⑤ neglecting I_{CBO} we get ⑥.

⇒ γ^* : emitter efficiency (or) emitter injection efficiency.

β^* : Transport factor (or) base Transport factor.

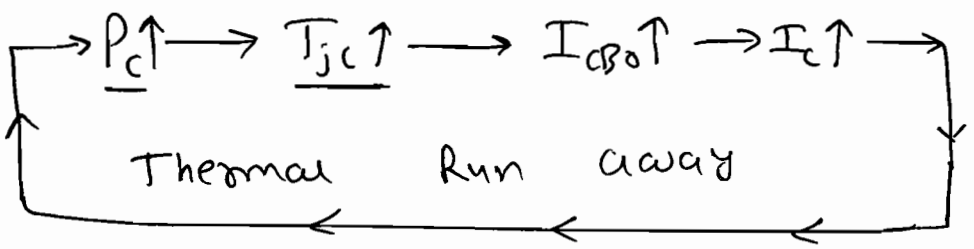
⇒





⇒ $P_C (I_C^2 R_R) > P_E (I_E^2 . R_f)$

$P_C \downarrow = (I_C \downarrow)^2 . R_R$



$\left(\frac{P_c}{(\text{Area}) \uparrow}\right) \downarrow$

⇒ over at collector junction P_c is large. hence Collector jn T_{jc} increases. hence I_{CBO} increases. hence I_c increases. hence P_c increases. which an itterative process due to which at some time excessive power (or) Temp. occurs at Collector jn and transistors burns away called thermal run-away.

⇒ To safe guard the Transistor, Collector made large in size & hence power per unit area ~~decreases~~ at J_c decreases.

⇒ Base thin implies thinner than L_p followed by thinner than emitter and Collector

⇒ $$A_V = \frac{V_o}{V_i} = R_f \cdot \frac{I_C \cdot R_L}{I_E \cdot R_f} > 1 \qquad (\because R_L = M\Omega, \; R_f = \Omega).$$

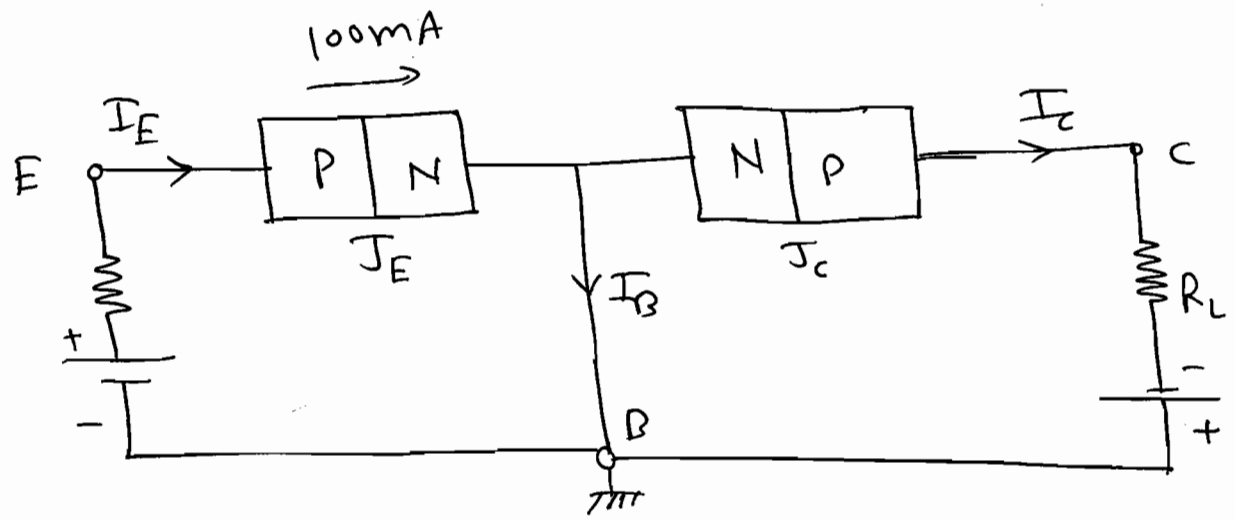
$\therefore A_I = \frac{I_C}{I_E} < 1.$

	A_V	A_I
CB →	✓	×
CE →	✓	✓
CC →	×	✓

* Two P-N Diode connected back to back Series can not act as Transistor (Amplifier):

Imp Concept

⇒



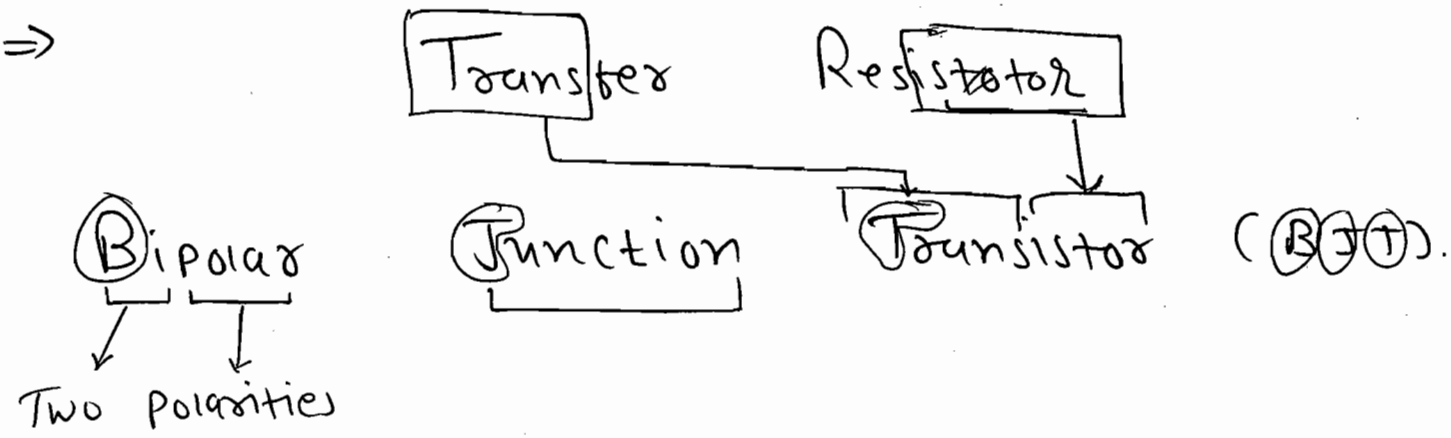
⇒ By making base thin in size and less dopped recombination of holes in base is not allowed hence large current I_E is forcebly transfer from Low resistance (J_E, FB) to high resistance (J_C, RB). Hence, Tra Transfer Resistor Property is exhibited. ~~exhibited~~

⇒ Two Polarities of charge carriers are crossing junctions to give current in device which is exhibiting transfer

resistor property.

→ Hence called <u>Bipolar Junction Transistor (BJT).</u>

⇒



* Early Effect (or) Base width Modulation: (or) Base narrowing:

⇒ W_B: Physical (or) Metarilgcal Base width.

W_B': Effective (or) undepleted Base width.

W_d: Width of depletion region.

⇒ J_E is FB hence width of depletion region & ions of depletion region decreases. hence V_o decreases by V_{EB}.

The applied forward bias J_C is reversed bias hence width of depletion region and ions of depletion region increases hence V_o increases by V_{CB},

the applied reverse biased.

⇒

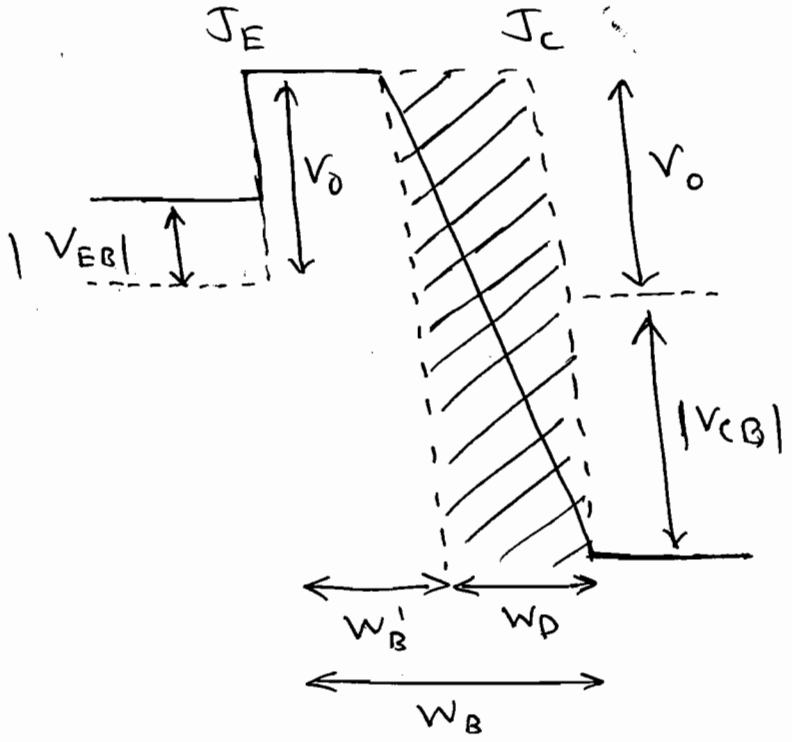


Fig- ①

⇒

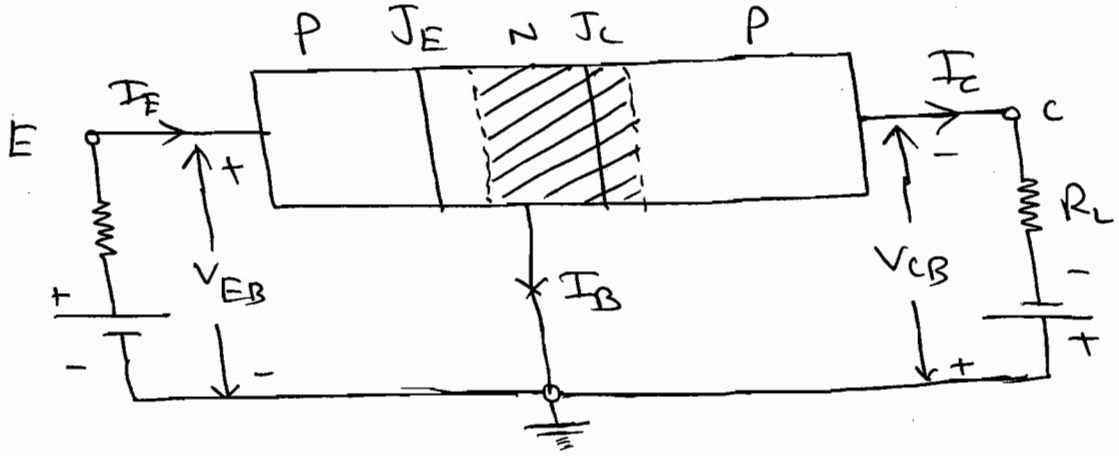


Fig- ②

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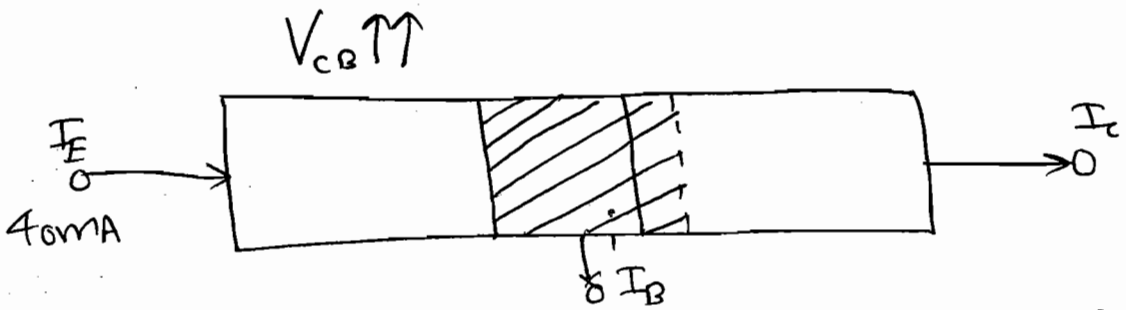


Fig- ③

⇒ Early effect No. ①:

⇒ As reverse bias to J_c increases width of depletion region at J_c and penetration of depletion region into base increases. Hence undepleted width W_B' decreases hence charge carriers which where sitting in a width of W_B earlier will now get confined to a smaller width of W_B' hence concentration gradient increases. J_E is forward bias hence majority carrier diffusion supports currents where diffusion is proportional to concentration gradient which is increasing hence I_E increases.

⇒ $$I = \left[-q D_p \left(\frac{dP}{(dx)\downarrow} \right) \uparrow \right] \uparrow$$

⇒ Early effect No. ②:

⇒ As reverse Bias J_c increases more & more width of depletion region & penetration of depletion region increases more and more. Hence W_B' decreases more and more. earlier with a width

of $W_B < L_p$ available for recombination, recombination was less. Now with a width of W_B' very much less than L_p available for recombination, recombination further decreases. Hence, I_B decreases, I_E increases and hence α increases.

⇒ Early effect No. -③:

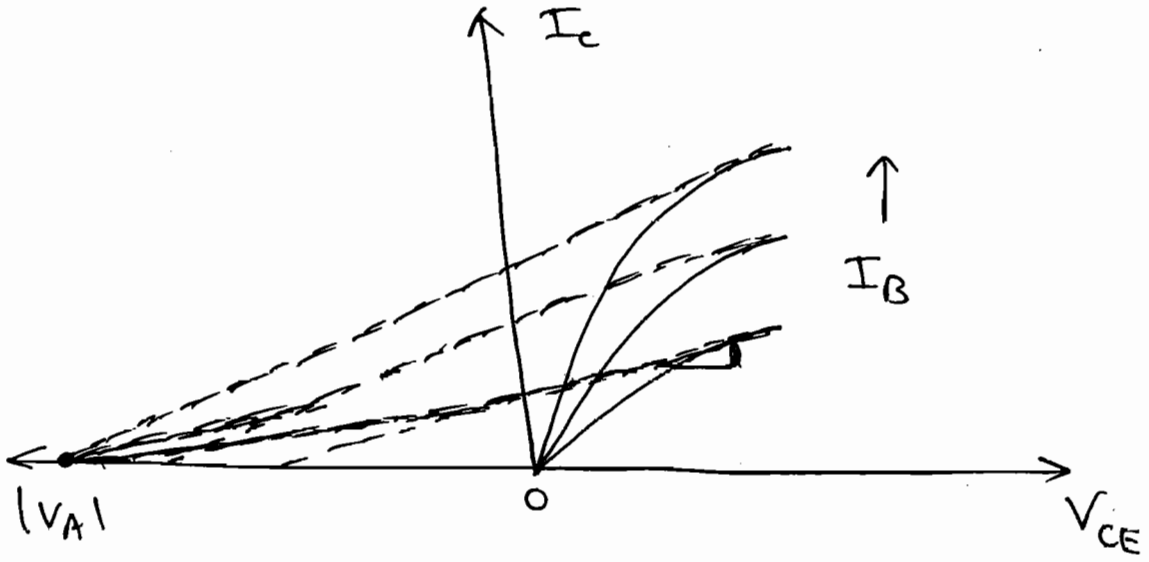
⇒ At large reverse bias to J_C width of depletion region increases and completly fills the base hence undepleted width W_B' and I_B become zero hence transistor can not act as amplifier i.e. Usefullness of Transistor as amplifier is terminated. Earlier depletion region was combined to J_C Now it is has reached J_E hence called punch through (or) reach through.

⇒ The above three effects where observed by J.M. Early. Hence called early effect.

→ out of W_B only W_B' is useful for recombination hence called effective base width.

→ Change in V_{CB} changes W_B' hence called base width modulation. as V_{CB} increases W_B' decreases hence called base narrowing.

⇒



⇒

$$r_o = \frac{|V_A|}{I_c}$$

$$I_c = \alpha I_o \cdot e^{V_{BE}/nV_T} \left(1 + \frac{V_{CE}}{V_A}\right).$$

r_o: Output resistance.

V_A: Early Voltage.

* Avalanch Breakdown:

⇒ As reverse biased to J_c increases more and more, at a perticular Voltage J_c undergoes avalanch BD hence avalanch multipiication starts hence Charge Carriers and I_c increases uncontrollably hence again usefulness gets terminated. this time due to avalanch BD and earier due to punch through.

⇒ **CB**:

$$M = \frac{1}{\left[1 - \left(\frac{V_{CB}}{BV_{CBo}}\right)^n\right]} \qquad n = 2 \text{ to } 10$$

CE: $BV_{CEO} = BV_{CBo}\left(\frac{1}{\beta}\right)^{1/n}$.

$$\text{Max-Rating} = \text{MIN}\ (BV_{PT}, BV_{AB}).$$

⇒ M: Multipiication factor due to avalanch Multipiication.

BV_{CBO}: Break down Voltage in CB. with

emitter open. is defined as reverse bias at J_c in CB at which avalanch BD occurs.

→ **BV_{CEO}** : Break Down Voltage in CE with Base open is defined as RB at J_c in CE at which avalanch BD occurs.

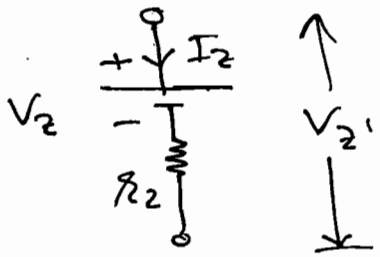
→ **BV_{PT}** : Break Down Voltage at which punch through occurs. It is independent of configuration.

→ **BV_{AB}** : Break Down Voltage at which avalanch Break Down occurs.

→ **Max_Rating** :- maximum rating is defined as maximum reverse bias that can be safely applied across J_c.

Q A zener diode has a eqn resistance of 20 Ω in BD given voltage across zener diode is 5.2V at $I_z = 1mA$. Determine voltage across diode at $I_z = 10mA$.

Soln:



$V_z' = V_z + I_z \cdot R_z$.

$5.2 = V_z + (1mA)(20)$

$V_z = 5.18V$.

at $I_z = 10mA$

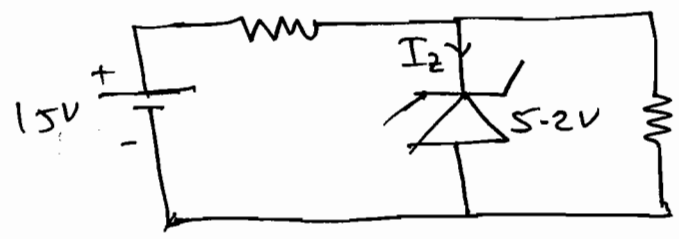
$\therefore V_z' = 5.18 + (10mA)(20)$

$\therefore \boxed{V_z' = 5.38V}$

Note:

⇒ If current through zener diode changes voltage across zener diode changes due to change in drop across R_z. But V_z and R_z or are constant.

The maximum rating of Zener diode shown in ckt is 260 mW it maintains a constant voltage if current through zener diode doesn't fall below 90% of max. permisible current find the range of I_z. for zener diode to act as regulator. safely.



Soln: $260\ mW = P_{z(max)} = V_z \times I_{z(max)}$ (5.2V)

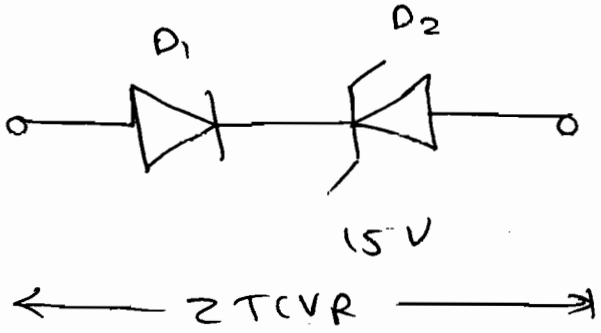
$\boxed{I_{z(max)} = 50mA}$

90 % of $I_{Z(max)}$ = 45 mA = $I_{Z(min)}$.

↓

50mA

Q In the given CKt temp. coefficient of D_1 is $-1.7\ mV/^\circ C$. The series combination is used to construct a zero temp. coefficient voltage reference. (ZTCVR) find in $\%/^\circ C$ the required temp. coefficient of D_2.



Soln:

Note: A ZTCVR should maintain constant voltage irrespective of fluctuation in temperature.

D_2: $+1.7 \times 10^{-3} \frac{V}{^\circ C} \times \frac{100}{15} = +0.01133\ \%/^\circ C$.

Q For a BJT $\beta = 100$ collector junction BD voltage in common base with Emitter open = 120 V. Assuming empirical constant as 3, calculate collector I_n

BD Voltage in CE in with base open.

Soln:

$$BV_{CEO} = BV_{CBO}\left(\frac{1}{\beta}\right)^{1/n}$$

($BV_{CBO} \downarrow 120V$, $\beta \downarrow 100$)

$$BV_{CEO} = 120 \times \left(\frac{1}{100}\right)^{1/3}.$$

$$\boxed{BV_{CEO} = 25.85\ V}$$

Imp:

Q for BJT $I_c = 1mA$ at $V_{CE} = 1V$. given early voltage as 75 V. Calculate I_c at $V_{CE} = 10V$. assume α as constant.

Soln:

$$I_c = \underbrace{\alpha I_0 \cdot e^{V_{BE}/nV_T}}_{x}\left(1 + \frac{V_{CE}}{V_A}\right).$$

$$\therefore \frac{I_c'}{1mA} = \frac{\cancel{x}\left(1 + \frac{10}{75}\right)}{\cancel{x}\left(1 + \frac{1}{75}\right)}.$$

$$\therefore I_c' = \frac{85}{76}\ mA.$$

$$\therefore \boxed{I_c' = 1.118mA.}$$

Q Find o/p R of BJT given early voltage as 150V and collector current 0.1 mA.

Soln:

$$r_o = \frac{|V_A|}{I_c} = 1.5\ M\Omega$$

Q A Ge PNP transistor is biased in active region given diffusion current at Emitter jn as 0.298mA. Calculate dynamic emitter Resistance.

Soln:

$$r_E = \frac{\eta V_T}{I_E}$$

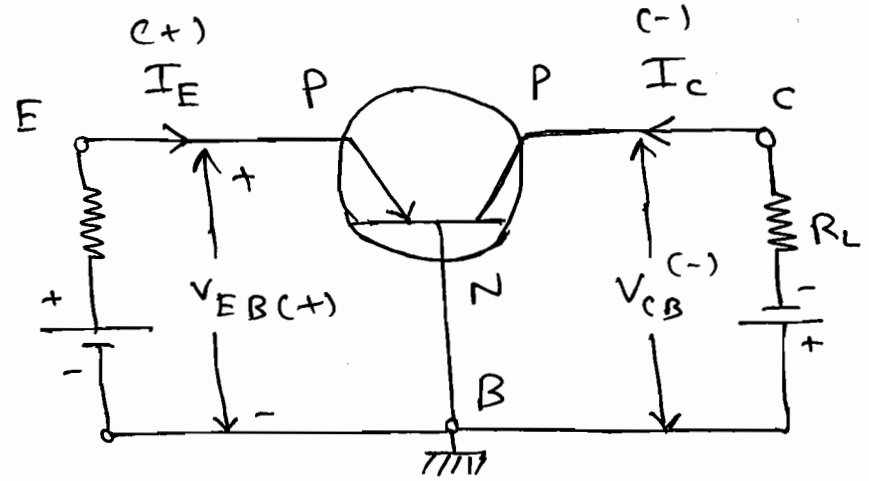
$$= \frac{1 \times 0.026}{0.298 \times 10^{-3}}$$

$$\therefore r_E = 87.24 \ \Omega.$$

$$\therefore \boxed{r_E = 87.24 \ \Omega}$$

* Input and output characteristic of CB (or) Grounded base configuration:

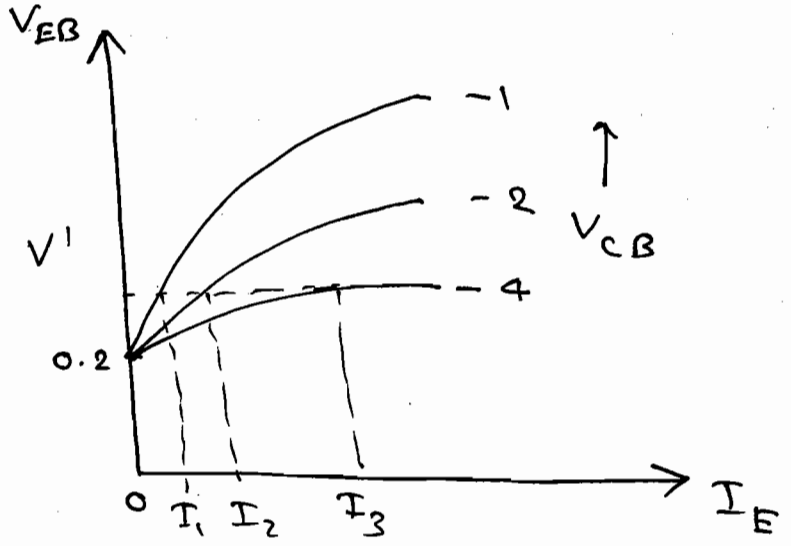
⇒



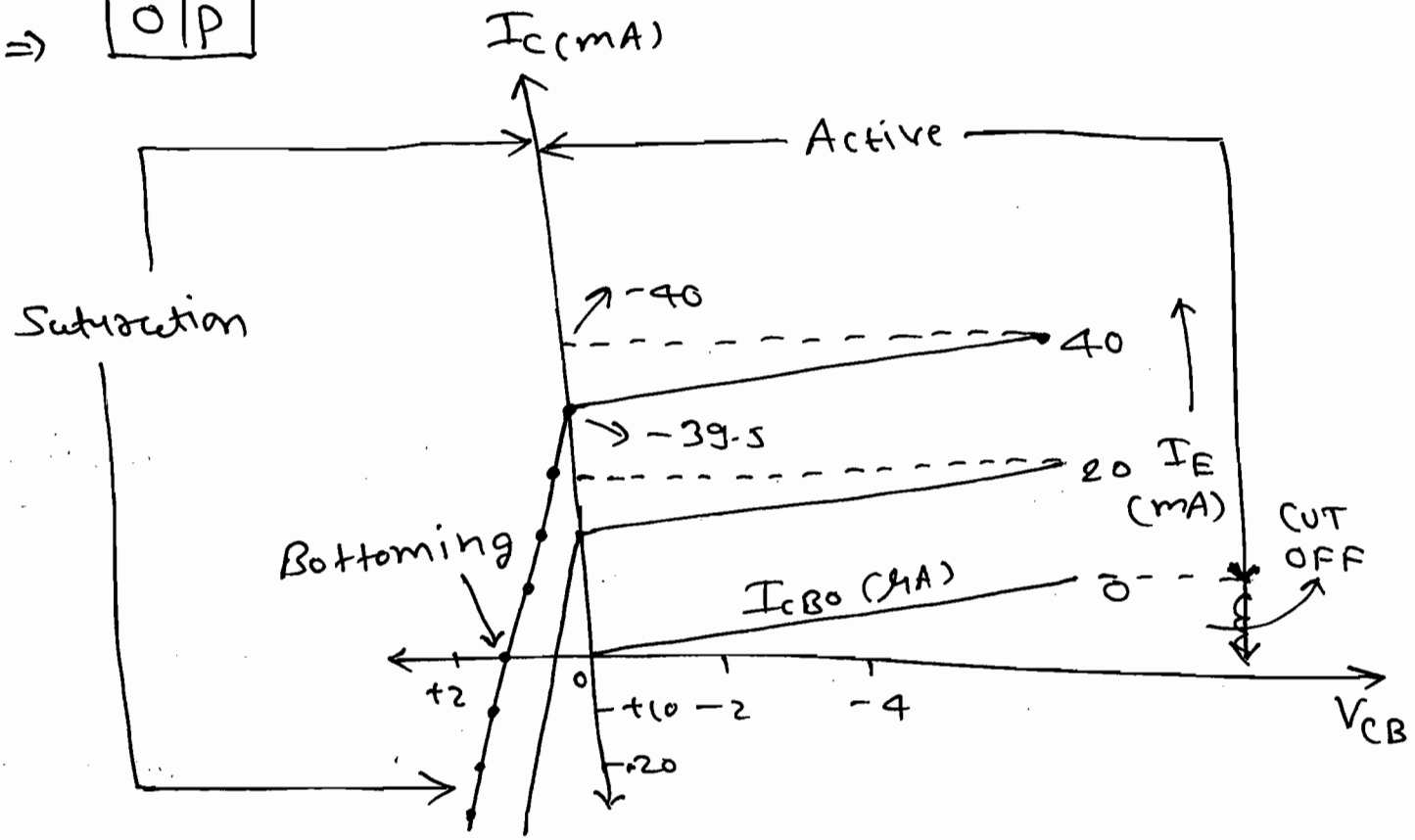
I.V. ⟶ I_E, V_{CB}

D.V. ⟶ V_{EB}, I_C.

⇒ I/P



⇒ O/P



⇒ I.V. : Independent Variable.

D.V. : Dependent Variable.

* Input characteristics:

⇒ I/P Chara. of CB Configuration Concept wise looks similar to Forward char. of P-N diode since V_{EB} and I_E are

are Voltage across and current through forward biased emitter jn diode. the shape doesn't match since x-axis and y-axis are interchanged.

⇒ As Reversed bias to J_c increases according to early effect ① I_E increases hence input current shift down.

* Output Characterestics:

⇒ Active Region:

→ $I_c = -\alpha I_E + I_{CBO}$.

→ Say $I_E = 0$, then $I_c = I_{CBO}$ is Constant. irrespective of V_{CB}.

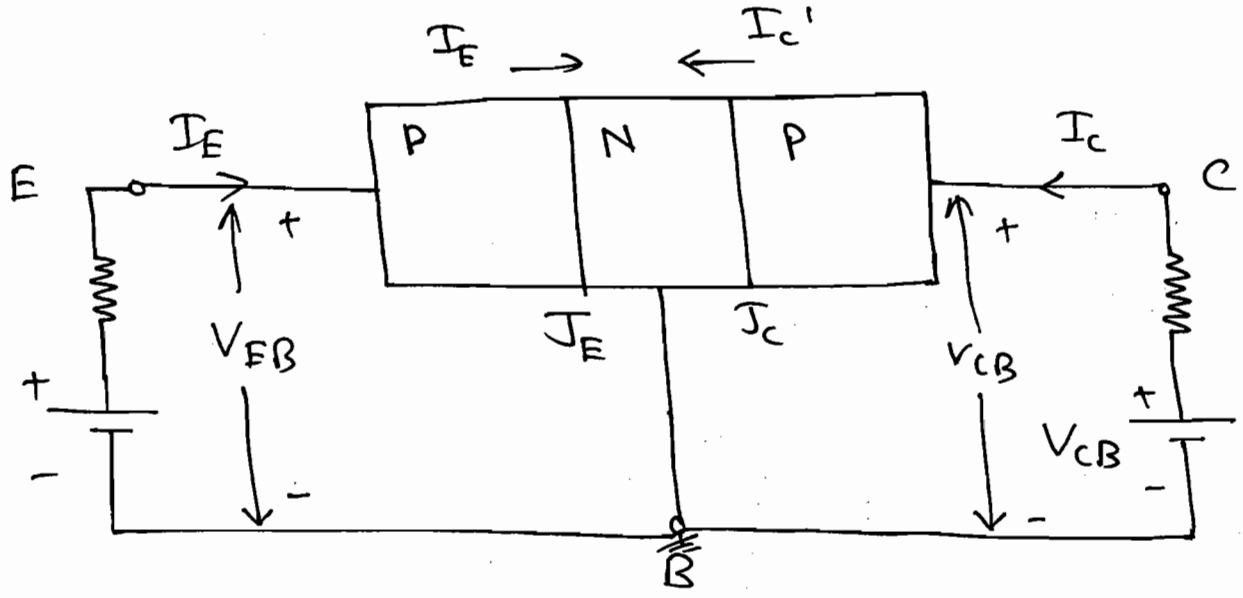
→ Say $I_E = 4mA$, then I_{CBO} gets neglacted. as reversed biased to J_c increases according to early effect ② α increases. $\alpha < 1$ and closed to 1. If it increases, finally it becomes one hence I_c starts from less than I_E and closed to I_E, increases and finally becomes I_E. Hence Curves are almost Straight line i.e. not much Slope is existing.

$$\Rightarrow \quad I_C = -\alpha I_E + I_{CBO}$$

$\alpha < 1$ — As RB To $J_C \uparrow$ → $\alpha \simeq 1$

$|I_C| < |I_E|$ — EE ② → $\alpha \uparrow$ — $|I_C| = |I_E|$.

$\Rightarrow$ Saturation:



$\Rightarrow$ V_{EB} = Constant

mA

V_{CB}	I_E	I_C'	Net Current	I_C
			$\rightarrow$ 30	
+0.5	40	10		−30
+1.5	40	40	0	0
			$\leftarrow$ 10	
+2.0	40	50		+10.

$\Rightarrow$ As V_{CB} Forward biased to J_C increases I_C changes from −ve to zero to +ve

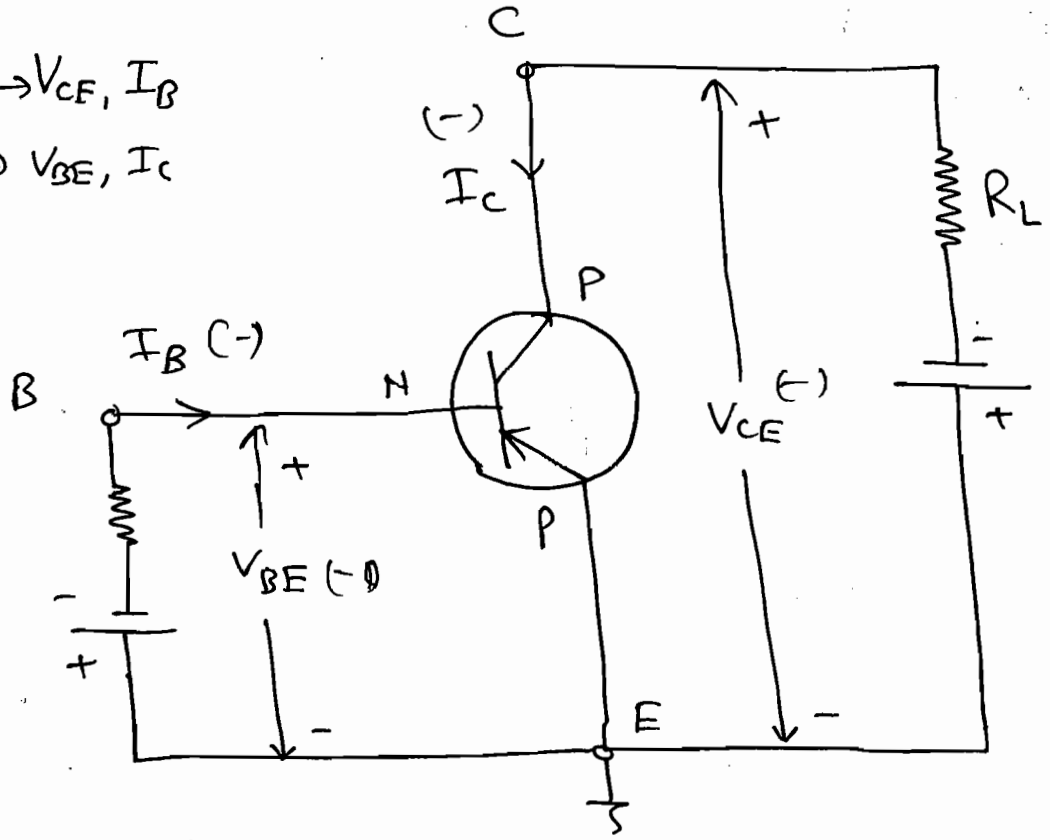
⇒ For different values of I_E, all the curves are touching the bottom at x-axis hence bottoming is said to have occurred.

* Input and output Characteristic of CE (or) Grounded Emitter Configuration:

⇒

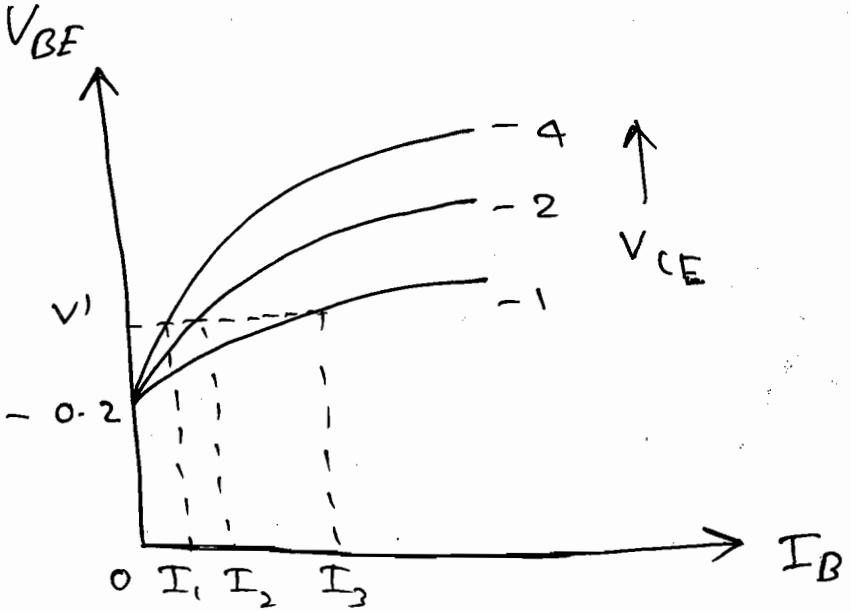
I.V. :→ V_{CE}, I_B

D.V. :→ V_{BE}, I_C



⇒

I/P



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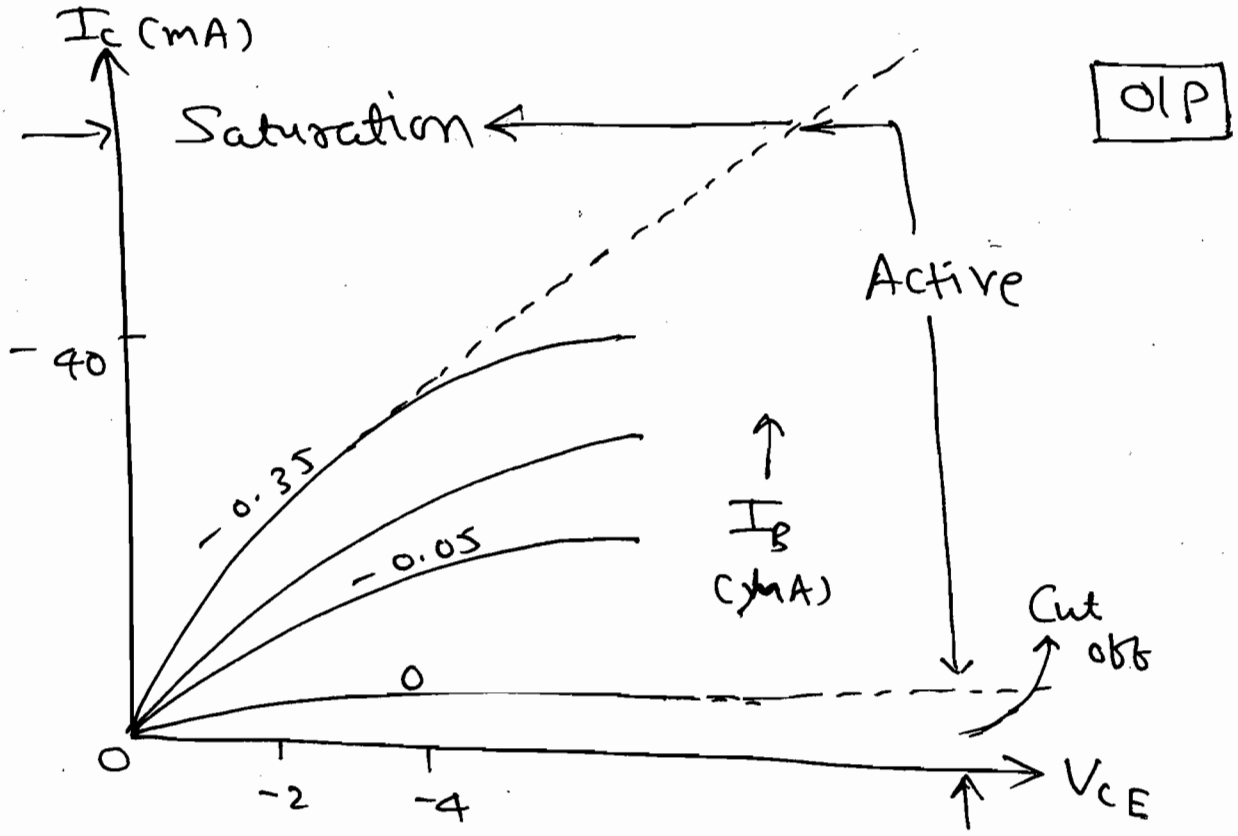


⇒

$$I_C = (1+\beta) I_{CBO} + \beta I_B .$$

$$\beta = \frac{I_C - I_{CBO}}{I_B + I_{CBO}} = \frac{\alpha}{1-\alpha} .$$

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{\alpha_{dc}}{1-\alpha_{dc}} .$$

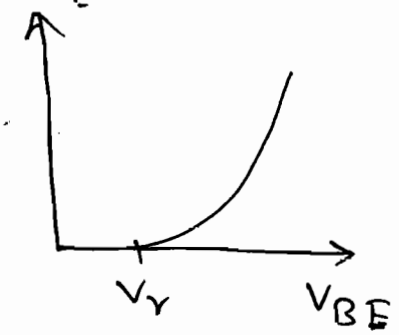
* Input Characteristics:

⇒ Input char. of CE configuration concept wise look similar to forward char. of P-N diode since V_{BE} and I_B (proportional to I_E) are Voltage across and current through forward biased emitter jn diode.

the shape doesn't match since x-axis & y+ axis are interchanged.

⇒ As reversed biased to J_c increases early effect - ② says α increases hence I_c increases hence I_B decreases. i.e. input curves move up.

⇒ $I_B \alpha I_E$



$$I_E = I_B + I_c$$

(mA): $1\,mA\uparrow = 0.01\,mA\uparrow + 0.99\,mA\uparrow$

As RB To $J_c\uparrow \longrightarrow$ EE ② $\rightarrow \alpha\uparrow \rightarrow \alpha\uparrow = \dfrac{I_c\uparrow}{I_E}$

$\rightarrow$ $I_E = I_B\downarrow + I_c\uparrow$.

⇒ <u>CE Saturation Resistance</u> (R_{CEsat}):

$$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_c}$$

→ I_{CBO}: <u>C</u>ollector current with collector jn RB. in <u>CB</u> with emitter <u>o</u>pen.

→ I_{CEO}: Collector current with collector jn RB in <u>CE</u> with base <u>O</u>pen.

→ β : Common emitter forward current Transfer ratio. (OR) CE current gain.

* Proof of Current gain:

① Mathamatically:

⇒ α is a number < 1 and closed to 1.

Hence $\beta = \left(\frac{I_C}{I_B}\right) > 1$ i.e. output current I_C greater than input current I_B.

② Logically:

⇒ For a small change in input current I_B there is a large change in output current I_C hence current gain exists.

$$I_E = I_B + I_C$$

(mA): 1mA = 0.01mA↑ + 0.99mA↑

③ Graphically:

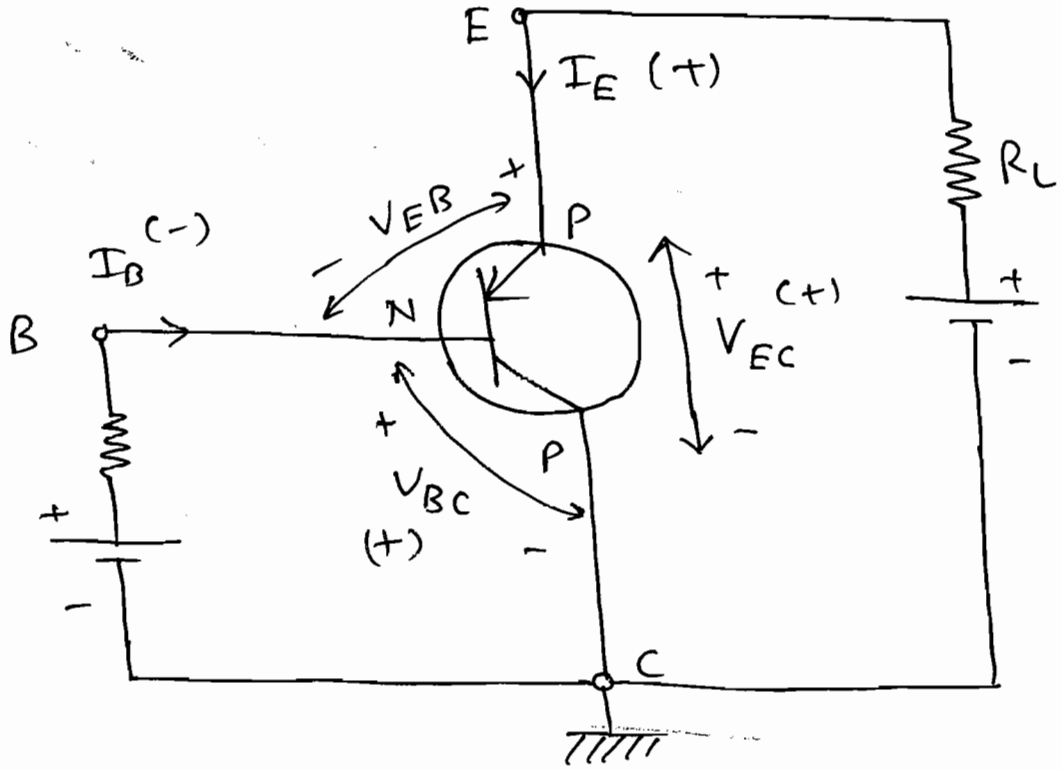
⇒ In o/p char. a slope is existing hence current gain possible.

④ Practically:

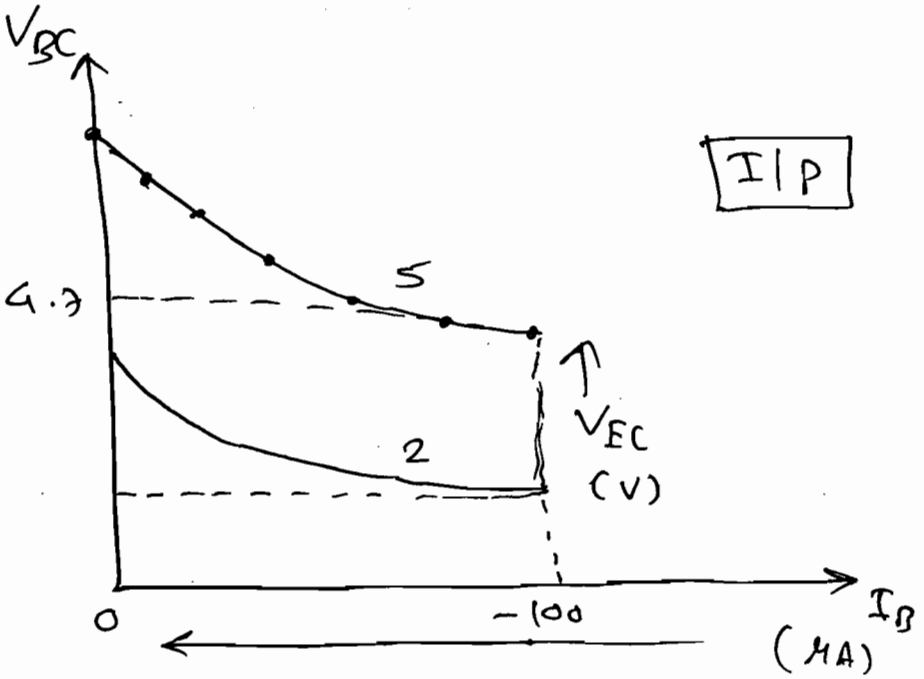
⇒ In CE amplifier experiment existance of current gain can be observed.

✱ Input and Output characteristics in CC (or) grounded collector config?

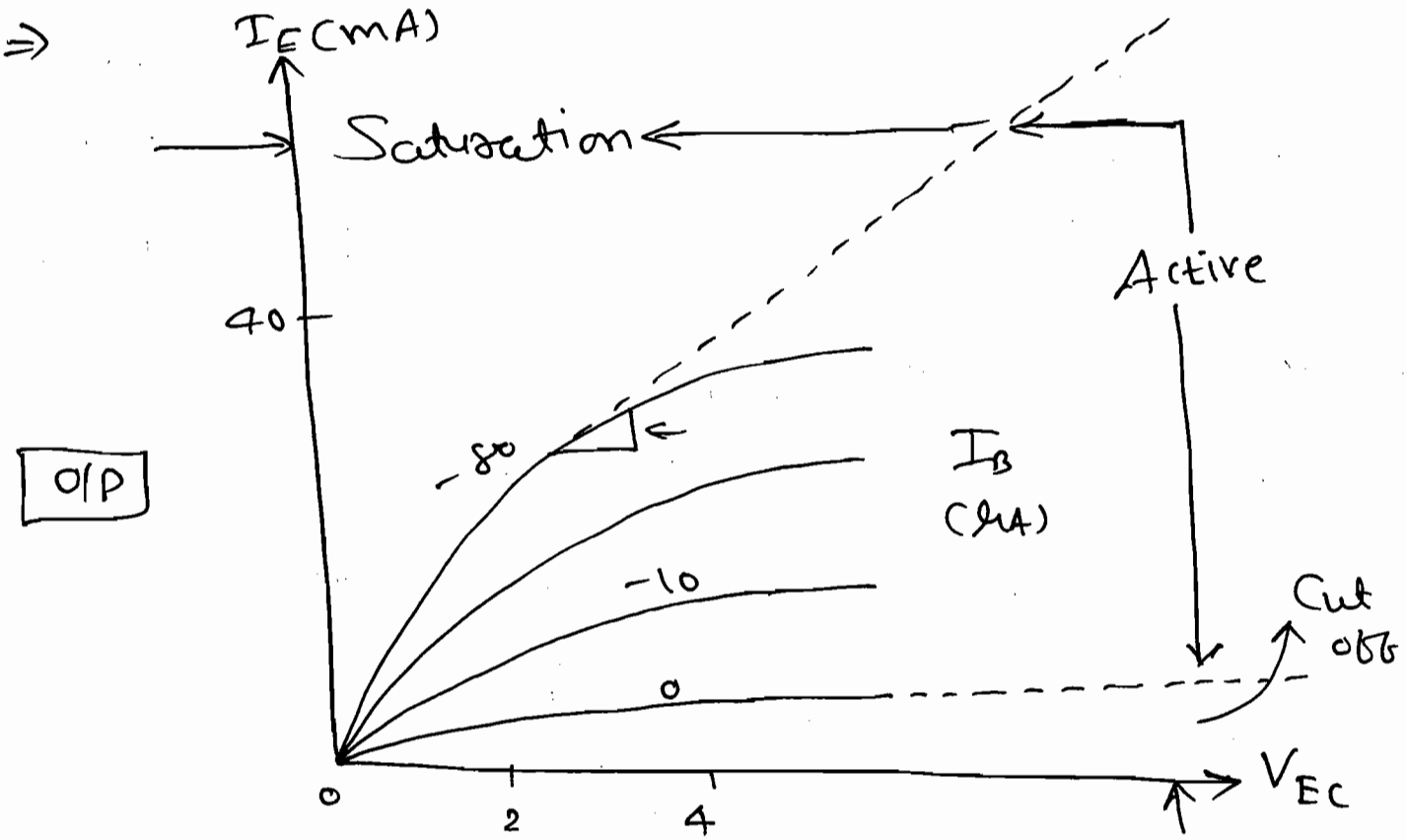
⇒



⇒



⇒



⇒ $\gamma = (-I_E / I_B)$

$$1+\beta = 1 + \frac{I_C}{I_B} = \frac{I_B + I_C}{I_B} = -\frac{I_E}{I_B} = \gamma.$$

$$\alpha << \beta < \gamma$$

A_I : CB CE CC

(0.98) (49) (50)

⇒ γ : Common Collector forward current transfer ratio (or) CC current gain.

* Input Characteristics:

⇒ With V_{EC} kept constant if V_{BC} is increased then V_{EB}, Forward Biased to I_E decreases hence I_E & I_B decreases.

⇒ If V_{BC} further increases then V_{EB} further decreases and becomes less than V_r, cut-in voltage. hence I_E and I_B become '0'. i.e. I_B starts from a value decreases and finally becomes '0'. Hence input curves move up.

⇒ $V_{EC} = V_{EB} + V_{BC} \longrightarrow V_{EB}\downarrow = \boxed{V_{EC}} - V_{BC}\uparrow$

$V_{EB}\downarrow \longrightarrow$ FB to $J_E\downarrow \longrightarrow I_E\downarrow \longrightarrow I_B\downarrow$

$V_{EB} < V_r \longrightarrow J_E$ not FB $\longrightarrow I_E = 0 \rightarrow I_B = 0$.

* Output Characteristics:

⇒ Variable parameter in O/P of CE is same as CC but X-axis in O/P of CE is same as that of CC except for change in polarity.

⇒ Y-axis in O/P of CE is same as that of CC except for slight increase in magnitude hence output of CC and CE look similar except that in CC slope is slightly greater than CE hence

Current gain in CC is (γ) slightly greater than CE (β).

Q A typical BJT has a β of 100. If Collector current is 1mA. Assuming active region find base and emitter currents.

Soln:

$$\beta = 100., \quad I_C = 1mA.$$

$$\therefore \quad \beta = \frac{I_C}{I_B}$$

$$I_B = \frac{I_C}{\beta} = \frac{1mA}{100}$$

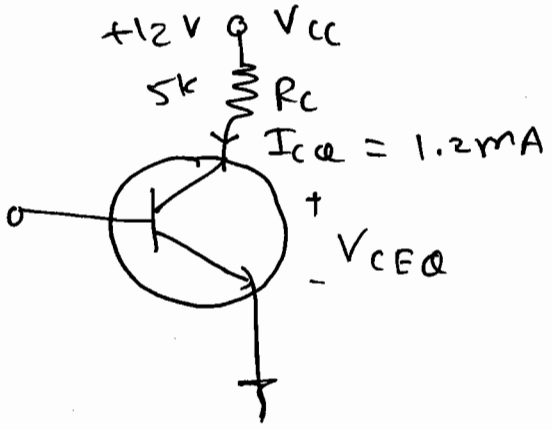
$$\therefore \boxed{I_B = 10\mu A}$$

$$\therefore \quad I_E = I_C + I_B$$

$$\boxed{I_E = 1010\mu A}$$

$$\Rightarrow \boxed{I_E = 1.01mA}$$

Q for the BJT given in ckt determine Q-point.



∴ Soln:

$$\boxed{I_{CEQ} = 1.2mA}$$

$$\therefore V_{CEQ} = V_C - V_E$$

but $V_E = 0$.

$$\therefore V_{CEQ} = V_C = V_{CC} - I_{CQ} \cdot R_C$$

$$V_{CEQ} = 12 - (5 \times 1.2).$$

$$= 12 - 6$$

$$\therefore \boxed{V_{CEQ} = 6\ V}$$

Q- Point : $(V_{CEQ}, I_{CQ}) = (6V, 1.2mA)$.

Q In grounded base configuration Voltage drop across a load resistor of 4 K is 3V. determine base current given $\alpha = 0.96$.

Soln:

$$I_C = 3/4 = 0.75mA.$$

$$\alpha = 0.96.$$

$$I_B = \frac{I_C}{\beta}$$

$$I_B = \frac{0.75}{24}$$

$$\therefore \beta = \frac{\alpha}{1-\alpha}$$

$$\beta = \frac{0.96}{0.04} = 24$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

$$\alpha = \frac{I_C}{I_E}$$

$$\alpha = \frac{I_C}{I_B + I_C}$$

$$\frac{1}{\alpha} = 1 + \frac{I_B}{I_C}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}.$$

$\Rightarrow \boxed{I_B = 31.25\,\mu A.}$

$\boxed{I_E = I_C/\alpha = 0.781\,mA}$

Q In a CB configuration emitter current is 1.6 mA, collector current with emitter open is 10 μA. Calculate collector current? given gain is 0.95.

Soln:

$$I_C = |-\alpha I_E| + I_{CBO}.$$

$$\therefore I_C = (0.95 \times 1.6) + 10\,\mu.$$

$$\Rightarrow \boxed{I_C = 1.53\,mA}$$

Q For CE mode BJT base current is 10 μA current gain 99. $I_{CBO} = 1\,\mu A$. Calculate collector current.

Soln:

$$I_B = 10\,\mu A.$$

$$\therefore I_C = \beta I_B + I_{CBO}.(1+\beta)$$

$$= (99 \times 10\mu) + 1\mu\,(100).$$

$$I_C = 1090\,\mu A$$

$$\therefore \boxed{I_C = 1.09\,mA}$$

Q) For a BJT Collector Current is 0.9mA, Base current is 20μA. Calculate α.

Soln:

$I_C = 0.9mA$

$I_B = 20\mu A$

$\therefore \beta = \frac{\alpha}{1-\alpha}$

$\beta = \frac{I_C}{I_B}$

$\beta =$

$\beta(1-\alpha) = \alpha$

$\beta = (1+\beta)\alpha$

$\alpha = \beta / 1+\beta$

$\alpha = \frac{I_C}{I_E}$

$\alpha = \frac{0.9m}{0.9m + 20\mu}$

$\therefore \boxed{\alpha = 0.978}$

Q) given common base current gain as 0.98. calculate CE current gain.

Ans:

$\alpha = 0.98$

$\beta = \frac{\alpha}{1-\alpha}$

$\therefore \beta = \frac{0.98}{0.02}$

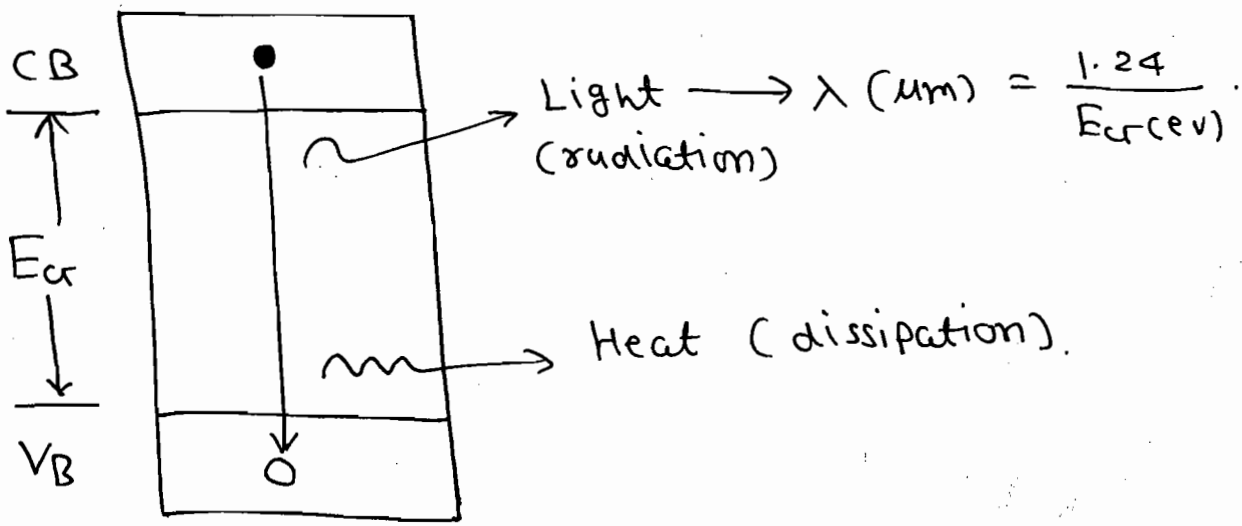
$\boxed{\beta = 49}$

✡ Opto Electronic Divices:

⇒ LED & LASER Convert electric energy to light energy and are used as optical Sources.

⇒ PIN & APD Convert light energy to electric energy and are used as optical detectors in fiber optic communications.

⇒



⇒ In certain semiconductors EHP Recombination occurs in two steps called Indirect transition (or) Indirect Recombination and E_G gets converted to heat (dissipation). Such Semiconductors are called Indirect band gap Semiconductors. e.g. Ge (or) Si.

⇒ In some other semiconductor EHP recombination occurs in single step called direct transition (or) direct recombination and E_g gets converted to light (radiation) such semiconductors are called direct band gap semiconductors.
e.g. Gallium (Ga) Arsenide (As).

⇒ If a P-N Junction is design using indirect Band gap Semiconductor and operated in F.B. then during recombination heat comes out called P-N diode.

⇒ If the same P-N junction is design using direct band gap semiconductor then during recombination light comes out called LED. The colour (or) wavelength emitted depends on E_g, to produce required coloured as O/P. Two (or) more semiconductors are mixed to form a compound such that componds energy band gap is equal to required E_g.

⇒ Compound:

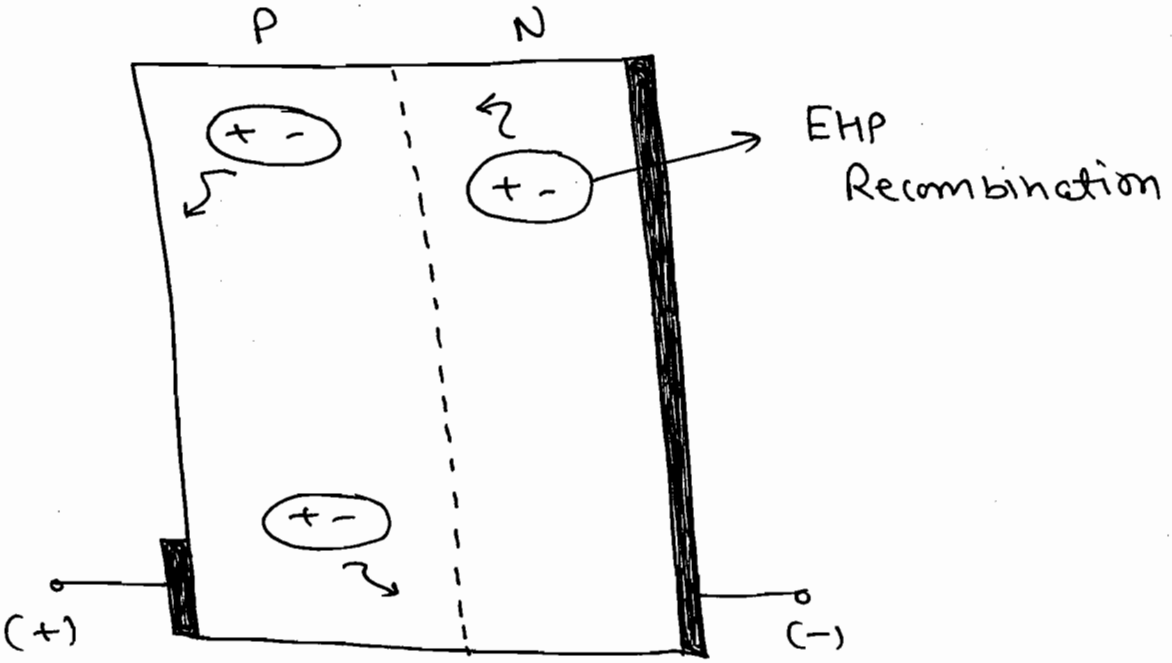
→ Binary : GaAs.

→ Ternary : GaAsP

→ Quarternary : InGaAsP.

* Light Emitting Diode (LED).

⇒



⇒ A P-N junction is design using direct band gap semiconductor and operated in FB condition then during EHP recombination E_G gets converted to light.

⇒ A two terminal device is emitting light hence called Light emitting Diode.

⇒ Applied electric field is responsible for light emission called electroluminations.

⇒ Injected charge carriers during recombination give out light called injection luminations.

⇒ During recombination light comes out called radiative recombination.

⇒ In p-N diode during recombination heat comes out called dissipative recombination.

⇒ In LED Spontenous Emission occurs.

* Advantages:

⇒ Small size ✓
⇒ Less weight. ✓
⇒ Low cost. ✓
⇒ Long life. ✓
⇒ Low power Consumption.
⇒ Rugged Construction. ✓
⇒ Temp. depedence is less. ✓

* Disadvantages:

⇒ Not highly directional.
⇒ Not highly chromatic.

* Light Amplification by Stimulated Emission of Radiation. (LASER).

⇒ If EHP recombination occurs after completion of life time and E_G gets converted to light then it is called Spontenous emission which occurs in LED.

⇒ If recombination occurs before life time completion due to external disturbance and light comes out it is called Stimulated emission which occurs LASER.

⇒ LASERs are produced in Cavity. In a Cavity say population inversion is achieved and an injected photon disturb an e^- and comes out as such the disturb e^- during recombination generates another Photon hence one photon becomes two. The process repeates and due to light amplification voluminous photons are generated. Light is coming out due to

due to stimulated emission with light amplification hence called LASER.

* Advantages:

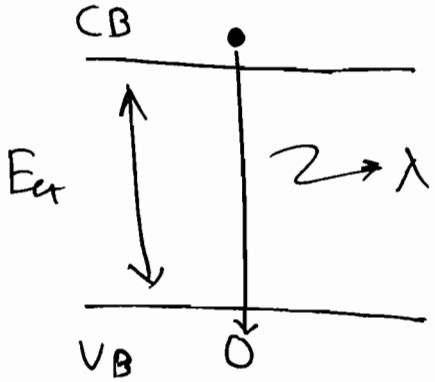
=> Highly directional.

=> Highly Chromatic.

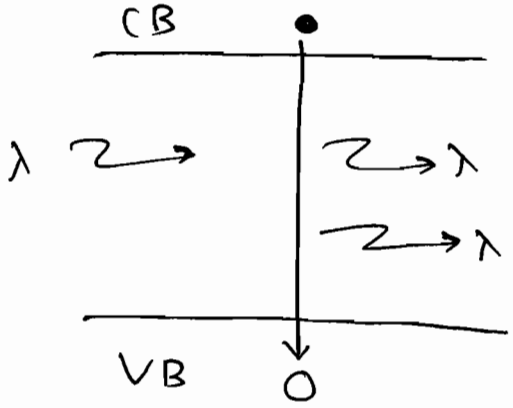
* Disadvantages.

=> (Invert the advantages of LED).

=>



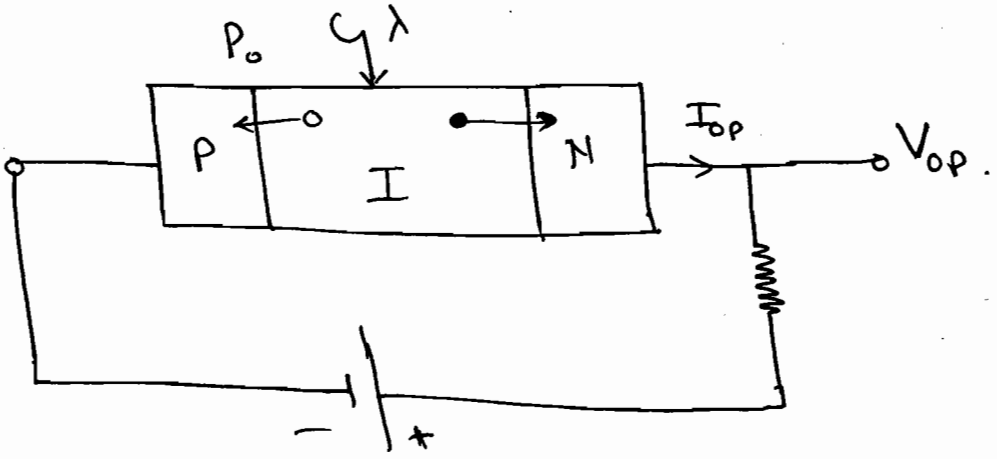
=> Spontaneous Emission



Stimulated emission

* PIN Photodiode:

⇒



⇒

⇒ $E_\lambda \geq E_{cr}$

$E_\lambda = hf = \frac{hc}{\lambda}$] → λ_{max} (μm) $= \frac{1.24}{E_{cr}(ev)}$.

⇒ Quantum efficiency → $\eta = \frac{\text{No. of EHP's generated}}{\text{No. of Photons Incidented}}$

$$\boxed{\eta = \frac{I_p/q}{P_o/hf}}.$$

⇒ Responsivity $\boxed{R = \frac{I_p}{P_o} = \frac{\eta q}{hf}}$ Amp/WATT.

⇒ λ : Wavelength of incident photon.

f : freq. of incident photon.

P_o : Incedent optical power.

h : planck's constant.

→ C: Speed of light

I_p: photo current generated in PIN diode.

⇒ If a Photon having an energy greater than or equal to E_G of a semiconductor falls on the same semiconductor then by absorbing energy of photon. photo carriers are generated which get attracted towards opposite polarity of applied reverse biased and produced photo current I_p.

⇒ Light energy is converted to electric energy hence called photodiode. In the absense of light thermally generated charge carriers support reverse saturation current I_o called Dark current.

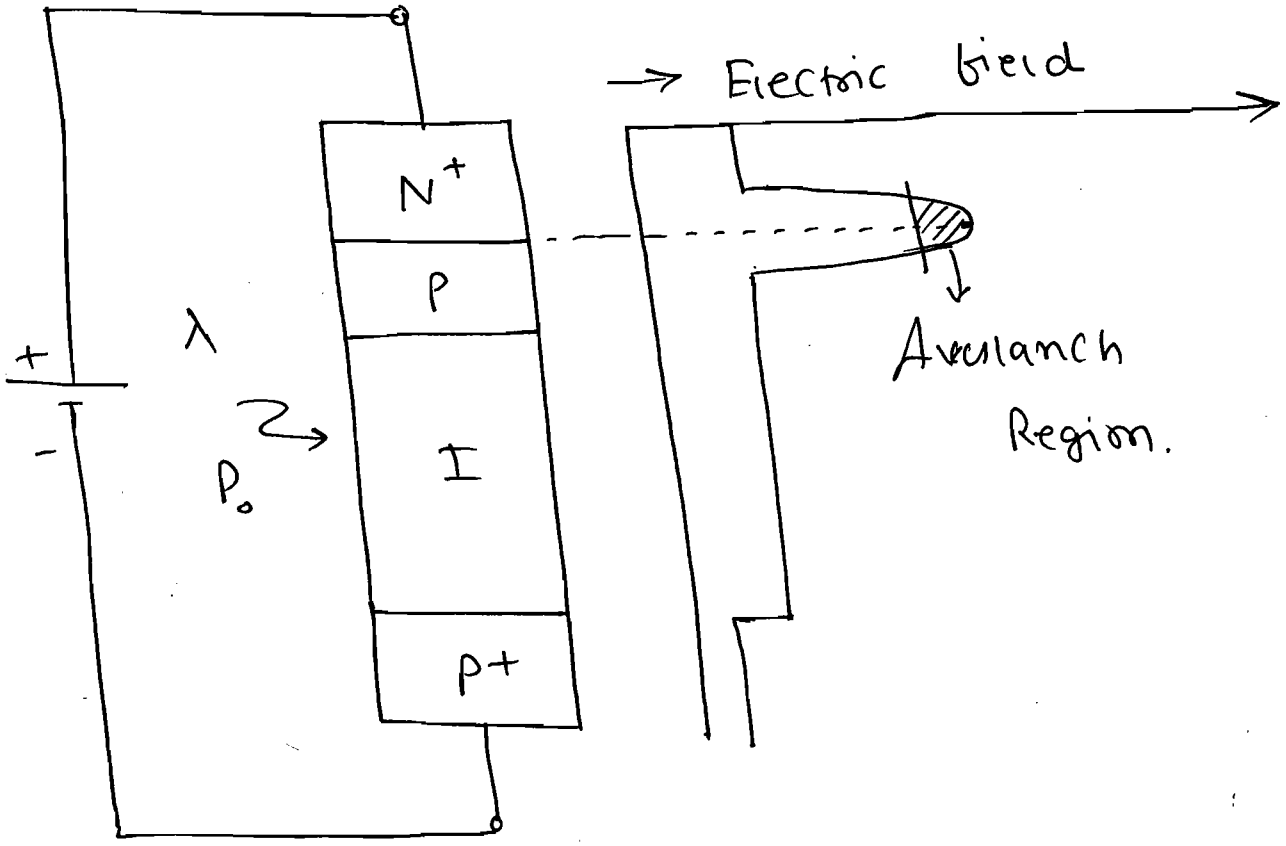
⇒ The range of wavelength over which photo diode gives output is called Spectral Response.

⇒ Minimum optical power to be incidented

on a photo diode to produce a usable output is called light sensitivity.

* Avalanch Photodiode (APD):

⇒



⇒ $$M = \frac{I_M}{I_p} > 1.$$

$$R_{APD} = \frac{\eta_2}{hf} . M,$$

⇒ M: Multiplication factor due to avalanch multiplication.

I_M: multiplied photo current generated in APD.

⇒ due to incident photons Photo carriers are generated which pass through n^+p jn where a large reverse external electric field is applied. due to which avalanch BD occurs. Hence avalanch multiplication starts. hence charge carriers and current increases.

⇒ For a power P_0 Incident on APD say I_M is the current generated and for the same power incidented on PIN diode say I_p is the current generated then

$$\frac{I_M}{I_p} > 1.$$

⇒ Increase in charge carriers and current is called current amplification.

⇒ [a] A silicon APD has a quantum efficiency of 0.65 at a freq. of 0.33×10^{15} Hz. Suppose 0.5 μW of Optical power produces a multiply photo current of 10 μA. Calculate the multiplication factor M.

Soln:

$$I_M = \frac{\eta q}{hf} \cdot M$$

$$\Rightarrow M = \frac{I_M \cdot hf}{\eta q}$$

$$M = 10 \times 10^{-6} \times$$

⇒ Applied η and P_0 to PIN diode and calculate I_p.

$$\therefore I_p = \frac{\eta q}{hf} \times P_0.$$

$$\therefore I_p = \frac{0.65 \times 1.6 \times 10^{-19}}{6.626 \times 10^{-34} \times 10^{15} \times 0.33} \times 0.5 \times 10^{-6}$$

$$I_p = 0.238\ \mu A$$

$$M = \frac{I_M}{I_p} = \frac{10\ \mu A}{0.238}$$

$$M = 42.05$$

$$\boxed{M \simeq 42.}$$

Q A PIN photodiode is constructed with GaAs which has a band gap of 1.43 eV find the longest wavelength that can generate current.

Soln:

$$\lambda_{max}\ (\mu m) = \frac{1.24}{E_G\ (eV)}$$

$$\Rightarrow \quad \lambda_{max(\mu m)} = \frac{1.24}{1.43}$$

$$\boxed{\lambda_{max} = 0.86\ \mu m}$$

(a) 6×10^6 photons are incident on a PIN diode and 5.4×10^6 EHPs are generated. Calculate Quantum efficiency.

Soln:

$$\text{Quantum efficiency } \eta = \frac{\text{No. of EHP's generated}}{\text{No. of incident photon}}$$

$$\eta = \frac{5.4 \times 10^6}{6 \times 10^6}$$

$$\boxed{\eta = 90\ \%}$$

(a) Photons are incident on a PIN diode which has a responsivity of 0.65 A/watt. If optical power level is 10 μW. Calculate photo current generated

Soln:

$$I_p = R/\Omega \quad \frac{I_p/q}{P_0/h\nu}.$$

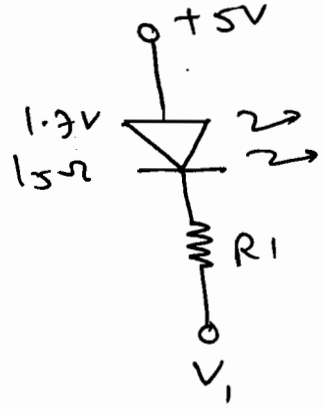
$$R = \frac{I_p}{P_0}$$

$$\therefore \quad I_p = R \cdot P_0 = 0.65 \times 10 \times 10^{-6}$$

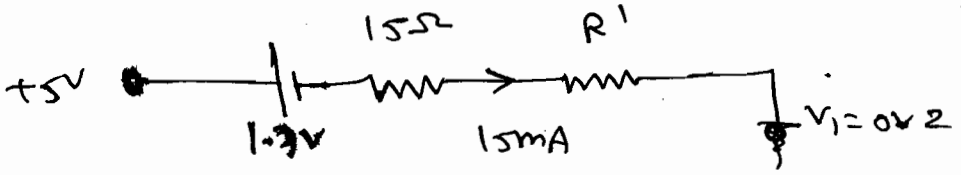
$$\boxed{I_p = 6.5\ \mu A}$$

[a] A LED is connected as shown it should glow when V_1 is at logic '0' state (0.2V). Calculate R'. Assume in active state current as 15mA.

Soln:



$\Rightarrow$ V_1 is at Logic '0' $\Rightarrow$ $V_1 = 0.2 = 0.2$



By KVL,

$$5 - 1.7 - 0.2 - (15 + R')\,15m = 0.$$

$$\frac{3.1}{15} = 15 + R'.$$

$$\therefore \boxed{R' = \frac{206.8}{191.67}\ \Omega}$$

* Junction Field Effect Transistor (JFET):

⇒

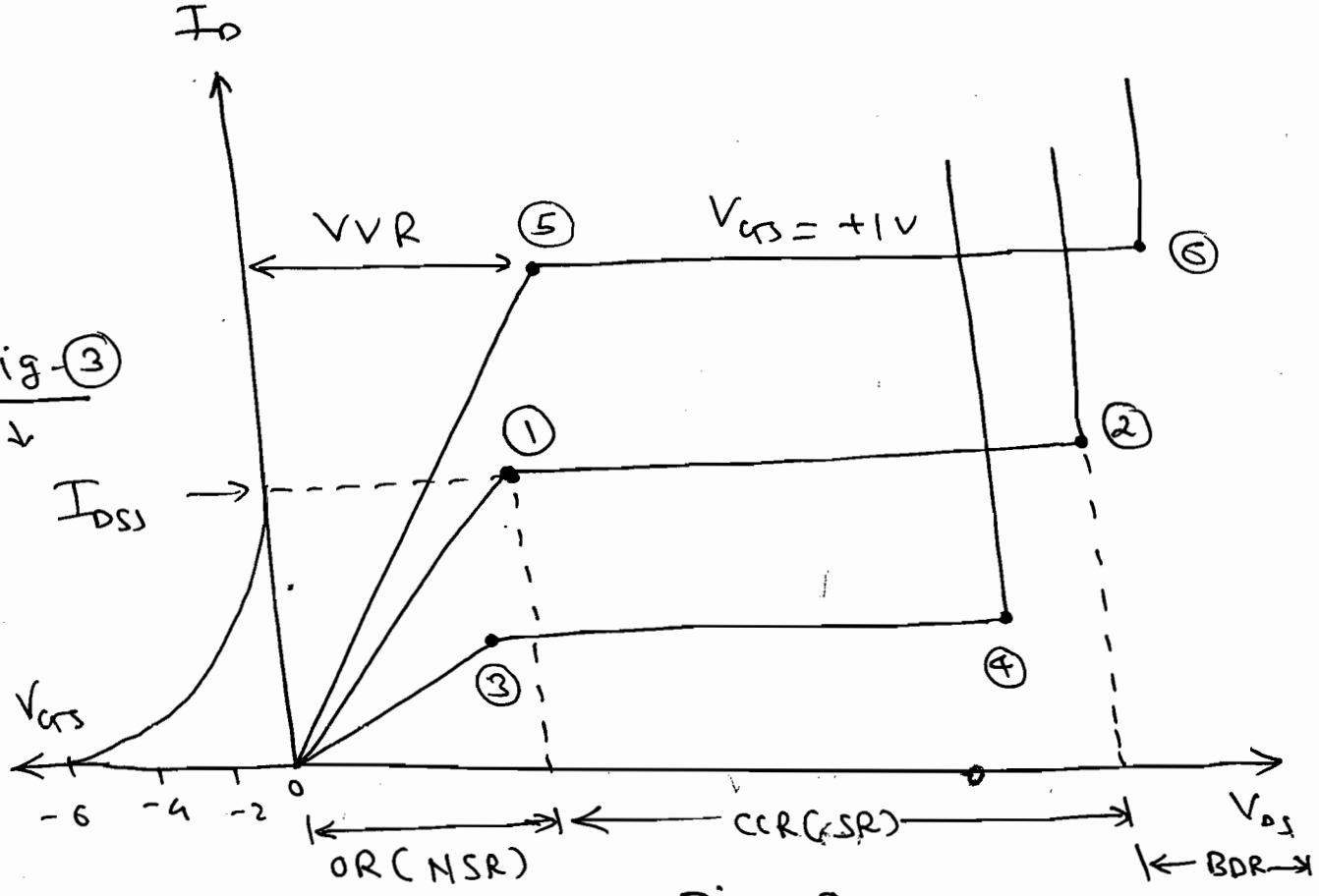


Fig-③

↓

Fig- ④

⇒

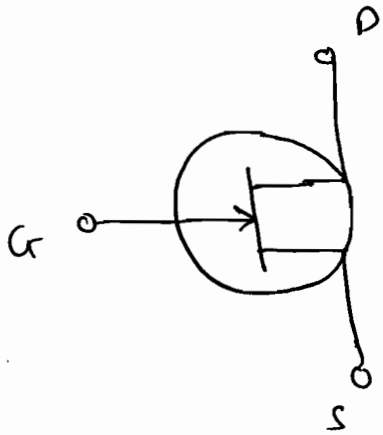


Fig-⑤

⇒

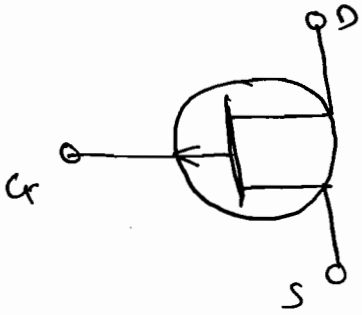


Fig- ⑥

⇒

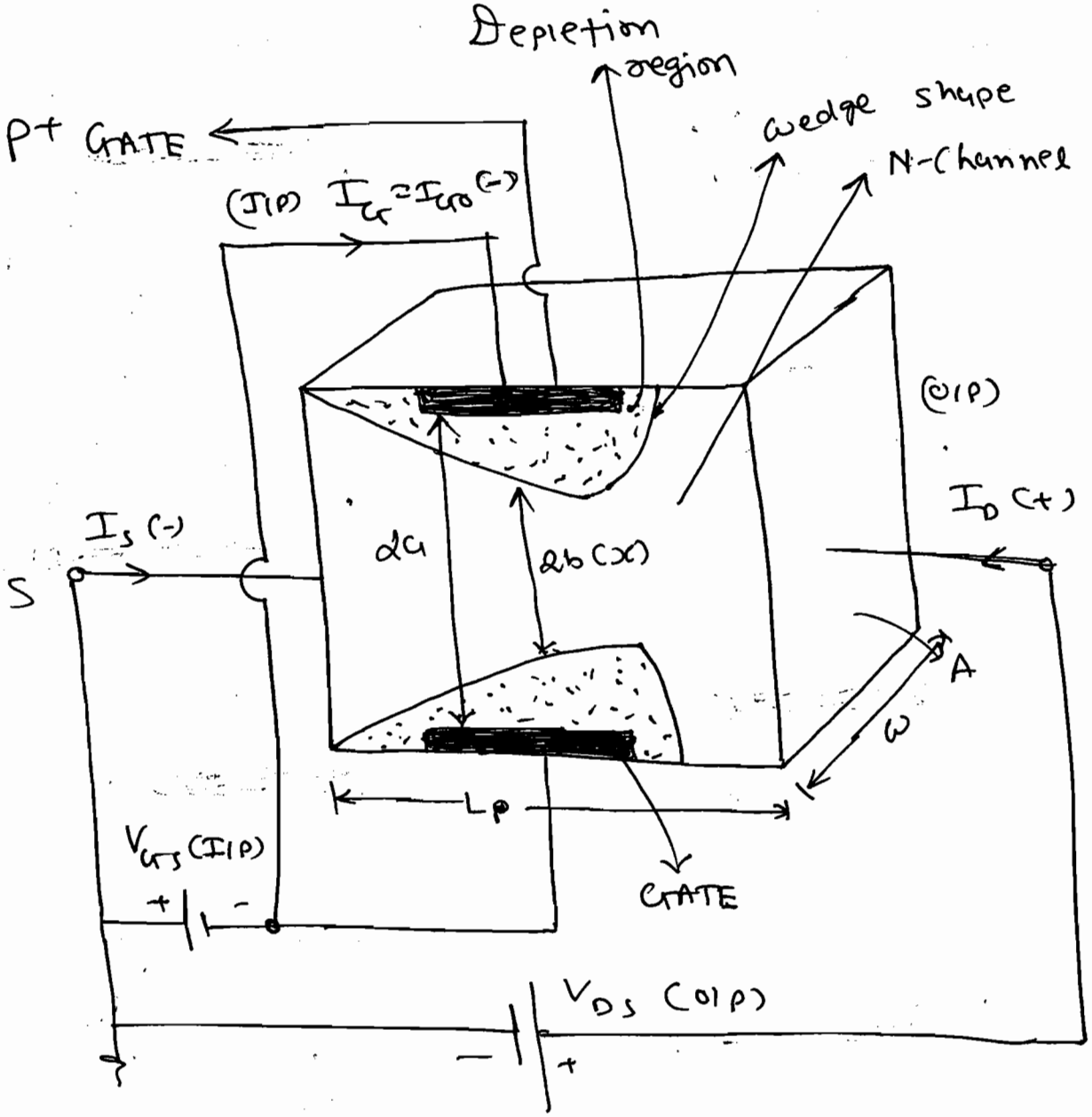

Depletion region
wedge shape
N-Channel
P+ GATE
(I/P) $I_G = I_{G0}$ (-)
(O/P)
I_D (+)
I_S (-)
S
$2a_G$
$2a_b(x)$
A
W
L_P
V_{GS} (I/P)
GATE
V_{DS} (O/P)

Fig- ①

⇒

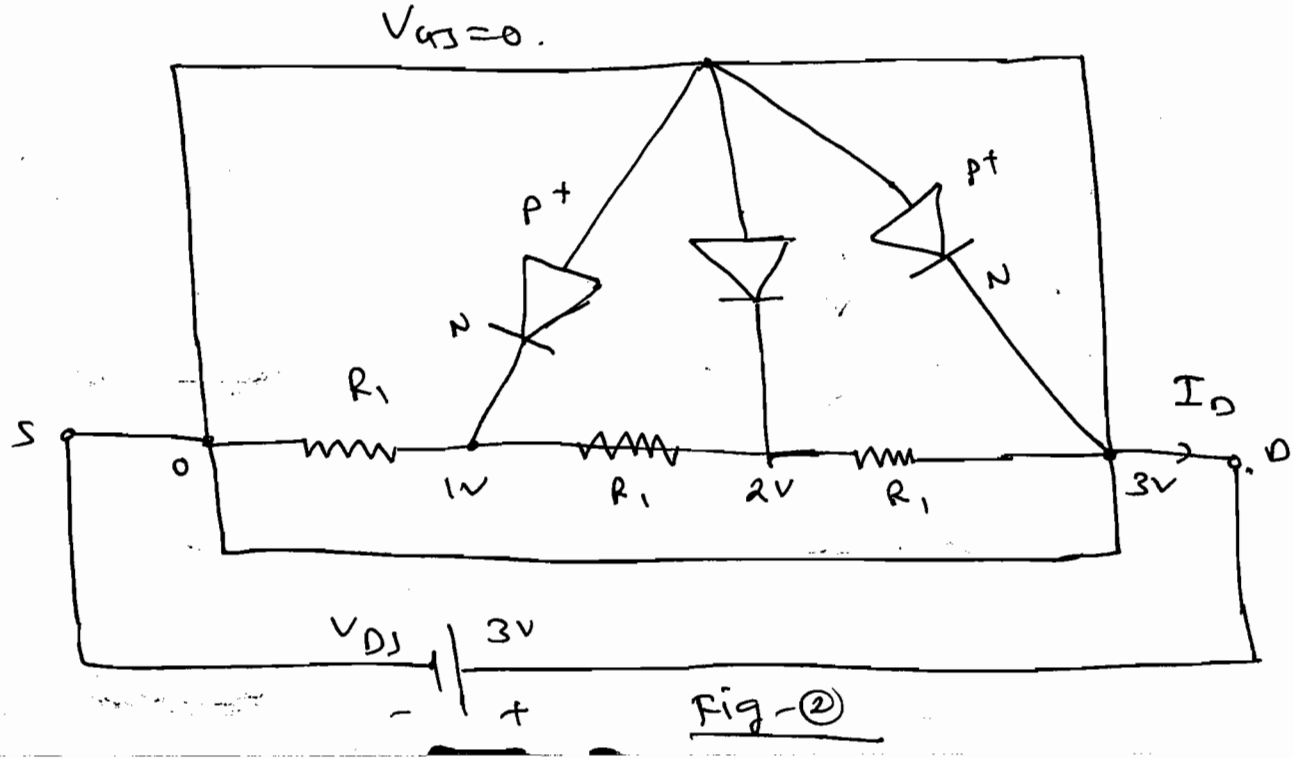
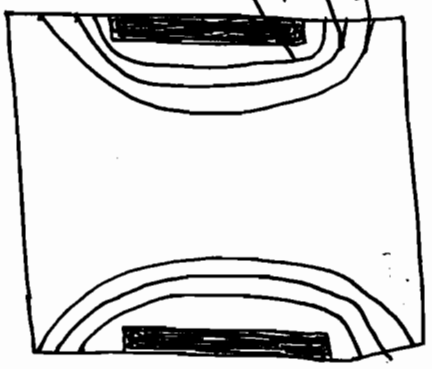

$V_{GS}=0$.
P+
P+
N
N
R_1
I_D
S
0
1V
R_1
2V
R_1
3V
D
V_{DS}
3V
-
+

Fig-②

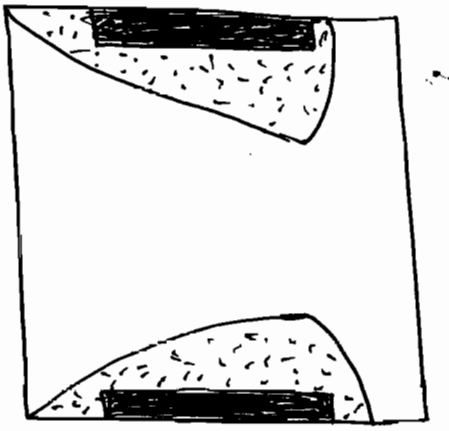
⇒

(A) $V_{DS} = 0$

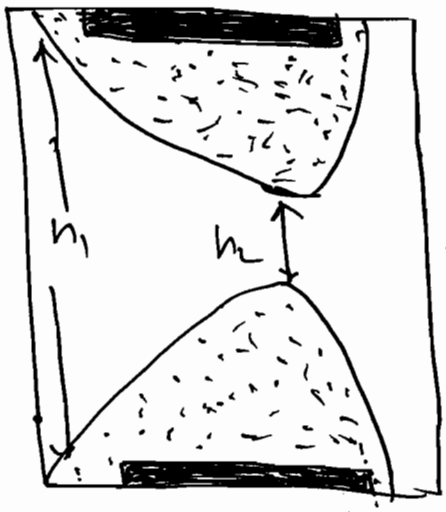
$V_{GS} = +1$, 0, -1



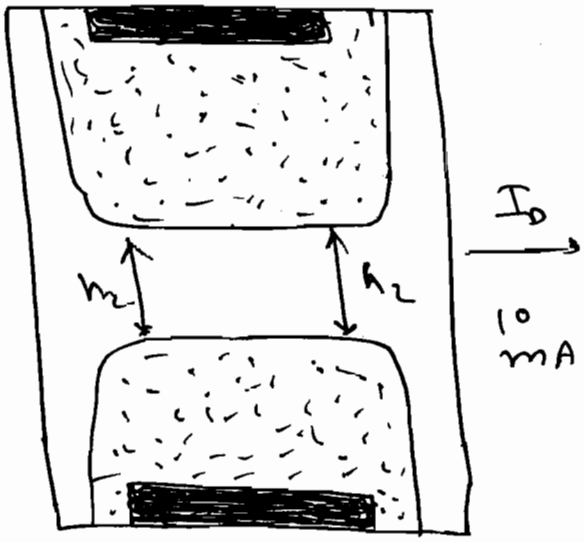
(B) $V_{DS} \uparrow$ (3V)



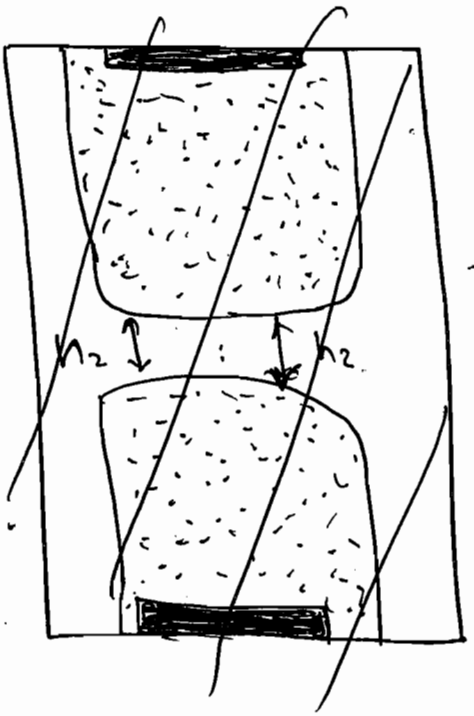
(C) $V_{DS} \uparrow\uparrow$ (6V)



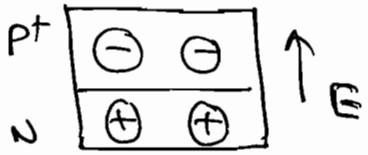
(D) $V_{DS} \uparrow\uparrow\uparrow$ (10V)



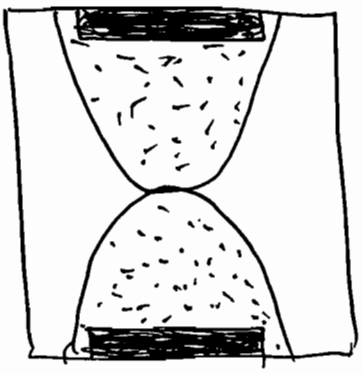
(E) ~~E~~



(F)



(E)



$V_{GS} \uparrow\uparrow$ (-6V)

⇒ Channel supports flow of only one charge carrier hence it is unipolar device.

⇒ The Voltage betⁿ drain and Source V_{DS} is to be choosen such that charge carriers enter through Source terminal into channel and leave the channel through drain terminal.

⇒ The Top and Bottom pt gates along with n-channel form gate junction diodes.

⇒ The Voltage betⁿ gate and Source V_{GS} is to be choosen such that gate junction diodes are reversed biased.

⇒ Interchanging drain and Source terminal will not affect the operation hence circuit symbol doesn't differentiate betⁿ drain and Source terminals.

⇒ The direction of arrow shows the direction flow of current when gate jⁿ diode is forward biy.

⇒ Pinch-OFF:

	V_{DS}	V_{GS}	I_D
①	↑	Const.	Const. (OR) (pinch off region).
②	Const.	↑	0

→ In fig-(A), the top and bottom curves drawn for $V_{GS} = 0$ and $V_{DS} = 0$ correspond to penetration of depletion region into channel under open circuit condition of gate j^n diode.

→ ~~In~~ N-channel, semiconductor bar acts like resistor across which a voltage V_{DS} is given through which a current I_D flows.

→ As V_{DS} increases I_D increases linearly as shown in ohmic Region (OR).

→ From left to right length (L) increases Resistance increases, voltage drop increases and Reverse bias given to n-side progressively increases hence penetration

of depletion region into channel progressively increases hence depletion region takes a non-uniform shape called wedge shape.

→ To the left, to middle and right sides penetration of depletion region into channel will be more in $V_{DS}=0V$ case than $V_{DS}=3V$ case. since in 0V case reverse bias is more than corresponding 3V case but the shape is still non-uniform.

⇒ $2a$: Height of channel. (distance betⁿ gates)

a: Half height of channel.

$2b(x)$: Effective height of channel (distance betⁿ depletion region at a distance of x).

$b(x)$: Effective half height of channel.

h_1, h_2: Max, min effective height of channel.

⇒ minimum effective e- height decides the magnitude of drain current.

⇒ w.r.t. Stability and retaining of current fig- ⓓ is correct and fig -Ⓐ is wrong hence as V_{DS} increases from 0V to 10V fig- Ⓒ moves to ⓓ hence I_D becomes constant as shown in CRR (Constant Current Region).

⇒ Beyond CCR as V_{DS} increases across top and botton depletion regions a large electric field gets developed and avalanch BD occurs hence avalanch multiplication starts hence charge carriers and I_D increase ~~or~~ un controllably. as in BD region (BDR).

⇒ Maximum Controllable current is possible in CCR hence called Saturation Region (SR). Hence OR (ohmic region) becomes Non Saturation

region (NSR).

→ ECR and VVR will occur at a lesser value of V_{DS} for $V_{GS} = -1V$ compare to $V_{GS} = 0V$ since in $V_{GS} = -1V$ case initial depletion region is deeper than $V_{GS} = 0V$ case. Device can be used as Voltage Variable Resistor (VVR) by Varying V_{GS} in ohmic region.

→ Input Resistance

$$R_{GS} = \frac{V_{GS}}{I_G}$$ is high.

⇒ As V_{GS} increases (more -ve) reverse bias given to gate in diodes increases more and more hence penetration of depletion region into channel increases hence minimum effective height and drain current decreases more and more. at a perticular Voltage big-(E) occurs hence mihimum effective height and I_D become zero. Thus, Transfer char. can be explained.

Note:

→ If V_{DS} increases and fig-(E) occurs then minimum effective height, drain current, current through Resistance, drop across Resistances and Voltage given to n side of diodes become zero hence the diodes are open circuited hence width of depletion region decreases hence fig-(E) Jumps to (A) hence fig (E) either was unstable.

→ If V_{GS} increases and fig-(E) occurs then even if voltage given to n-sides of diodes becomes '0' <u>still</u> the diode are reversed biased due to -ve supply given by V_{GS} to P^+ side.

→ In a Reverse bias diode a large depletion region can survive hence this time fig-(E) is a stable state.

→ Pinch off voltage V_P is defined as Voltage bet^n gate and source V_{GS} for $V_{DS} = 0$ at which channel closes.

(V_p is -ve for n-channel and +ve for p channel).

→ As input voltage V_{GS} increases, input current I_G is constant but output ~~Volta~~ current I_D decreases hence it is voltage ~~control~~ control device.

→ In fig-(F), +ve means +very charged donor ion existing in depletion region of n-channel, -ve means -very charged Acceptor ion existing in depletion region of p^+-gate.

→ Across +ve and -ve ions existing in depletion region internally electric flux line get developed which control the operation hence called electric field effect.

⇒ Electric field deloped across a junction is controlling the operation of a 3-terminal device hence called Junction Field effect Transistor (JFET).

* Salient points of JFET: (compare to BJT).

⇒ Voltage Controlled device.

⇒ I/p Resistance is high.

⇒ No offset Voltage.

⇒ Unipolar device.

⇒ Small in size.

⇒ Better thermal Stability.

⇒ Easy to fabricate.

⇒ Low power Consumption.

Note:

→ In a BJT in the path of flow of current a junction exist hence a minimum offset voltage V_γ to be applied for BJT to go to on state No such junction (or) offset voltage for JFET.

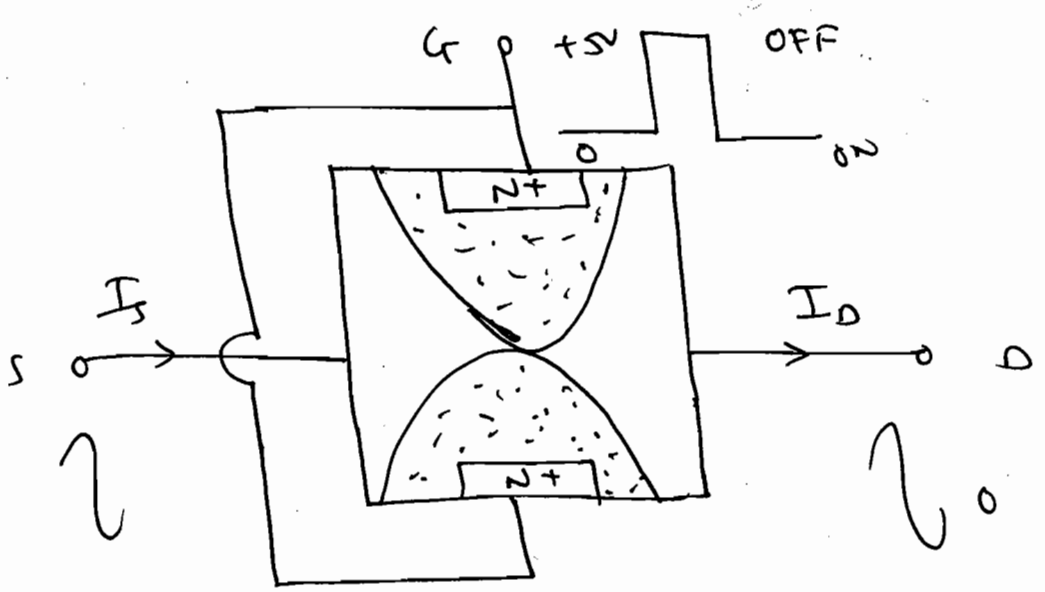
* Applications:

⇒ Voltage Variable resistor.

⇒ Buffer.

⇒ Digital Analog switch.

→ A digital pulse is controlling a operation of analog switch hence called digital analog switch.



$$\Rightarrow V_p = (-qN_D a^2/2\epsilon) \rightarrow \text{N- Channel.}$$

$$V_p = (+qN_A a^2/2\epsilon) \rightarrow \text{P- Channel.}$$

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2.$$

$$\rightarrow V_{DS} + V_p = V_{GS}.$$

$$\rightarrow V_{GS} = (1 - b/a)^2 V_p.$$

$$\rightarrow I_D = \frac{2aWqN_D\mu_n}{L}\left[1 - \left(\frac{V_{GS}}{V_p}\right)^{1/2}\right] V_{DS}.$$

$$R_{d_{ON}} = \frac{V_{DS}}{I_D}\Big|_{V_{GS}=0} = \frac{L}{2qWqN_D\mu_n}.$$

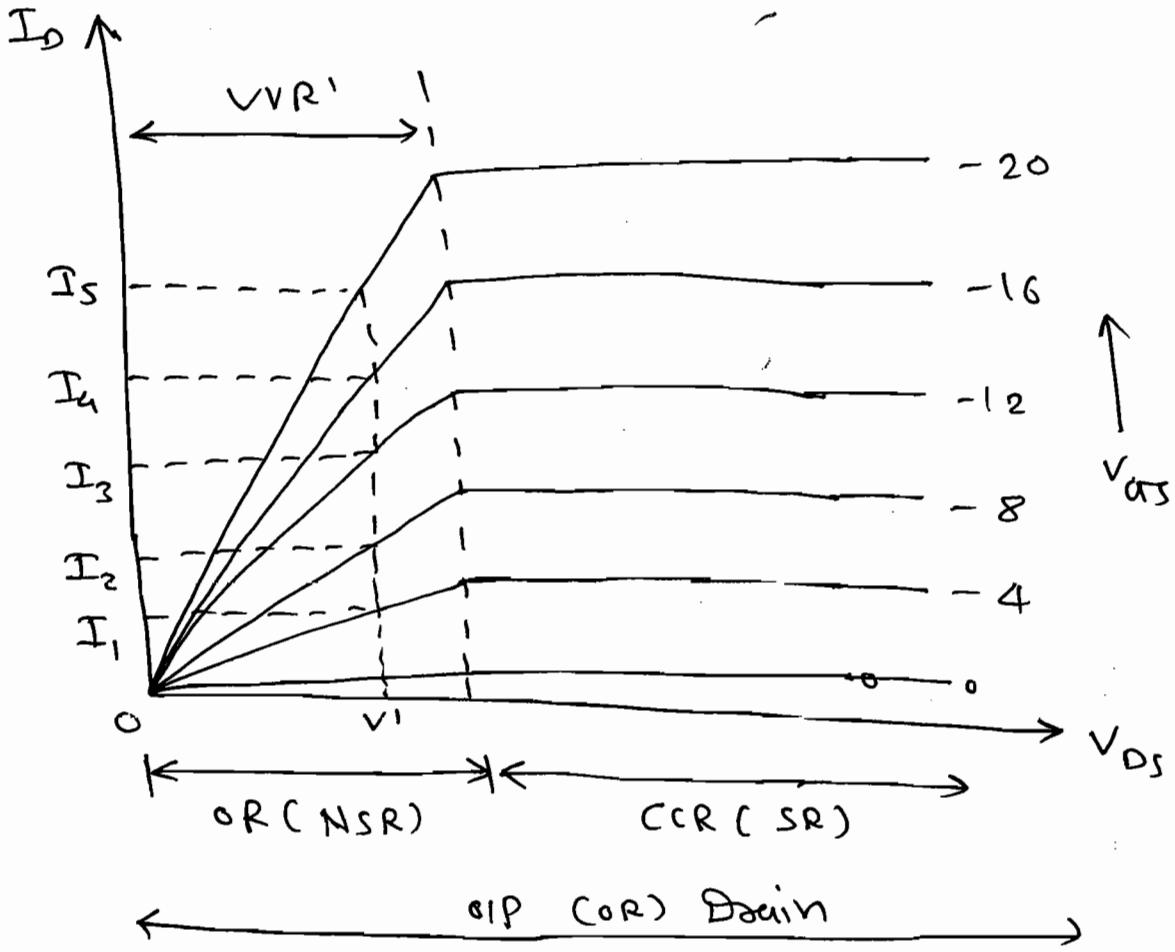
⇒ I_{DSS} : Drain Saturation current at $V_{GS}=0$

I_{DS} : Drain sat^n current when $V_{GS} \neq 0$.

$R_{d,ON}$: drain ON Resistance.

* Induced P-Channel Enhancement MOSFET (IGFET) (OR) PMOS.

⇒



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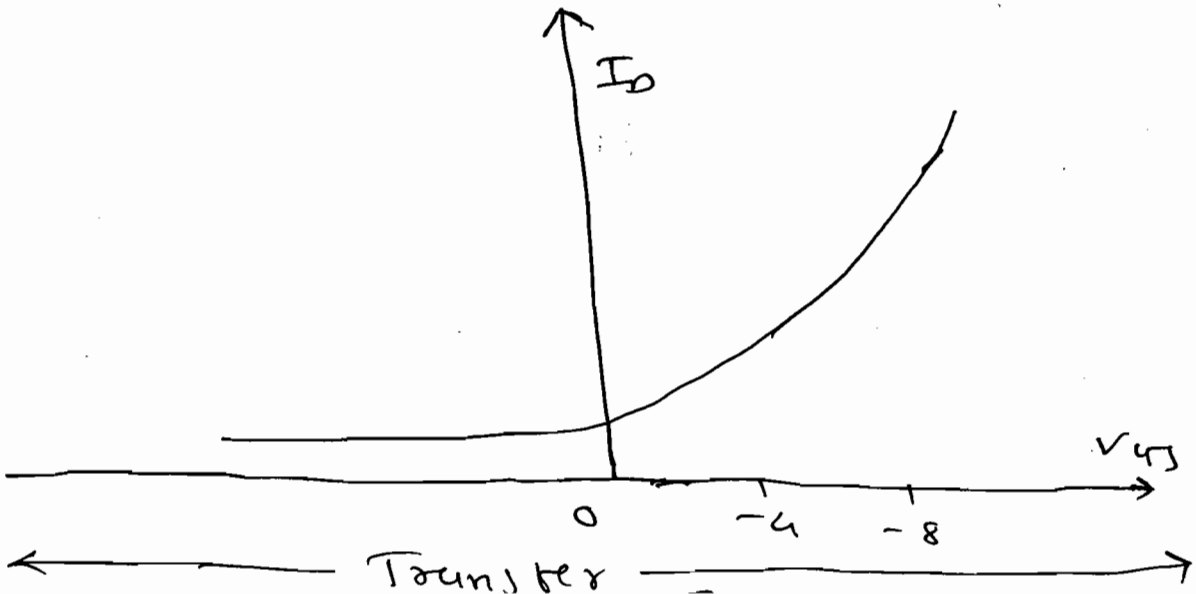
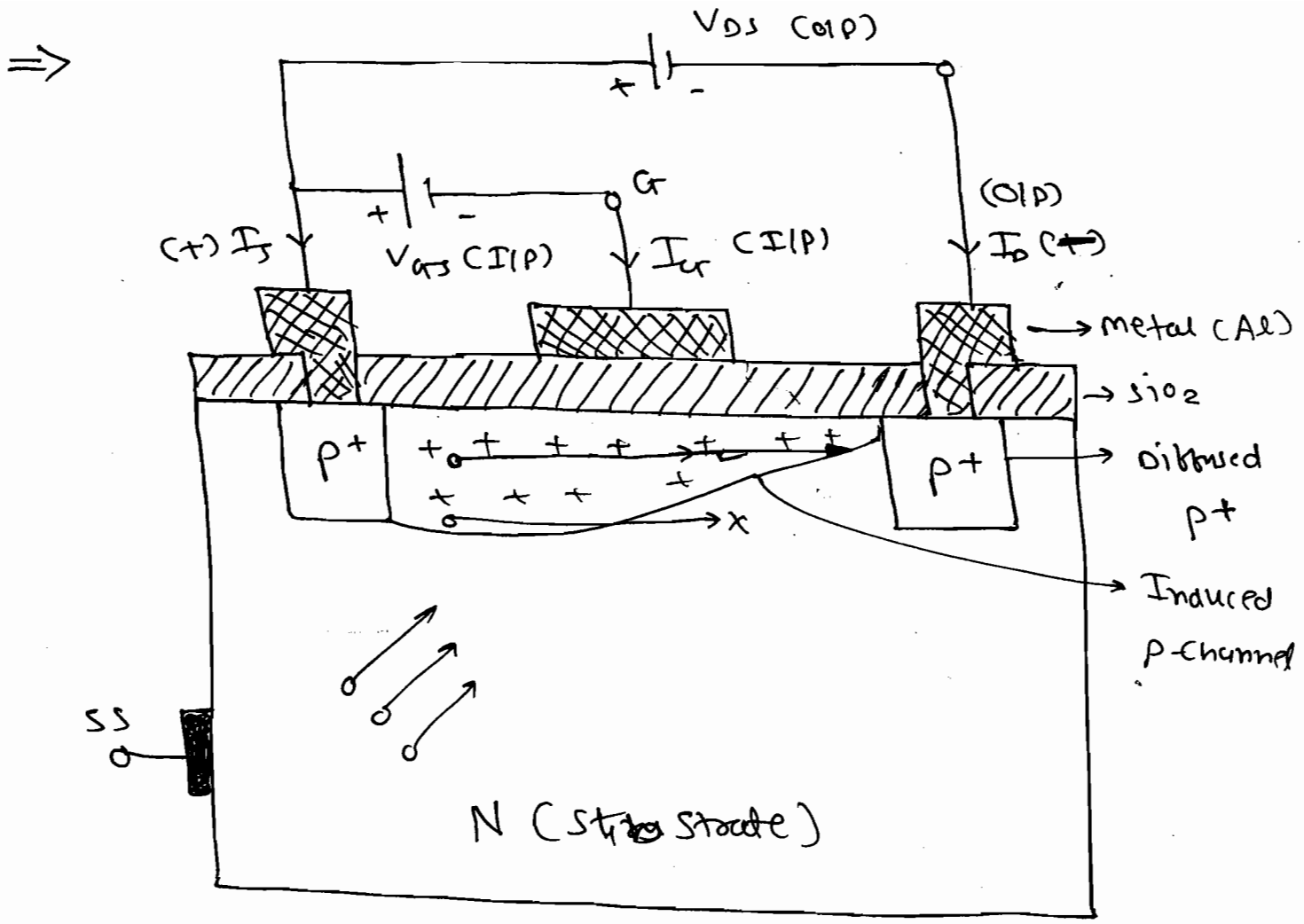
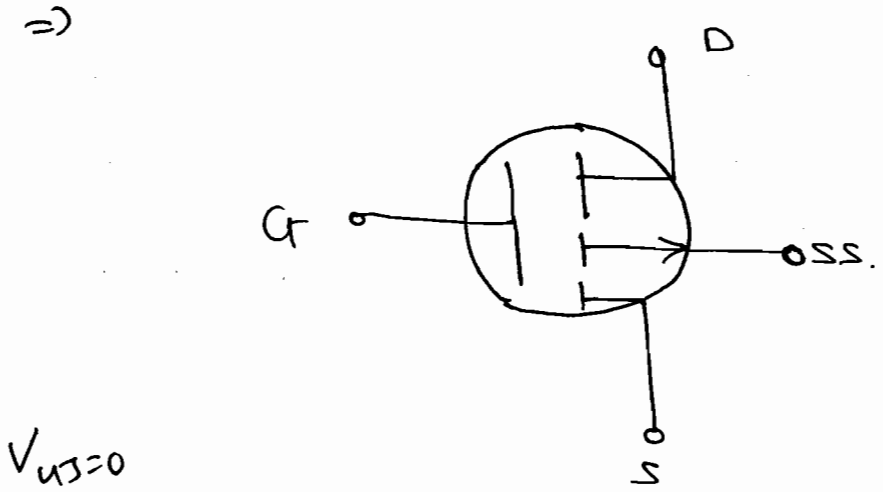
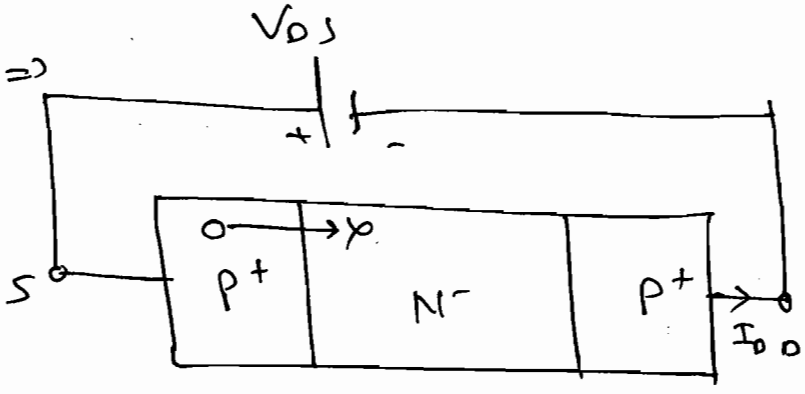


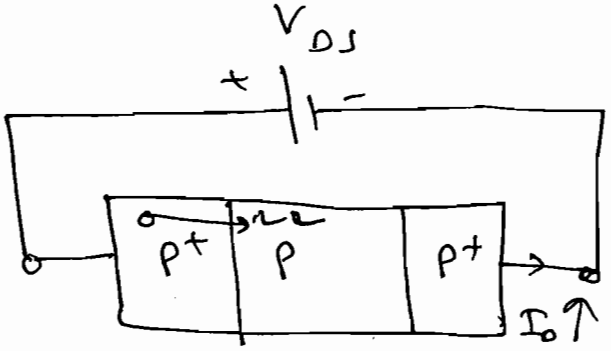

VDS (O/P)
+
-
G
(O/P)
(+) IS
VGS (I/P)
IG (I/P)
ID (+)
metal (Al)
SiO2
P+
P+
Diffused P+
X
Induced P-Channel
SS
N (Substrate)


D
G
SS.
S

$V_{GS}=0$

$V_{GS}=-ve$


VDS
+
-
P+
N-
P+
S
X
ID


VDS
+
-
P+
P
P+
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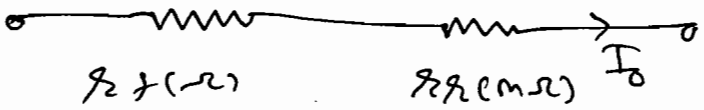
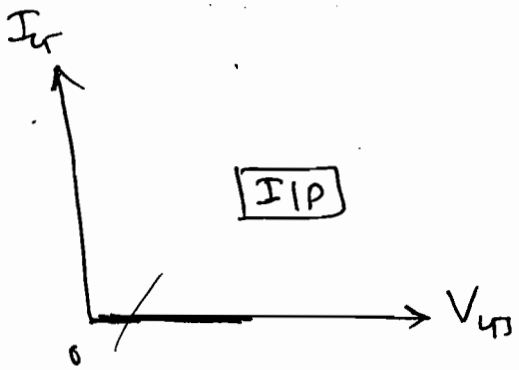

ID

$\Rightarrow V_{DS} = V_{DG} + V_{GS}$

$V_{DS} = -V_{GD} + V_{GS}$

$V_{GD} \downarrow = \boxed{V_{GS}} - V_{DS} \uparrow$

$\Rightarrow R_{GS} = \frac{V_{GS}}{I_G} = \infty.$ ($I_G \approx 0$)



$R = \frac{\rho l}{A}$

$\uparrow V_{DS} = \uparrow I_D R$

$\Rightarrow$ Device supports flow of only one charge carrier hence it is unipolar device. the voltage betn D & S V_{DS} is to be choosen such that charge carriers enter through source terminal into device and leave the device through drain terminal.

$\Rightarrow$ For $V_{GS} = 0$ diffused p^+ region and n^- substrate form diodes. For a given V_{DS} source diode is Forward bias and Drain diode is RB. hence $I_D = I_0$, very small current flows.

$\Rightarrow$ Even if V_{DS} increases $I_D = I_0$ will be

constant since n^- channel opposes the flow of charge carrier.

⇒ Sun V_{GS} is made -ve then holes of Substrate are pulled towards gate terminal but they can ~~not~~ reach gate due to insulating SiO_2 layer hence they gate accumulated beneath SiO_2 layer betn the two p^+ region called Induced p- channel. which supports flow of charge carriers hence drain current increases.

⇒ For the Same V_{DS} as earlier if V_{GS} becomes more and more -ve then Channel becomes more and more p-type. hence I_D increases called Enhancement type.

⇒ For a given value of V_{GS} Induced channel and diffussed areas act like a resistor across which a voltage V_D is given through which a current I_D flows as V_{DS} increases I_D increases linearly as shown in Ohmic region ~~(OR)~~ (OR)

→ Beyond a particular V_{DS} if V_{DS} further increases Pull exerted on the incoming holes to the drain side decreases hence holes get accumulated at source side hence height of induced channel at drain side becomes constant hence I_D becomes constant as in constant current region (CCR). maximum current is possible in CCR hence called Saturation region (SR). and hence (OR) becomes non-saturation region (NSR).

⇒ Device can be used as Voltage Variable Resistor (VVR) in CCR. by Varying V_{GS}.

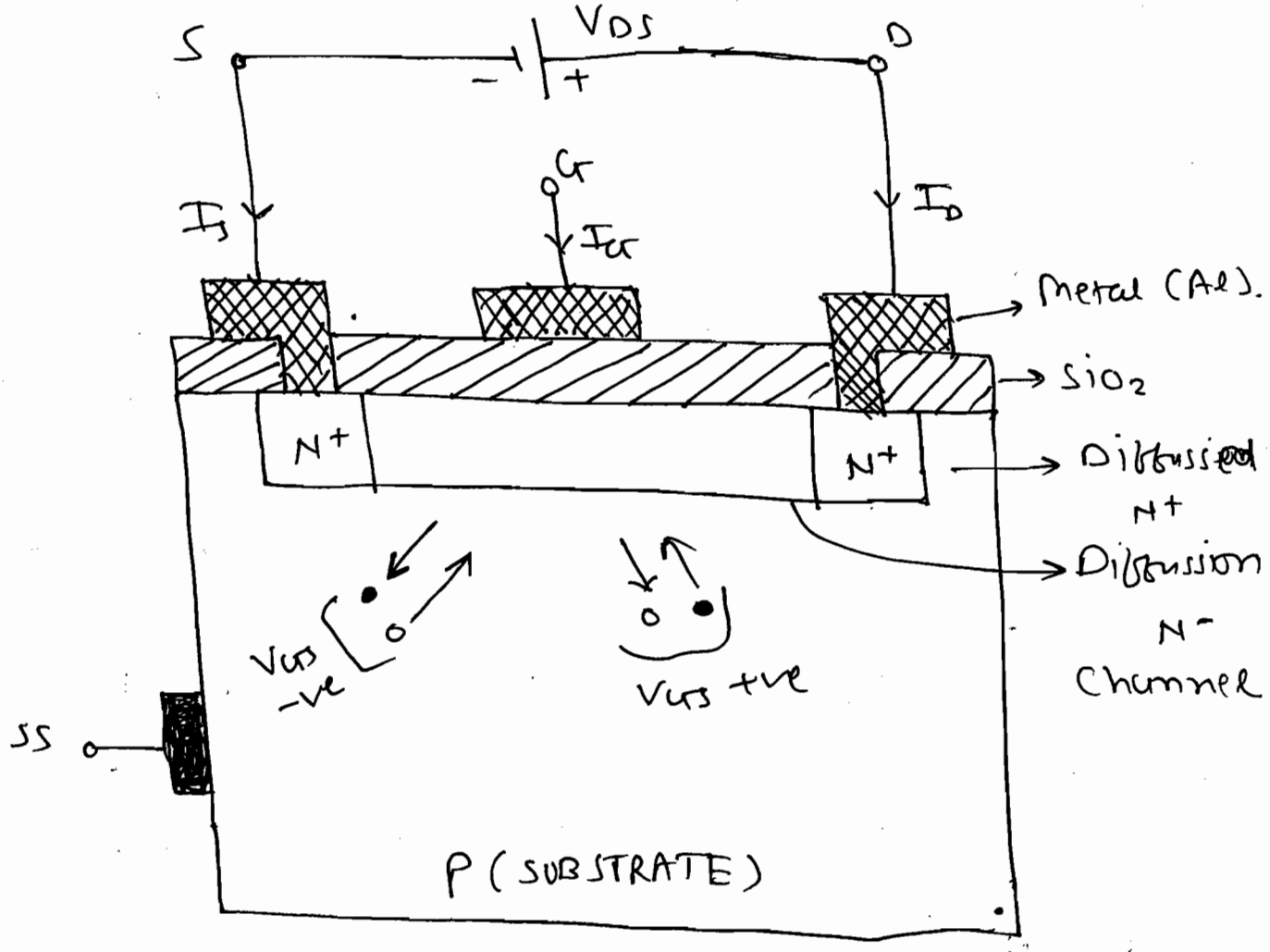
⇒ Input resistance $R_{GS} = \frac{V_{GS}}{I_G}$ ideally is infinity practically very high. since gate terminal is insulated by SiO_2 layer. As V_{GS}, increases input voltage increases input current I_G is constant and output current I_D increases hence It is Voltage Controlled Device.

⇒ Electric field developed across metal oxide semiconductor (MOS) is controlling the operation of a 3-terminal device hence called metal oxide semiconductor field Effect Transistor. (MOSFET).

⇒ Gate terminal is Insulated hence called insulated gate field effect Transistor. (IGFET).

* Enhancement cum Depletion N-Channel MOSFET:

⇒



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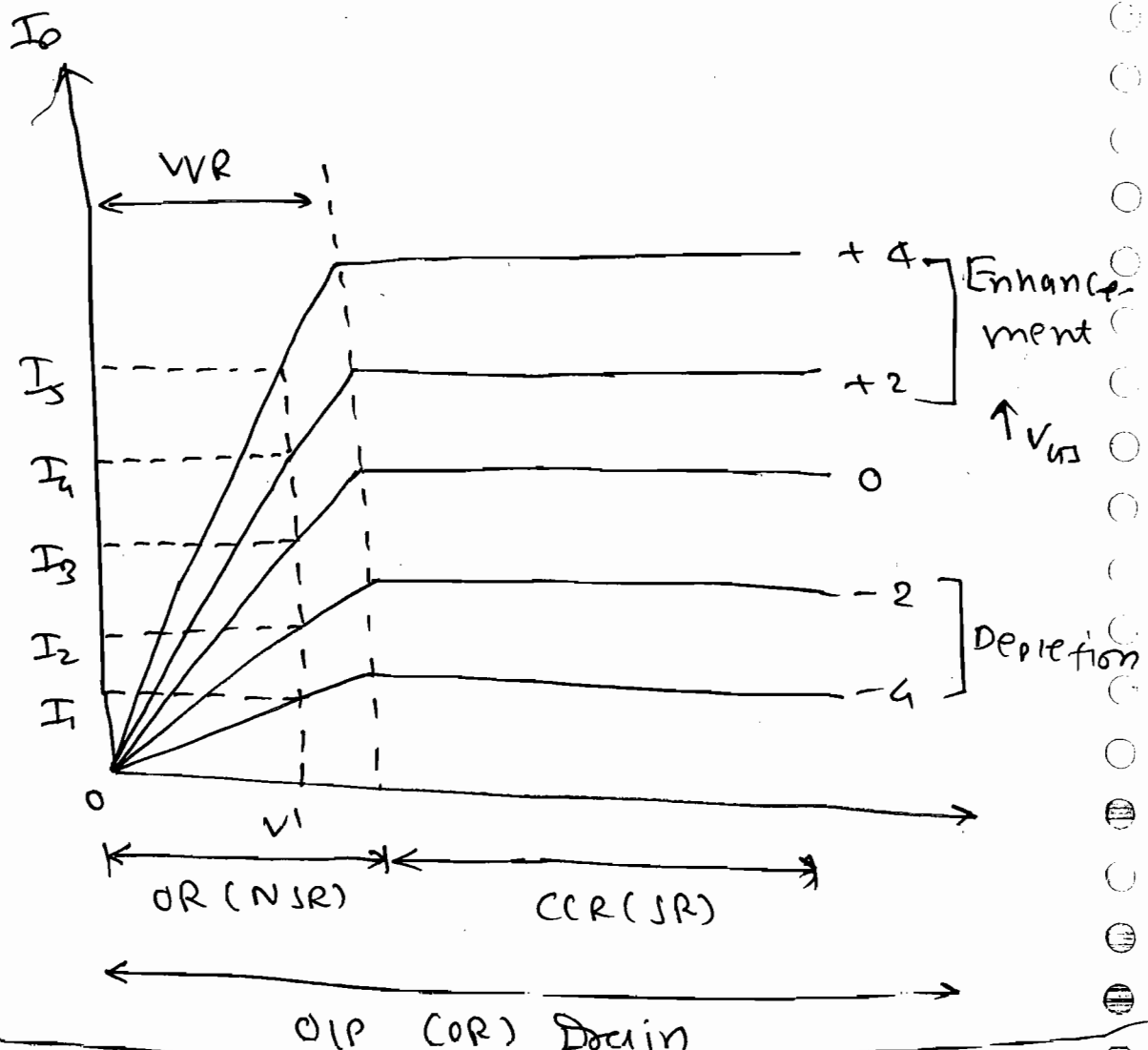
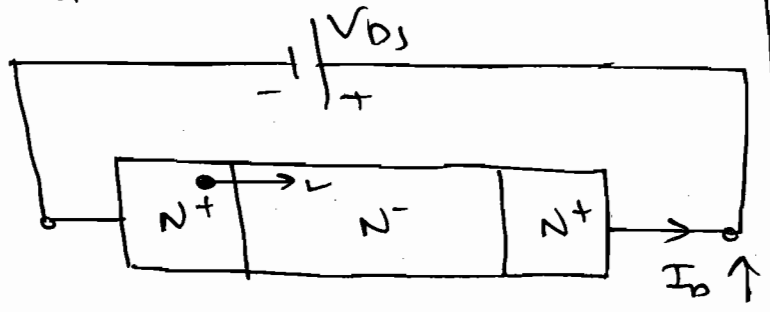


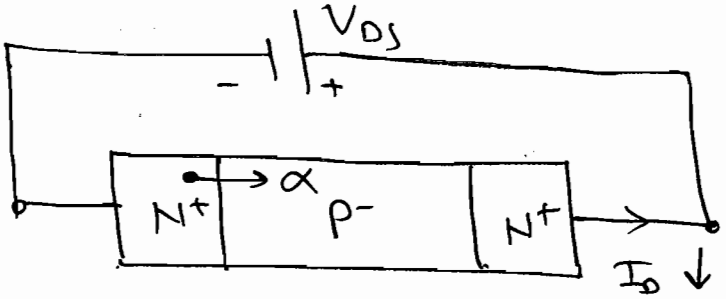
$V_{GS} = 0$

⇒



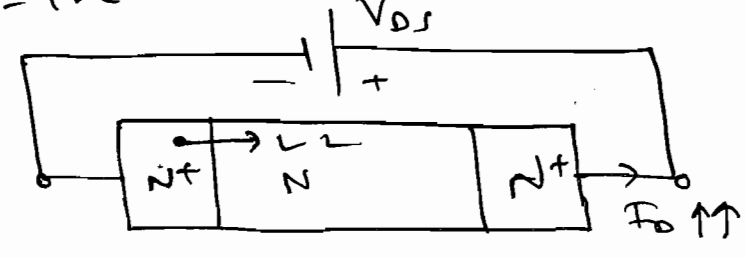
$V_{GS} = -ve$

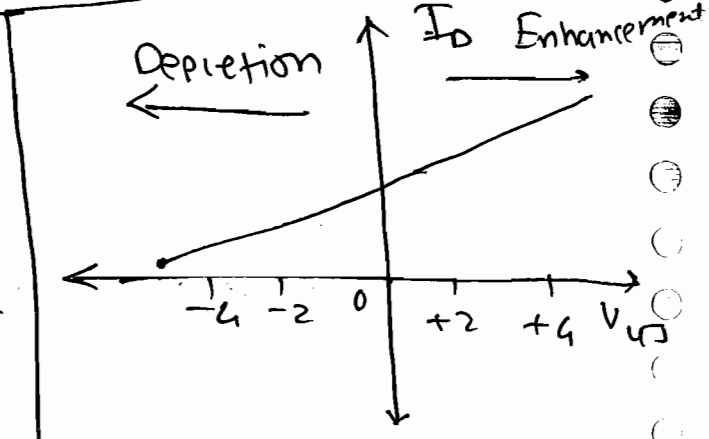
⇒



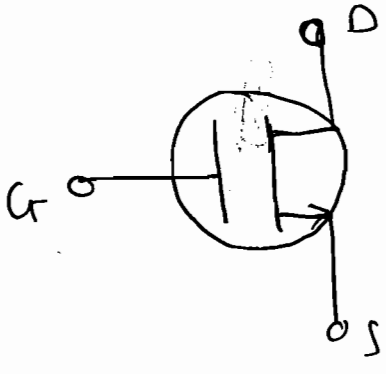
$V_{GS} = +ve$

⇒





Transfer



⇒ For $V_{GS}=0$, diffussed n- channel supports flow of charge carrier hence, a non-zero value of I_D is possible.

⇒ Say V_{GS} is made -ve then e^- of channel are zipped to substrate and holes of substrate are attracted to channel hence channel becomes p-type and opposses flow of charge carriers hence I_D decreases called depletion mode.

⇒ Say V_{GS} is made +ve then holes of channel are zipped to substrate and e^- of substrate attracted into channel hence channel becomes more n-type hence I_D increases called Enhancement mode.

* Applications:

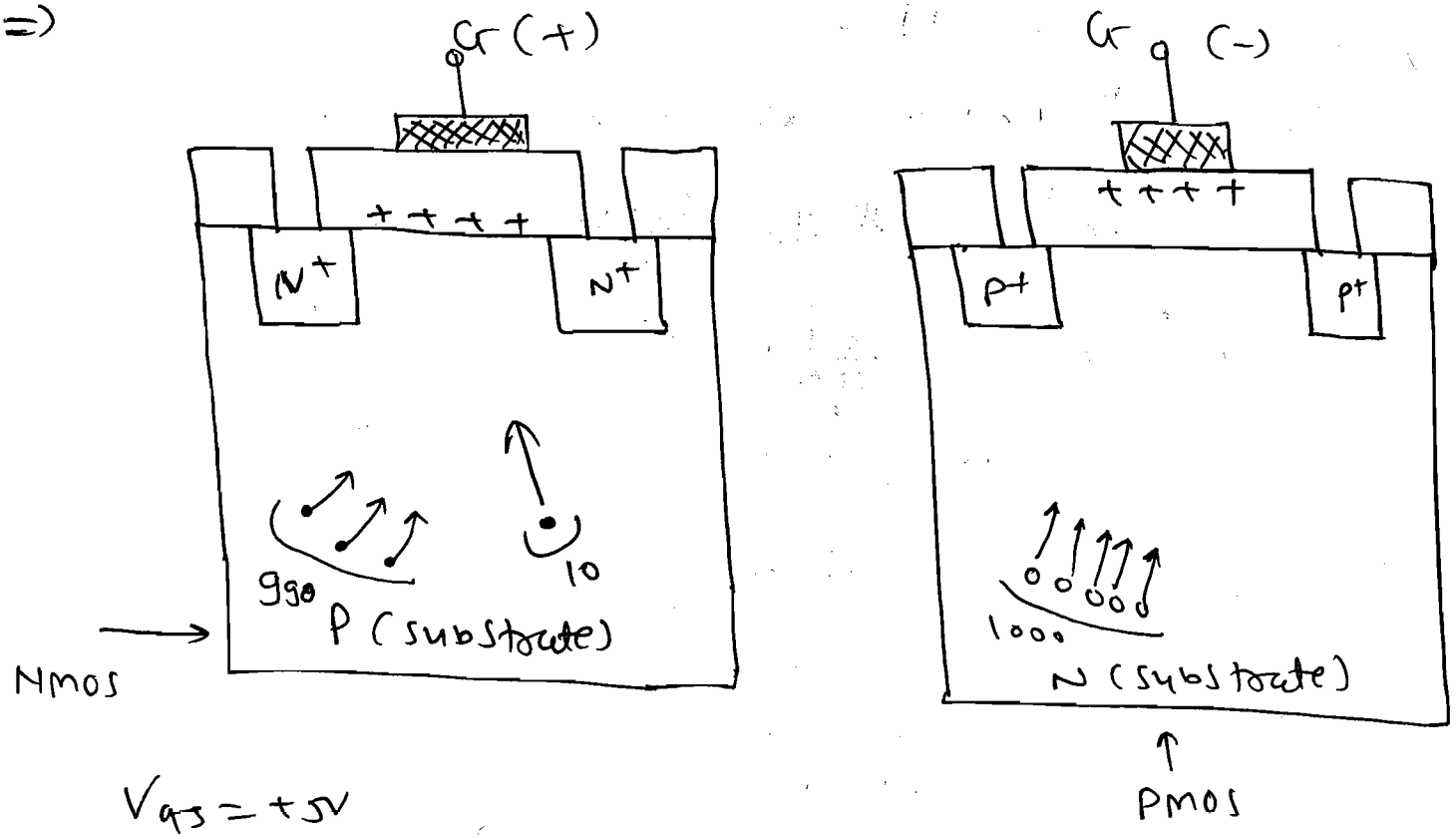
⇒ Voltage Variable Resistor.

⇒ Buffer.

⇒ memory element.

Note: In PMOS there is no [redacted]. Premature ON problem

⇒



$V_{GS} = +5V$

$V_{GS} = +4.9V$

"Premature ON"

$V_{GS} = -5V$.

⇒ During the Preparation of SiO_2 layer certain +vely charge impurities will get developed which where seen to effect the operation.

⇒ In NMOS V_{GS} +ve will ripple the impurities hence they move the bottom surface of SiO_2 layer. and attract charge carriers into channel and make the device to get switched ON at a voltage prior to designed voltage called 'premature ON' problem.

⇒ In PMOS V_{GS} -ve attracts impurities hence they move to top surface of SiO_2 layer. They can not affect incomming charge carriers hence device gets switched on at designed voltage.

Q An n-channel JFET has $I_{DSS} = 8mA$ $V_{GS(OFF)} = -5V$. Calculated minimum voltage bet^n D & S for pinch off. and drain current given $V_{GS} = -2V$.

Soln:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2.$$

$$V_P = V_{GS(OFF)} = -5V.$$

$$\therefore I_D = 8\left[1 - \frac{(-2)}{(-5)}\right]^2.$$

$$\boxed{I_D = 2.88mA}$$

$$\therefore V_{DS} + V_P = V_{GS}$$

$$V_{DS(min)} = V_{GS} - V_P$$

$$= -2 - (-5).$$

$$\boxed{V_{DS(min)} = +3V}$$

(a) Gate current is 1nA when a reverse gate Voltage of 12 V is applied to FET. R_{GS} (in) in MΩ is.

Soln:

$$R_{GS} = \frac{V_{GS}}{I_G} = \frac{12}{1 \times 10^{-9}} = 12 \times 10^9 \ \Omega$$

$$R_{GS} = 12 \times 10^3 \ M\Omega.$$

(a) For n-channel Silicon FET given half channel height 3×10^{-4} cm. Calculate effective half channel height b given $V_{GS} = V_P/2$.

Soln:

$$V_{GS} = (1 - b/a)^2 V_P$$

$$\therefore \frac{1}{2} = (1 - b/a)^2$$

$$b/a = 1 - 0.707$$

$$b = 0.878 \times 10^{-4} \text{ cm.}$$

(a) Pinch-off Voltage for n-channel FET given a $a = 2 \times 10^{-4}$ cm

$$N_D = 125 \times 10^{13} \text{ cm}^{-3}.$$

$$\epsilon = 106.188 \times 10^{-14} \text{ F/cm.}$$

Soln:

$$V_p = -\frac{qN_a a^2}{2\epsilon}$$

$$V_p = -\frac{1.6\times10^{-19} \times 125\times10^{13} \times 4\times10^{-8}}{2\times106.88\times10^{-14}}$$

$$\therefore \boxed{V_p = -3.74\ V}$$