

# COMPUTER ORGANIZATION AND ARCHITECTURE TEST 3

Number of Questions: 35

Section Marks: 30

**Directions for questions 1 to 35:** Select the correct alternative from the given choices.

1. A computer 'A' uses the following 32-bit floating point representation of real numbers.



Computer 'B' uses the following floating point representation scheme.



Which of the following statement is TRUE with regard to computer B's method of representing floating-point numbers over computer A's method?

- (A) Both range and precision are decreased.  
 (B) The range is decreased but the precision is increased.  
 (C) The range is increased but the precision is decreased.  
 (D) Both range and precision remain same.
2. The minimum number of control bits required to execute a microprogram which has 50 control signals is \_\_\_\_\_.
- (A) 5 (B) 6  
 (C) 50 (D) 100
3. Consider the following instructions:  
 BEQ  $R_0, R_1, L_1$   
 The opcode is BEQ, which means Branch if Equal. The instruction checks the equality of  $R_0, R_1$  and if both are equal jump to  $L_1$ . Which of the following correctly specifies given instruction but with much greater branching distance?
- (A) compare  $R_0, R_1$  if zero jump to  $L_1$   
 (B) LOAD  $R_0$  Branch if equal  $R_1, L_1$   
 (C) Branch if not equal  $R_0, R_1, L_2$  Jump  $L_1 L_2$ :  
 (D) Branch if not Equal  $R_0, R_1, L_1$  Jump  $L_2 L_1$ :
4. Consider a loop branch that branches 100 times in a row, then it is not taken once. Assume that the prediction bit for this branch remains in the prediction buffer. The prediction accuracy for this branch by using 1-bit branch history table prediction scheme (in percentage) is \_\_\_\_\_.
- (A) 90 (B) 95  
 (C) 98 (D) 99
5. The biased exponent value for double precision floating point numbers is \_\_\_\_\_.
- (A) 1023 (B) 1024  
 (C) 256 (D) 255

6. Consider the following instruction:

ADD  $R_1, (R_2, R_3)$

Here  $R_1, R_2, R_3$  are registers

The Sum of data present in the  $R_2$  and  $R_3$  is stored in a 32-bit register  $R_1$ .

Which of the following mode best reflects the mode of second operand?

- (A) Indexed mode  
 (B) Base Register mode  
 (C) Base with index mode  
 (D) Base with index and offset mode
7. Consider an instruction format with fields containing zeros:

0000	0000 0000	0000 0000	0000 0000 0000
Opcode	Destination Register	Source Register	Immediate value

What is the maximum possible number of operations, registers with the given instruction format?

- (A) 4, 8 (B) 4, 16  
 (C) 16, 256 (D) 16, 65536
8. A 64 M-bit DRAM organized as 4 M addresses of 16-bit words each. A memory system is built using 128 M addresses of 256-bit words each. How many DRAM chips that are required for this memory system?
- (A) 16 (B) 32  
 (C) 128 (D) 512
9. Consider a hypothetical 64-bit micro-processor having 64-bit instructions composed of two fields: Opcode: 2-bytes. Immediate operand or an operand address: remaining bytes.  
 What is the maximum directly addressable memory capacity (in bytes)?
- (A)  $2^{16}$  (B)  $2^{48}$   
 (C)  $2^{64}$  (D)  $2^{24}$
10. Consider a machine with a byte addressable main memory of 4 GB and a block size of 16 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine. How many bytes of main memory can be stored in the cache?
- (A) 4096 (B)  $2^{20}$   
 (C) 512 (D) 736
11. Consider a dynamic RAM that must be given a refresh cycle 64 times per ms. Each refresh operation requires 150 ns; a memory cycle requires 250 ns. What percentage of the memory's total operating time is given to refreshes?
- (A) 1% (B) 3%  
 (C) 5% (D) 10%
12. A DMA module is transferring characters to memory using cycle stealing, from a device transmitting at

9600 bps. The processor is fetching instructions at the rate of 1 million instructions per second (1 MIPS). By how much the processor is slowed down due to the DMA activity?

- (A) 0.0012% (B) 0.01%  
(C) 0.001% (D) 0.12%

13. Match list-A with list-B and select the correct answer using the code given below the list:

	List-A		List-B
a.	Cache	1.	Printer
b.	DMA I/O	2.	Disk
c.	Interrupt I/O	3.	High speed RAM

- (A) a-1, b-2, c-3 (B) a-2, b-3, c-1  
(C) a-3, b-2, c-1 (D) a-3, b-1, c-2

14. The speed gained by a 'p' segment pipeline executing 'q' tasks is:

- (A)  $\frac{(q+p-1)}{pq}$  (B)  $\frac{p+q}{pq-1}$   
(C)  $\frac{pq}{p+q-1}$  (D)  $\frac{p+q}{pq+1}$

15. The IEEE 32-bit floating point format of -6 is:

- (A) 1 10000001 100000000000000000000000  
(B) 1 00000010 000000000000000000000000  
(C) 1 00000001 100000000000000000000000  
(D) 1 10000001 000000000000000000000000

16. Consider below code segment:

```
LOAD R1, M[1000]
LOAD R2, M[1002]
ADD R3, R1, R2
STORE R3, M[1008]
LOAD R4, M[1004]
ADD R5, R1, R4
STORE R5, M[1010]
```

Assume that this program is executed on a pipelined processor with 5 stages: FI (Fetch Instruction), RD (Read registers while Decoding), EX (Execute the operation or calculate the address), MEM (Access an operand in data memory), WR (write result into a register).

The first operand of each instruction will be the destination. What is the minimum number of stalls that will be there in the reordered code of given code if the processor uses forwarding also?

- (A) 0 (B) 1  
(C) 2 (D) 3

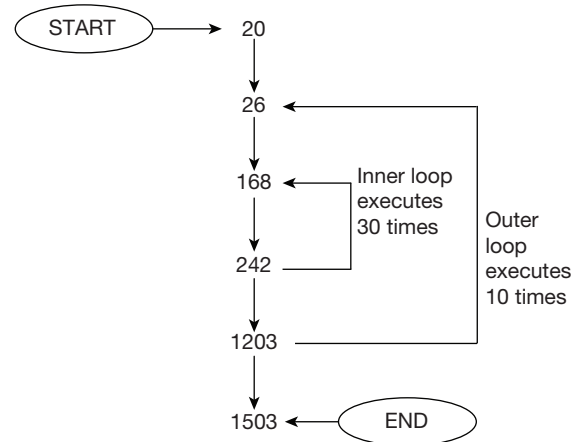
17. Consider a  $2 \times 8$  two-dimensional array of elements,  $M$ . Assume that each element in the array occupies one word and the array elements are stored in column-major order in the main memory from location 2000 to location 2015. The cache consists of 8 blocks and each block will have just two words. Assume also that

whenever needed, LRU replacement policy can be used. What is the percentage of cache utilization for Direct mapped, Associative and 2-way set-Associative respectively, if the processor accesses the following elements?

$M_{0,0}, M_{0,1}, M_{0,2}, M_{0,3}, M_{0,4}, M_{0,5}, M_{0,6}, M_{0,7}, M_{1,0}, M_{1,1}, M_{1,2}, M_{1,3}, M_{1,4}, M_{1,5}, M_{1,6}, M_{1,7}$ .

- (A) 50%, 100%, 50% (B) 50%, 50%, 50%  
(C) 100%, 100%, 100% (D) 100%, 100%, 50%

18. Consider the given program structure, which is in Main memory:



The memory addresses are in decimal. The program consists of two loops along with start and end statements. All the instructions in the program are executed in sequential manner. The program is to be run on a computer that has an instruction cache of size 1 K words organized in a direct-mapped manner. The main memory size is 64 K words with block size of 128 words. Let the cycle time of main memory is 10 ns and cycle time of the cache is 1 ns.

Then the total time needed for reading instructions from main memory to the cache during the execution of the program (in nano seconds) is \_\_\_\_\_.

- (A) 1280 (B) 4864  
(C) 48640 (D) 61440

19. A pipelined processor has two branch delay slots. An optimizing compiler can fill one of these slots 75% of the time and can fill the second slot only 20% of the time. What is the ratio of improvement in performance achieved by this optimization to without optimization, assuming that 10% of the instructions executed are branch instructions?

- (A) 1.102 (B) 1.086  
(C) 0.9 (D) 1.105

20. Consider a system with a 4 KB, 4-way set associative cache memory with 128 lines, a 1024 word array where each element is a 32-bit word. When a program accesses this array with a scale of  $D$ , it means starting with the first element, the program accesses every

$D^{\text{th}}$  element. For example, for  $D = 1$ , the program accesses every element, for  $D = 2$ , the program accesses every second element and so on. Assuming a cache that is initially empty and a program makes one pass over this array with a scale of  $D$ , what is the miss rate generated for  $D = 8$ ?

- (A)  $\frac{1}{2}$  (B)  $\frac{1}{4}$   
(C)  $\frac{1}{8}$  (D)  $\frac{1}{16}$

21. A computer has 32-bit instructions and 12-bit addresses. If there are 240 two-address instructions, how many one-address operations can be formulated?

- (A) 4096 (B) 65536  
(C) 8192 (D) 131072

22. Consider a pipelined processor with a 5-stage pipeline. Assume that all instructions take 5 cycles. The dynamic instruction count by type, as a percentage of the total, is as follows:

10% store instructions  
20% load instructions  
30% branch instructions  
40% ALU instructions

What is the ideal speed-up due to pipelining for this processor?

- (A) 2.5 (B) 5  
(C) 10 (D) 50

23. For the data given in Q. No. 22, let stalls due to data hazards occur only under two reasons.

A stall of two cycles occur when a load instruction is followed by an ALU instruction that uses the result of load. This scenario exists for 40% of the load instructions.

A stall of three cycles occur when a branch instruction is preceded by an ALU operation whose result is used as a branch condition. This scenario exists for 50% of the branch instructions. What is the decrease in the ideal speed up of pipelining only due to data hazards?

- (A) 50% (B) 75.6%  
(C) 18.9% (D) 37.8%

24. Given

$x = (0100\ 0110\ 1101\ 1000\ 0000\ 0000\ 0000\ 0000)_2$  and  
 $y = (1011\ 1110\ 1110\ 0000\ 0000\ 0000\ 0000\ 0000)_2$ ,  
representing single precision IEEE 754 floating point numbers. Then the respective values of  $x + y$  and  $x * y$  in decimal (approximately) are:

- (A) 27647.5625 and -12096  
(B) 27647.5625 and -24192  
(C) 13823.75 and 24192  
(D) 13823.75 and -24192

25. A 5-stage pipeline has the following stages:

IF: Instruction fetch

ID: Instruction decode and register file read

EX: Execution or address calculation

MEM: Data memory access

WB: Write back

The following code executed on this pipeline:

Instruction	Operation
ADD $R_1, R_2, R_3$	$R_1 \leftarrow R_2 + R_3$
SUB $R_4, R_1, R_5$	$R_4 \leftarrow R_1 - R_5$
LOAD $R_6, 200(R_1)$	$R_6 \leftarrow M[200 + R_1]$
ADD $R_7, R_1, R_6$	$R_7 \leftarrow R_1 + R_6$

Use forwarding to resolve data hazards. Then the number of stalls that will occur because of data hazards in given code is \_\_\_\_.

- (A) 0 (B) 1  
(C) 2 (D) 3

26. Consider a floating point representation:  $c.r^e$  where  $c$  represents coefficient register of size 10 in which MSB bit is used to represent sign,  $r$  represents radix and  $e$  represents contents of exponent register of size 5, in which MSB is used to represent sign. Then the contents of coefficient and exponent registers for the number +1001.110 will be:

- (A) 0100111000, 00100 (B) 0001001110, 00100  
(C) 1001110000, 10100 (D) 1001110000, 10101

27. Consider a 32-bit microprocessor, with a 16-bit external data bus, driven by an 8 MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles. What is the minimum data transfer rate across the bus that this microprocessor can sustain, in bytes?

- (A) 2 MB/sec (B) 4 MB/sec  
(C) 6 MB/sec (D) 8 MB/sec

28. Consider a bus structure in which a single internal bus connects the ALU and all processor registers.

Which of the following represents the correct sequence of micro-operations to add a number to the accumulator when the number is an indirect address operand?

- (A)  $t_1: \text{MAR} \leftarrow (\text{IR}(\text{address}))$   
 $t_2: \text{MBR} \leftarrow \text{memory}$   
 $t_3: Y \leftarrow (\text{MBR})$   
 $t_4: Z \leftarrow (AC) + (Y)$   
 $t_5: AC \leftarrow (Z)$   
(B)  $t_1: \text{MAR} \leftarrow (\text{IR}(\text{address}))$   
 $t_2: \text{MBR} \leftarrow \text{memory}$   
 $t_3: Z \leftarrow (AC) + (\text{MBR})$   
 $t_4: AC \leftarrow (Z)$   
(C)  $t_1: \text{MBR} \leftarrow (\text{IR}(\text{address}))$   
 $t_2: Z \leftarrow (AC) + (\text{MBR})$   
 $t_3: AC \leftarrow (Z)$   
(D)  $t_1: \text{MAR} \leftarrow (\text{IR}(\text{address}))$   
 $t_2: \text{MBR} \leftarrow \text{memory}$   
 $t_3: \text{MAR} \leftarrow (\text{MBR})$   
 $t_4: \text{MBR} \leftarrow \text{memory}$

$t_5: Y \leftarrow (MBR)$   
 $t_6: AC \leftarrow (AC) + (Y)$   
 $t_7: AC \leftarrow (Z)$

29. For the data given in Q. No. 28, what is the number of clock cycles required for above operation if each micro-operation takes one clock cycle?  
 (A) 5 (B) 4  
 (C) 3 (D) 7
30. The access time of a cache memory is 100 ns and that of main memory is 1  $\mu$ s. 80% of the memory requests are for read and others are for write. Hit ratio for read only accesses is 0.9. A write-through procedure is used. The average access time of the system for both read and write requests is:  
 (A) 160 ns (B) 200 ns  
 (C) 360 ns (D) 720 ns
31. Consider a new instruction named branch-on-bit-set. The instruction  
 “bbs reg, pos, label”  
 jumps to label if bit in position ‘pos’ of register oper- and ‘reg’ is one. A register is 32 bits wide and the bits are numbered 0 to 31, bit in position 0 being the least significant. Consider the following emulation of this instruction on a processor that does not have branch-on-bit-set implemented.  
 result  $\leftarrow$  reg & mark  
 Branch to label if result is non-zero.  
 The variable ‘result’ is temporary register. For correct emulation the variable mask must be generated by:  
 (A) mask  $\leftarrow 0xf$  (B) mask  $\leftarrow pos$   
 (C) mask  $\leftarrow 0xffff \gg pos$  (D) mask  $\leftarrow 0x1 \ll pos$
32. Consider a computer with the following characteristics: Total main memory: 1 MB; word size is 1 byte; Block size of 16 bytes; and cache size of 64 kbytes; for the main memory address F0010, what will be the cache line bits for a direct mapped cache?  
 (A) 1111 (B) 0000  
 (C) 0000 0000 0001 (D) 000000001000
33. Consider a system in which a data transfer over a bus takes 500 ns. Transfer of bus control in either direction, from processor to I/O device or vice versa, takes 250 ns. One of the I/O devices has a data transfer rate of 50 kb/s and employs DMA. Data is transferred one byte at a time. Suppose we employ DMA in a cycle-stealing mode. When transferring a block of 128 bytes, it would tie up the bus for (in micro seconds) \_\_\_\_\_.  
 (A) 250 (B) 0.2  
 (C) 128 (D) 0.4
34. A PC relative mode branch instruction is 2 bytes long. The address of the instruction, in decimal, is 356029. Determine the branch target address if the signed displacement in the instruction is -31.  
 (A) 356029 (B) 356030  
 (C) 356031 (D) 356000
35. Consider a system employing interrupt driven I/O for a particular device that transfers data on an average of 10 KB/sec on a continuous basis. Assume that interrupt processing takes 100  $\mu$ s (i.e., the time to jump to the ISR, execute it and return to the main program). Determine what fraction of processor time is consumed by this I/O device if it interrupts for every byte.  
 (A) 1 (B) 10  
 (C) 100 (D) 0.8

### ANSWER KEYS

- |       |       |       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 1. B  | 2. B  | 3. C  | 4. C  | 5. A  | 6. C  | 7. C  | 8. D  | 9. B  | 10. C |
| 11. A | 12. D | 13. C | 14. C | 15. A | 16. A | 17. C | 18. D | 19. B | 20. B |
| 21. B | 22. B | 23. D | 24. A | 25. B | 26. A | 27. B | 28. D | 29. D | 30. C |
| 31. D | 32. C | 33. D | 34. D | 35. A |       |       |       |       |       |

### HINTS AND EXPLANATIONS

- The range of a floating point number depends on exponent size. As exponent size in ‘B’ decreases, the range also decreases.  
 The precision specifies number of digits after decimal point, which increases in ‘B’ computer. Choice (B)
- Using Vertical Microprogramming, there will be 6-control bits to provide 50 control signals.  
 ( $\because 2^6 = 64 > 50$ ) Choice (B)
- Given instruction BEQ  $R_0, R_1, L_1$ .  
 This instruction can be replaced by following instructions, to achieve greater branching distance:  
 BNE  $R_0, R_1, L_2$   
 Jump  $L_1, L_2$ :  
 We get much greater branching distance by using 1-address instruction: Jump  $L_1$ .  
 We can’t use zero-address as we need to specify the opcode ‘jump’  
 By using the instruction ‘Jump  $L_1$ ’ the address space is more so we can specify much greater branching distance. Choice (C)
- Branch history table is a small memory, which contains a bit that says whether the branch was recently taken or not.

In the given problem, the loop executes 100 times but in the 101<sup>th</sup> time the loop is not taken.

But it will be incorrectly predicted by 1-bit branch history table prediction as the loop is taken for 100 times. In the 1<sup>st</sup> iteration also the predictor specifies incorrect branch prediction as the bit is set to 'not taken' in the exit stage of last execution of the program.

∴ 2 wrong predictions, out of 101 predictions.

∴ Prediction Accuracy percentage

$$= \frac{99}{101} \times 100 = 98\% \quad \text{Choice (C)}$$

5. In Double precision floating point format,

Number of bits for exponent = 11

∴ Biased exponent =  $2^{k-1} - 1$ ,

Where  $k$  is the number of bits used for exponent.

Here  $k = 11$ , hence Biased exponent

$$= 2^{10} - 1 = 1023. \quad \text{Choice (A)}$$

6. If we assume  $R_2$  as Base register,  $R_3$  as Index register, then the mode will be Base with index mode.

Choice (C)

7. Number of bits in opcode = 4

⇒ Number of operations possible =  $2^4 = 16$

Number of bits in src/dest. Registers = 8

∴ Number of registers =  $2^8 = 256$  Choice (C)

8. Each DRAM has  $4M$  addresses of 16-bit words.

⇒ DRAM capacity =  $4M \times 16$

Memory system capacity =  $128M \times 256$

$$\therefore \text{Number of chips required} = \frac{128M \times 256}{4M \times 16} = 512$$

Choice (D)

9. Instruction size = 64-bits

Opcode size =  $2B = 16$ -bits

Operand/Address field =  $64 - 16 = 48$ -bits.

The 48-bits can be used to specify a particular address.

∴ Maximum directly addressable memory =  $2^{48}$

Choice (B)

10. Number of lines in cache = 32

There are 32 lines in cache. Each line will have 16 bytes.

∴ Total bytes of memory in cache

$$= 16 \times 32 = 512 \text{ bytes} \quad \text{Choice (C)}$$

11. The DRAM has given a refresh cycle 64 times per ms.

Time required for one refresh operation = 150 ns

In 1 ms, the time required to refresh is  $64 \times 150 \text{ ns} = 9600 \text{ ns}$

∴ The fraction of time devoted to memory refresh is

$$\frac{9600 \times 10^{-9}}{10^{-3}} = 0.0096$$

∴ Approximate percentage of the memory's total operating time given to refreshes is 1%.

Choice (A)

12. The DMA is transmitting at a rate of 9600 bits per second i.e., it is transmitting  $\frac{9600}{8} = 1200$  characters

per second. The processor is processing at a rate of 1 million instructions per second i.e., It will take

$$\frac{1}{10^6} = 1\mu \text{ second to process a single instruction.}$$

A single character will be processed by DMA in

$$\frac{1}{1200} \approx 833 \mu\text{s}$$

∴ Slow down of processor due to DMA

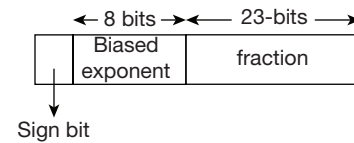
$$= \frac{1}{833} \times 100 = 0.12\% \quad \text{Choice (D)}$$

13. Cache is high speed RAM, DMA I/O is used with disk, Interrupt I/O is used with printer. Choice (C)

14. Without pipelining, execution time =  $pq$   
with pipelining, execution time =  $p + q - 1$

$$\therefore \text{speed up} = \frac{pq}{p + q - 1} \quad \text{Choice (C)}$$

15. IEEE 32-bit floating point representation will be in the form of:



$$6 = 110$$

For  $-6$  sign bit is 1.

$$6 = 110 = 1.10 \times 2^{010}$$

Exponent = 010

Biased exponent =  $127 + 2 = 129 = 10000001$

Fraction = 100000000000000000000000

Hence IEEE 32-bit floating point representation of  $-6$  is:

110000001

100000000000000000000000

Choice (A)

16. In given code stalls occur before the ADD instructions. 2 stalls are there in given code. To minimize stalls, we reorder the code. In the reordered code place LOAD  $R_4$ ,  $M[1004]$  before ADD  $R_3$ ,  $R_1$ ,  $R_2$ .

The resultant code will be:

LOAD  $R_1$ ,  $M[1000]$

LOAD  $R_2$ ,  $M[1002]$

LOAD  $R_4$ ,  $M[1004]$

ADD  $R_3$ ,  $R_1$ ,  $R_2$

ADD  $R_5$ ,  $R_1$ ,  $R_4$

STORE  $R_3$ ,  $M[1008]$

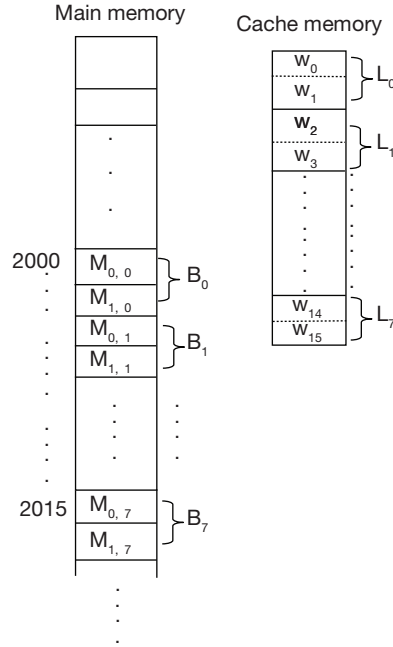
STORE  $R_5$ ,  $M[1010]$

No stalls in the reordered code.

Choice (A)

17. The Array  $M_{2 \times 8}$  is stored in column-major order in the main memory, i.e.,





In direct mapping,  $B_0$  is placed in  $L_0$ ,  $B_1$  in  $L_1$ ,  $B_2$  in  $L_2$ , ...,  $B_7$  in  $L_7$  to access the elements  $M_{0,0} - M_{0,7}$ . The remaining elements are already in cache. All those accesses will be hits.

As all the 8-blocks used, cache utilization is 100%. In Associative mapping, each block of main memory will be placed at anywhere in the cache lines. Also 8-accesses will be misses and the remaining will be hits. No need of replacement and all lines of cache will be used.

∴ Cache utilization = 100%

In 2-way set-Associative mapping, two blocks will be treated as a single set. There will be 4-sets.

Cache memory

$L_0L_1$	Set 0
$L_2L_3$	Set 1
$L_4L_5$	Set 2
$L_6L_7$	Set 3

All the four sets are used. Set 0 consists  $B_0$ ,  $B_4$ , set 1 contains  $B_1$ ,  $B_5$ . Like this all sets are used. Hence cache utilization is 100%. Choice (C)

18. Given main memory size =  $64 \text{ K} = 2^{16}$  words

Block size =  $128 = 2^7$  words

Cache size =  $1 \text{ K} = 2^{10}$  words

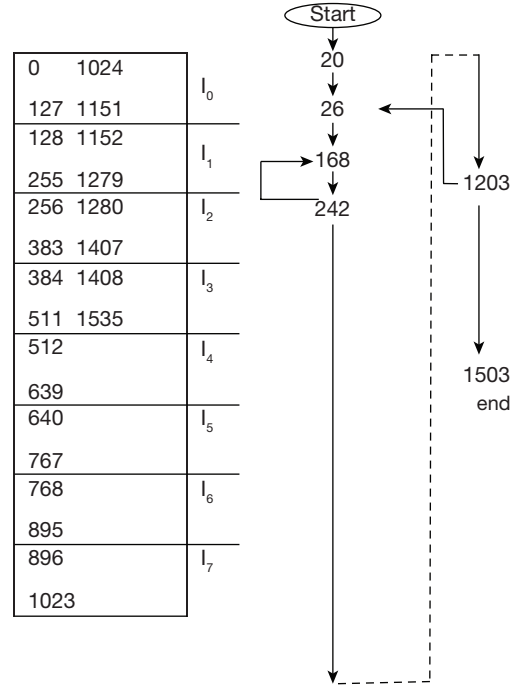
Word field size = 7

$$\text{Number of lines} = \frac{2^{10}}{2^7} = 2^3$$

∴ Line field size = 3

$$\Rightarrow \text{Tag} = 16 - (7 + 3) = 6$$

The cache memory is shown below with main memory block addresses.



Hence the sequence of reads from the main memory blocks into cache line is:

Line: 0, 1, 2, 3, 4, 5, 6, 7, 0, 1, 0, 1, ... 0, 1, 0, 1, 2, 3  
 Pass 1 outer loop      Pass 2      Pass 10

i.e., in pass1 of outer loop the lines 0, 1, 2, 3, 4, 5, 6, 7, 0, 1 will be accessed. In pass 2, 0, 1 are accessed for (0 – 127), (128 – 255) and again 0, 1 are accessed for (1024 – 1151), (1152 – 1279).

In last pass 0, 1, 0, 1, 2, 3 lines will be accessed.

∴ Total time for reading the blocks of main memory into the cache

$$= (10 + 9 \times 4 + 2) \times 128 \times 10$$

$$= 61440 \text{ n sec.}$$

Choice (D)

19. Let the number of instruction be 100.

Without optimization, time required to execute 100

$$\text{Instructions} = 100 + 10 \times 2 = 100 + 20 = 120$$

With optimization time required

$$= (120 - 0.75 \times 10 - 0.20 \times 10) = 110.5$$

∴ Improvement using optimization

$$= \frac{120}{110.5} = 1.086.$$

Choice (B)

20. Number of lines in cache = 128

As the cache is a 4-way set associative, each set contains 4-blocks.

$$\therefore \text{Number of sets} = \frac{128}{4} = 32$$

So there will be 32 misses.

### 3.32 | Computer Organization and Architecture Test 3

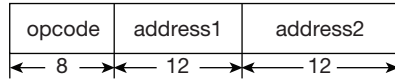
But the program accesses every  $8^{\text{th}}$  word.

$$\therefore \text{Number of misses} = \frac{32}{8} = 4$$

$$\text{Hence miss rate} = \frac{1}{4} \quad \text{Choice (B)}$$

21. Instruction size = 32-bits

Two address instruction format will be



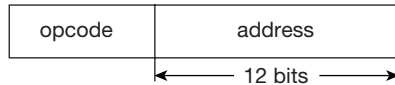
There will be  $2^8$  possible combinations of operations.

Two address instructions = 240

Operations for single address instructions

$$= 256 - 240 = 16$$

Single address instruction format will be



$$\text{Total one address operations} = 16 \times 2^{12} = 65536.$$

Choice (B)

22. The ideal speed up of a pipelined processor is equal to the number of stages in the pipeline.

$\therefore$  As there are 5-stages the speed will be 5.

Choice (B)

23. Ideal speed up = 5

Speed up due to Data hazards

$$\begin{aligned} & \frac{\text{Pipeline Depth}}{1 + (\text{load frequency} \times \text{load penalty}) + (\text{branch frequency} \times \text{branch penalty})} \\ &= \frac{5}{1 + (0.2 \times 0.4 \times 2) + (0.3 \times 0.5 \times 3)} \\ &= \frac{5}{1 + 0.16 + 0.45} = 3.11 \end{aligned}$$

$$\therefore \text{Speed up} = \frac{5 - 3.11}{5} \times 100 = 37.8\% \quad \text{Choice (D)}$$

24. Given  $x = 0100\ 0110\ 1101\ 1000\ 0000\ 0000\ 0000\ 0000$   
 $y = 1011\ 1110\ 1110\ 0000\ 0000\ 0000\ 0000\ 0000$   
 IEEE 754 floating point representation numbers has the following format:

Sign	Biased exponent	Mantissa
1	8	23

For  $x$ , sign bit = 0  $\Rightarrow$  sign = +

Biased exponent = 100 01101 = 141

Exponent = 141 - 127 (Bias) = 14

Mantissa = 1.101 1000 0000 0000 0000 0000

$$\therefore x = +1.101\ 1000\ 0000\ 0000\ 0000\ 0000 \times 2^{14} = +27648$$

For  $y$ , sign bit = 1  $\Rightarrow$  sign = -

Biased exponent = 011 1110 1 = 125

$$\text{Exponent} = 125 - 127 = -2$$

$$\text{Mantissa} = 1.110\ 0000\ 0000\ 0000\ 0000\ 0000$$

$$\therefore y = -1.110\ 0000\ 0000\ 0000\ 0000\ 0000 \times 2^{-2} = -0.4375$$

$$x + y = 27648 - 0.4375 = 27647.5625$$

$$x * y = 27648 * 0.4375 = -12096 \quad \text{Choice (A)}$$

25. Given code:

$I_1$ : ADD  $R_1, R_2, R_3$

$I_2$ : SUB  $R_4, R_1, R_5$

$I_3$ : LOAD  $R_6, 200(R_1)$

$I_4$ : ADD  $R_7, R_1, R_6$

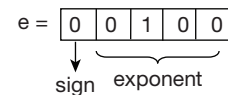
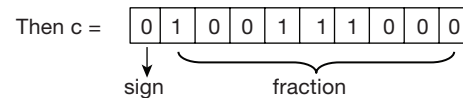
$I_2, I_3, I_4$  are dependent on  $I_1$ .  $I_4$  dependent on  $I_3$ .

The execution chart is shown below:

	1	2	3	4	5	6	7	8	9	10
$I_1$	IF	ID	EX	MEM	WB					
$I_2$		IF	ID	EX	MEM	WB				
$I_3$			IF	ID	EX	MEM	WB			
$I_4$				IF	Stall	ID	EX	MEM	WB	

$\therefore R_1$  can be forwarded to  $I_2, I_3$  and  $I_4$ , but  $R_6$  (in  $I_3$ ) cannot be forwarded to  $I_4$  immediately, so one stall occurs. Choice (B)

26. Given number +1001.110



The decimal point will be at 4th position from left.

Choice (A)

27. Input clock frequency = 8 MHz

$$\text{clock cycle} = \frac{1}{8 \text{ MHz}} = 125 \text{ ns}$$

Given that bus cycle = 4  $\times$  clock cycle

$$= 4 \times 125 = 500 \text{ ns}$$

Data bus width = 16-bits = 2 B

$\therefore$  2 B can be transferred for every 500 ns.

$$\therefore \text{Transfer rate} = \frac{2 \text{ B}}{500 \text{ ns}} = 4 \text{ MB/sec} \quad \text{Choice (B)}$$

28. As the number is an indirect address operand, the effective address will present in the given address location. So we refer two times to get the actual operand from memory. Hence the correct sequence of micro-operation is Choice (D)

29. As there are 7 micro-operations and each micro-operation takes one clock cycle, the total number of clock cycles for addition with an indirect address operand = 7. Choice (D)

30. Access time of cache = 100 ns

$$\text{Access time of main memory} = 1 \mu\text{s} = 10^3 \text{ ns}$$

Read requests = 80%

Write requests = 20%

Hit ratio for read only access = 0.9

Write-through means main memory is updated while updating cache memory.

Average access time of the system

$$= 0.8(0.9 \times 100 + 0.1(100 + 1000)) + 0.2 \times 1000$$

$$= 160 + 200 = 360 \text{ ns} \quad \text{Choice (C)}$$

31. The instruction “bbs reg, pos, label” jumps to label if bit in position ‘pos’ of register operand ‘reg’ is one.

To implement this instruction as

result  $\leftarrow$  reg & mask

We are performing ‘and’ operation between ‘reg’ and ‘mask’.

The mask must be ‘1’ to check a position value of ‘reg’. And it is left shifted POS number of times to align that 1 to the required position of reg.

For example,

$$\text{Reg} = A091 = 1010 \ 0000 \ 1001 \ 0001$$

$$\text{POS} = 2$$

Using bbs, we won’t jump to label as 2<sup>nd</sup> bit is zero using mask  $\leftarrow$  0x1  $\ll$  POS

$$\leftarrow 0x1 \ll 2$$

$$\leftarrow 0x0100$$

Now we perform AND between reg and mask. As the result is zero we won’t jump to label. Choice (D)

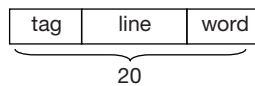
32. Main memory = 1 MB = 2<sup>20</sup> B

Word size = 1 B

$$\text{Block size} = 16 \text{ B} = 2^4 \text{ B}$$

$$\text{Cache size} = 64 \text{ KB} = 2^{16} \text{ B}$$

For Direct mapped cache:



word size = 4

$$\text{Number of blocks in cache} = \frac{2^{16}}{2^4} = 2^{12}$$

$$\therefore \text{Line} = 12$$

$$\text{tag} + \text{line} = 20 - 4 = 16$$

$$\text{Tag} = 16 - 12 = 4$$

Given address F0010:

$$F0010 = \frac{1111}{\text{tag}} \frac{000000000001}{\text{line}} \frac{000}{\text{word}}$$

$$\therefore \text{Line address} = 0000 \ 0000 \ 0001 \quad \text{Choice (C)}$$

33. The time required to transfer one byte is:

$$= 250 + 500 + 250$$

$$= 1000 \text{ ns} = 1 \mu\text{s}$$

To transfer 128 bytes, we require 128  $\mu\text{s}$ .

Choice (D)

34. Instructions size = 2 B

$$\text{Current instructions address} = 356029$$

PC always points to the address of the next instruction. i.e.,  $356029 + 2 = 356031$

In PC-relative addressing mode, the content of PC is added to the displacement, which is given as -31.

So the branch target address

$$= 356031 - 31 = 356000$$

Choice (D)

35. Data transferred = 10 kB/sec

$$= 10000 \text{ Bytes/sec}$$

Given that interrupts are generated for every 1 Byte.

There will be 10000 interrupts and rate of interrupts

$$= \frac{1}{10000} = 100 \mu\text{s}$$

$\therefore$  Fraction of processor time consumed by this I/O

$$= \frac{100}{100} = 1$$

Choice (A)