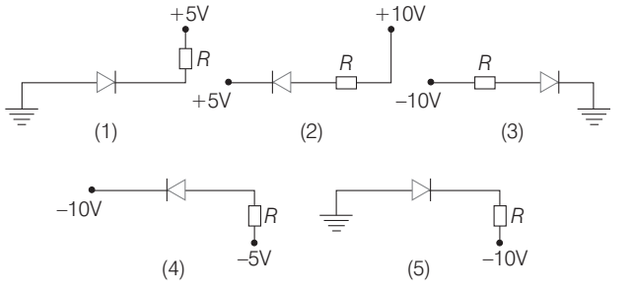
DAY THIRTY SEVEN

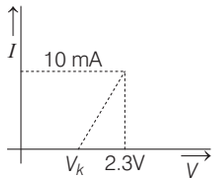
Unit Test 8
(Electronic Devices)

1 In the figure shown below, which of the diodes are forward biased?



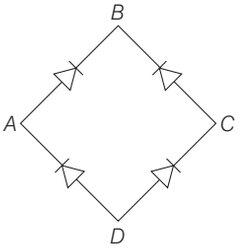
(a) 1, 2, 3 (b) 2, 4, 5 (c) 1, 3, 4 (d) 2, 3, 4

2 The resistance of a germanium junction diode whose *V*-*I* graph is shown in the figure, is ($V_k = 0.3$ V).



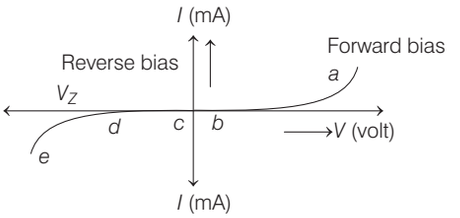
(a) 5 kΩ (b) 0.2 kΩ (c) 2.3 kΩ (d) $\left(\frac{10}{2.3}\right)$ kΩ

3 In the figure, the input is across the terminals *A* and *C* and the output is across *B* and *D*. Then, the output is



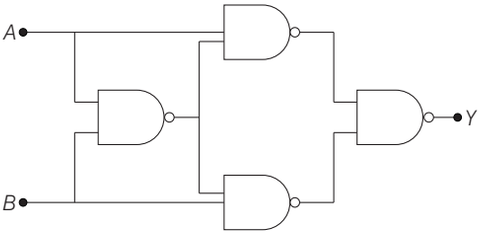
(a) zero (b) same as the input
(c) full wave rectified (d) half wave rectified

4 The graph given below represents the *I*-*V* characteristics of a zener diode. Which part of the characteristics curve is most relevant for its operation as a voltage regulator?



(a) *ab* (b) *bc*
(c) *cd* (d) *de*

5 Truth table for system of four NAND gates as shown in figure is



(a)

A	*B*	*Y*
0	0	0
0	1	1
1	0	1
1	1	0

(b)

A	*B*	*Y*
0	0	0
0	1	0
1	0	1
1	1	1

(c)

A	*B*	*Y*
0	0	1
0	1	1
1	0	0
1	1	0

(d)

A	*B*	*Y*
0	0	1
0	1	0
1	0	0
1	1	1

6 In common-emitter amplifier, the current gain is 62. The collector resistance and input resistance are 5 k Ω and 500 Ω, respectively. If the input voltage is 0.01 V, the output voltage is

(a) 0.62 V (b) 6.2 V
(c) 62 V (d) 620 V

7 The reverse saturation of *p-n* diode

(a) depends on doping concentrations
(b) depends on diffusion length of carriers
(c) depends on the doping concentrations and diffusion length
(d) depends on the doping concentrations, diffusion length and device temperature

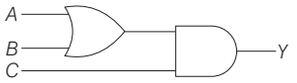
8 A *p-n-p* transistor is said to be in active region of operation, when

(a) both emitter junction and collector junction are forward biased
(b) both emitter junction and collector junction are reverse biased
(c) emitter junction is forward biased and collector junction is reverse biased
(d) emitter junction is reverse biased and collector junction is forward biased

9 A *n-p-n* transistor conducts, when

(a) collector is positive and emitter is at same potential as the base
(b) both collector and emitter are negative with respect to the base
(c) both collector and emitter are positive with respect to the base
(d) collector is positive and emitter is negative with respect to the base

10 To get an output $Y = 1$ from the circuit shown, the inputs A, B and C must be respectively



(a) 0, 1, 0 (b) 1, 0, 0
(c) 1, 0, 1 (d) 1, 1, 0

11 An AND gate is followed by a NOT gate in series. With two inputs A and B, the Boolean expression for the output Y will be

(a) $\overline{A + B}$ (b) $\overline{A \cdot B}$
(c) $A \cdot B$ (d) $A + B$

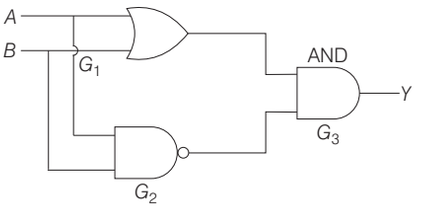
12 In the *CB* mode of a transistor, when the collector voltage is changed by 0.5 V. The collector current changes by 0.05 mA. The output resistance will be

(a) 10 kΩ (b) 20 kΩ
(c) 5 kΩ (d) 2.5 kΩ

13 The current gain of a transistor in common emitter mode is 49. The change in collector current and emitter current corresponding to the change in base current by 5.0 μA, will be

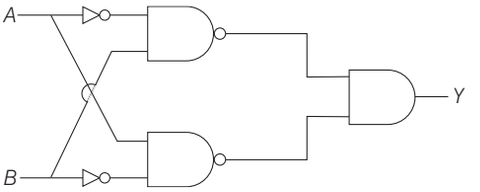
(a) 245 μA, 250 μA (b) 240 μA, 235 μA
(c) 260 μA, 255 μA (d) None of the above

14 The following configuration of gates is equivalent to



(a) NAND (b) XOR
(c) OR (d) None of these

15 The following circuit represents



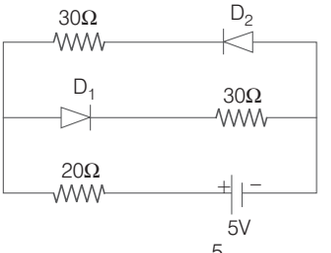
(a) XNOR gate (b) XOR gate
(c) AND gate (d) NAND gate

16 The truth table is given below

Inputs		Output
A	*B*	*Y*
0	0	0
1	0	0
0	1	0
1	1	1

represents
(a) AND gate
(b) NOR gate
(c) OR gate
(d) NAND gate

17 If internal resistance of cell is negligible, then current flowing through the circuit is

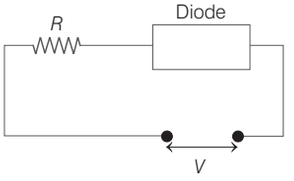


(a) $\frac{3}{50}$A (b) $\frac{5}{50}$A
(c) $\frac{4}{50}$A (d) $\frac{2}{50}$A

18 For a transistor $\frac{I_c}{I_e} = 0.96$, the current gain in common-emitter configuration is

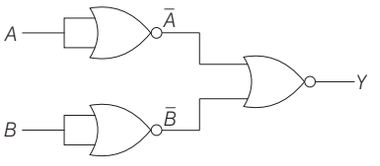
(a) 6 (b) 12 (c) 24 (d) 48

19 For a given circuit of ideal *p-n* junction diode, which of the following is correct ?



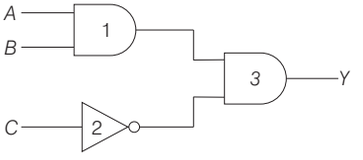
(a) In forward biasing the voltage across R is V
(b) In reverse biasing the voltage across R is V
(c) In forward biasing the voltage across R is $2V$
(d) In reverse biasing the voltage across R is $2V$

20 Identify the operation performed by the circuit given below



(a) NOT (b) AND (c) OR (d) NAND

21 In the following circuit, the output Y becomes zero for the inputs



(a) $A = 1, B = 0, C = 0$ (b) $A = 0, B = 1, C = 1$
(c) $A = 0, B = 0, C = 0$ (d) $A = 1, B = 1, C = 1$

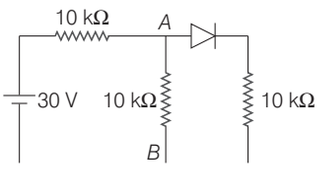
22 The inputs and outputs for different time intervals are given below the NAND gate.

Time	Input *A*	Input *B*	Output *Y*
t_1 to t_2	0	1	P
t_2 to t_3	0	0	Q
t_3 to t_4	1	0	R
t_4 to t_5	1	1	S

The values taken by P, Q, R, S are respectively

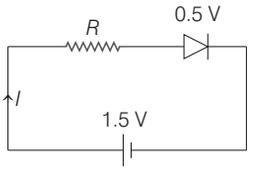
(a) 1, 1, 1, 0 (b) 0, 1, 0, 1
(c) 0, 1, 0, 0 (d) 1, 0, 1, 1
(e) 1, 0, 1, 0

23 In the figure, potential difference between A and B is



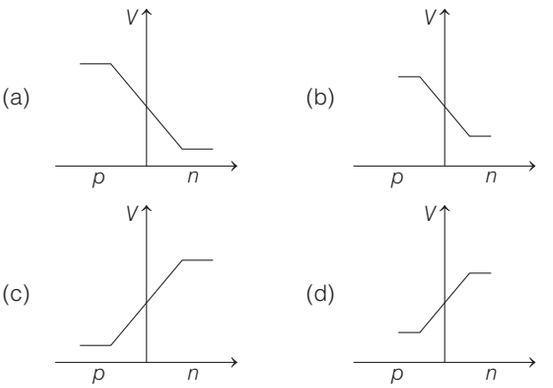
(a) zero (b) 5 V (c) 10 V (d) 15 V

24 The diode used in the circuit shown in the figure, has a constant voltage drop of 0.5 V at all currents and a maximum power rating of 100 mW. What should be the value of the resistor R, connected in series with the diode for obtaining maximum current?

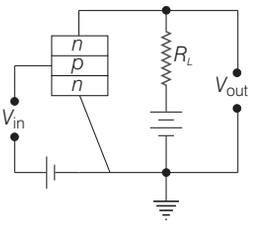


(a) 1.5 Ω (b) 5 Ω
(c) 6.67 Ω (d) 200 Ω

25 In a forward biased *p-n* junction diode, the potential barrier in the depletion region is of the form

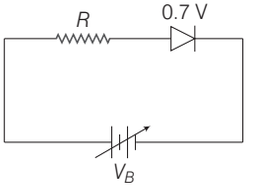


26 An *n-p-n* transistor circuit is arranged as shown in figure. It is



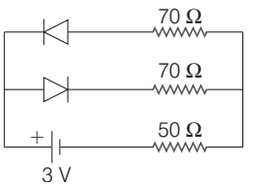
(a) a common base amplifier circuit
(b) a common emitter amplifier circuit
(c) a common collector amplifier circuit
(d) None of the above

27 The junction diode in the following circuit requires a minimum current of 1 mA to be above the knee point (0.7 V) of its *I-V* characteristic curve. The voltage across the junction diode is independent of current above the knee point, if $V_B = 4$ V, then the maximum value of R, so that the voltage is above knee point will be



(a) 3.3 kΩ (b) 4.0 kΩ (c) 4.7 kΩ (d) 6.6 kΩ

28 The circuit shown in the figure contains two diodes, each with a forward resistance of 30 Ω and with infinite backward resistance. If the battery is 3 V, the current (in ampere) through the 50 Ω resistance is



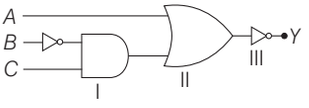
(a) zero (b) 0.01 (c) 0.02 (d) 0.03

29 Which of the following is not equal to 1 in Boolean algebra?

(a) $\overline{A \cdot \overline{A}}$ (b) $A \cdot \overline{A}$

(c) $A + \overline{A}$ (d) $A + 1$

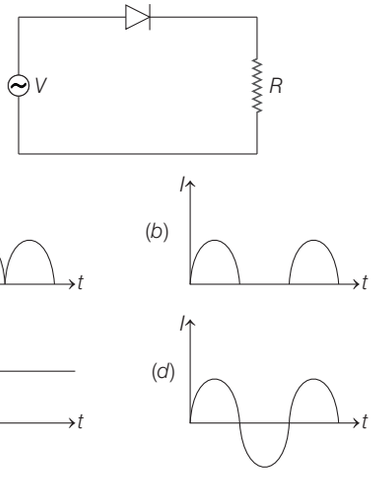
30 The output Y of the logic circuit shown in figure, is best represented as



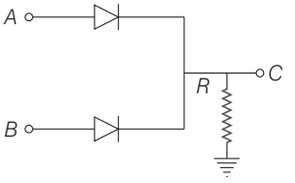
(a) $\overline{A} + \overline{B \cdot C}$ (b) $\overline{A + \overline{B} \cdot C}$

(c) $\overline{A + B \cdot C}$ (d) $\overline{A + \overline{B} \cdot C}$

31 A p-n junction diode shown in the figure can act as a rectifier. An alternating current source (V) is connected in the circuit. The current (I) in the resistor (R) can be shown by



32 In the circuit as shown in figure, A and B represent two inputs and C represents the



(a) OR gate (b) NOR gate

(c) AND gate (d) NAND gate

33 The ratio of electron and hole current in a semiconductor is 7/4 and the ratio of drift velocities of electrons and holes is 5/4, then ratio of concentrations of electrons and holes will be

(a) 5/7 (b) 7/5 (c) 25/49 (d) 49/25

34 In a junction diode, the direction of diffusion current is

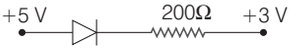
(a) from n-region to p-region

(b) from p-region to n-region

(c) from n-region to p-region, if the junction is forward biased and *vice versa*, if it is reverse biased

(d) from p-region to n-region if the junction is forward biased and *vice versa*, if it is reverse biased

35 The direction of flow of current in the given diagram is



(a) zero (b) 10^{-2} A (c) 10 A (d) 0.025 A

Direction (Q. Nos. 36-41) *In each of the following questions a statement of Assertion is given followed by a corresponding statement of Reason just below it. Of the statements mark the correct answer as*

(a) If both Assertion and Reason are true and the Reason is the correct explanation of the Assertion

(b) If both Assertion and Reason are true but the Reason is not correct explanation of the Assertion

(c) If Assertion is true but Reason is false

(d) If both Assertion and Reason are false

36 **Assertion** (A) In a common emitter transistor amplifier, the input current is much less than the output current.
Reason (R) The common emitter transistor amplifier has very high input impedance.

37 **Assertion** (A) The logic gate NOT can be built using diode.
Reason (R) The output voltage and the input voltage of the diode have 180° phase difference.

38 **Assertion** (A) A transistor amplifier in common emitter configuration, has a low input impedance.
Reason (R) The base to emitter region is forward biased.

39 **Assertion** (A) NAND or NOR gates are called digital building blocks.

Reason (R) The repeated use of NAND or NOR gate can produce all the basic or completed gates.

40 **Assertion** (A) The resistivity of a semiconductor increases with temperature.
Reason (R) The atoms of a semiconductor vibrate with larger amplitudes at higher temperatures thereby increasing its resistivity.

ANSWERS

1. (b)	**2.** (b)	**3.** (c)	**4.** (d)	**5.** (a)	**6.** (b)	**7.** (d)	**8.** (c)	**9.** (d)	**10.** (c)
11. (b)	**12.** (a)	**13.** (a)	**14.** (b)	**15.** (a)	**16.** (a)	**17.** (b)	**18.** (c)	**19.** (a)	**20.** (b)
21. (d)	**22.** (a)	**23.** (c)	**24.** (b)	**25.** (d)	**26.** (b)	**27.** (a)	**28.** (c)	**29.** (b)	**30.** (d)
31. (b)	**32.** (a)	**33.** (b)	**34.** (b)	**35.** (b)	**36.** (c)	**37.** (d)	**38.** (a)	**39.** (a)	**40.** (d)

Hints and Explanations

1 A *p*-*n* junction diode is said to be forward biased, if the positive terminal of the external battery is connected to *p*-side and the negative terminal to the *n*-side of the junction.
Thus, 2, 4 and 5 are forward biased.

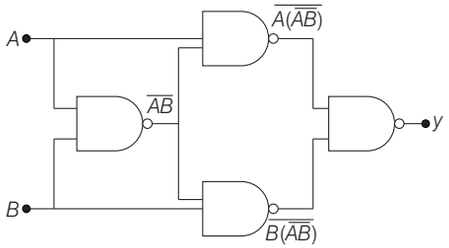
2 $R = \dfrac{\Delta V}{\Delta I} = \dfrac{2.3 - 0.3}{10 \times 10^{-3}} = \dfrac{2}{10} \times 10^3$
$= 0.2 \times 10^3\ \Omega = 0.2\ \text{k}\Omega$

3 The given figure represents a full wave rectifier, which is also known as bridge rectifier, which uses four diodes.

4 When reverse bias is increased, then the electric field across the junction also increases. At some stages, the electric field becomes so high that it breaks the covalent bonds, creating electron-hole pairs. This mechanism is known as Zener breakdown.

In breakdown region for a long range of load (R_L), the voltage remains the same though the current may be large. So, option (d) is correct.

5 Output, $Y = \overline{(A \cdot \overline{(A \cdot B)})} \cdot \overline{(B \cdot \overline{(A \cdot B)})}$



$= \overline{(\overline{A} + A \cdot B) \cdot (\overline{B} + A \cdot B)}$
$= (\overline{\overline{A} + A \cdot B}) + (\overline{\overline{B} + A \cdot B})$
$= A \cdot (\overline{A \cdot B}) + B \cdot (\overline{A \cdot B})$
$= A \cdot (\overline{A} + \overline{B}) + B \cdot (\overline{A} + \overline{B})$
$= A \cdot \overline{B} + B \cdot \overline{A}$

A	B	$\overline{A}$	$\overline{B}$	$A \cdot \overline{B}$	$B \cdot \overline{A}$	Y
0	0	1	1	0	0	0
0	1	1	0	0	1	1
1	0	0	1	1	0	1
1	1	0	0	0	0	0

It is the truth table for XOR gate.

6 Voltage gain = resistance gain × current gain
or $\dfrac{V_{\text{out}}}{V_{\text{in}}} = \dfrac{R_{\text{out}}}{R_{\text{in}}} \times \beta$
$\Rightarrow\ V_{\text{out}} = \dfrac{R_{\text{out}}}{R_{\text{in}}} \times \beta \times V_{\text{in}}$
$\therefore\ V_{\text{out}} = \dfrac{5000}{500} \times 62 \times 0.01 = 6.2\ \text{V}$

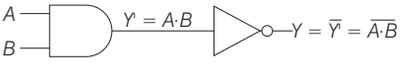
7. The reverse saturation of *p*-*n* diode depends on the doping concentrations, diffusion length and device temperature.

8 For amplification of a *p*-*n*-*p* transistor, emitter junction is forward biased and collector junction is reverse biased. In this state, *p*-*n*-*p* transistor is said to be in active region of operation.

9 In an *n*-*p*-*n* transistor, the emitter-base junction is forward biased. However, collector-base junction is reverse biased.

10 For the given combination,
$Y = (A + B) \cdot C$
If $Y = 1$, $A = 1$, $B = 0$, $C = 1$

11 The inputs for AND gate give output
$Y' = A \cdot B$

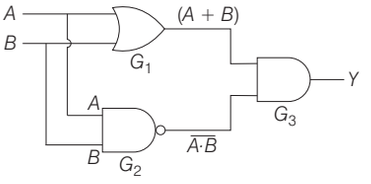


Y' is the input for NOT gate
$\therefore\ Y = \overline{Y'}$
$\Rightarrow\ Y = \overline{A \cdot B}$

12 Here, $\Delta V_C = 0.5\ \text{V}$
$\Delta I_C = 0.05\ \text{mA} = 0.05 \times 10^{-3}\ \text{A}$
Output resistance is given by
$R_{\text{out}} = \dfrac{\Delta V_C}{\Delta I_C}$
$= \dfrac{0.5}{0.05 \times 10^{-3}} = 10^4\ \Omega = 10\ \text{k}\Omega$

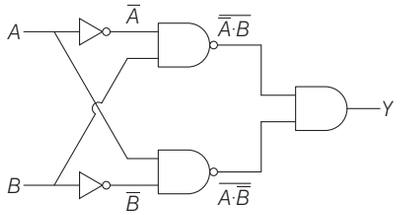
13 Current gain, $\beta = \dfrac{\Delta I_C}{\Delta I_B}$, where ΔI_C is change in collector current and ΔI_B is change in base current.
$\therefore \Delta I_C = \beta \Delta I_B = 49 \times 5 = 245\ \mu\text{A}$
Also, $\Delta I_E = \Delta I_B + \Delta I_C$
$= (245 + 5)\mu\text{A}$
$= 250\ \mu\text{A}$

14 The given output equation can be written as



$Y = (A + B) \cdot \overline{AB}$
$Y = (A + B) \cdot (\overline{A} + \overline{B})$ [$\because$ Using de Morgan's theorem]
$= A\overline{A} + A\overline{B} + B\overline{A} + B\overline{B}$
$= 0 + A\overline{B} + \overline{A}B + 0$
$= \overline{A}B + A\overline{B}$
This boolean expression for XOR gate.

15 The given output equation can be written as



$Y = \overline{A \cdot \overline{B}} \cdot \overline{\overline{A} \cdot B}$

$= (\overline{A} + B) \cdot (A + \overline{B})$

(Using de Morgan's theorem)

$= \overline{A}\, A + B\,\overline{B} + BA + \overline{A}\,\overline{B}$

$= AB + \overline{A}\,\overline{B}$

This Boolean expression for XNOR gate.

16 We can see from the truth table that output is 1, only when its both inputs are 1. This is possible only for AND gate. The Boolean expression for AND gate is $Y = A \cdot B$, which satisfies the truth table as given below.

$0 \cdot 0 = 0$

$1 \cdot 0 = 0$

$0 \cdot 1 = 0$

$1 \cdot 1 = 1$

Here, symbol $(\cdot)$ represents AND operation.

17 In the circuit, diode D_1 is forward biased and diode D_2 is reverse biased. Therefore, no current flows in the arm containing D_2 and all of the current flows through arm containing D_1.

Thus, current flowing through the circuit $= \dfrac{5}{20 + 30} = \dfrac{5}{50}$ A

18 Given, $\dfrac{I_c}{I_e}$ = Current gain $(\alpha) = 0.96$

So, current gain in common emitter configuration is

$$\beta = \frac{\alpha}{1 - \alpha}$$

$$= \frac{0.96}{1 - 0.96} = \frac{0.96}{0.04} = 24$$

19 In forward biasing, the diode conducts. For ideal junction diode, the forward resistance is zero. Therefore, entire applied voltage occurs across resistance R, i.e. there occurs no voltage drop. Thus, voltage across R is V in forward biasing.

While in reverse biasing, the diode does not conduct, so it has infinite resistance. Thus, voltage across R is zero in reverse biasing.

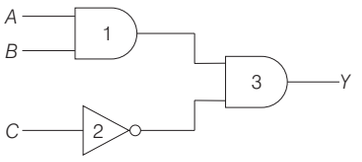
20 The output of the circuit is

$$Y = \overline{\overline{A} + \overline{B}} = \overline{\overline{A}} \cdot \overline{\overline{B}}$$

$= A \cdot B$ [$\because \overline{\overline{A}} = A$ and $\overline{\overline{B}} = B$]

which is the output of an AND gate.

21 Output of gate-1, $Y_1 = A \cdot B$

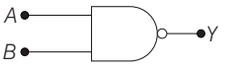


Output of gate 2, $Y_2 = \overline{C}$

Output of gate 3, $Y = Y_1 \cdot Y_2 = (A \cdot B) \cdot \overline{C}$

Thus, from the given options output will be zero, if $A = 1$, $B = 1$ and $C = 1$

22 NAND gate is obtained when the output of AND gate is made as the input of NOT gate. Boolean expression for NAND gate is



$Y = \overline{A \cdot B}$

Input (A)	Input (B)	Output (Y)
0	0	1
1	0	1
0	1	1
1	1	0

23 Here, p-n junction is forward biased. If p-n junction is ideal, its resistance is zero. The effective resistance across A and B

$$= \frac{10 \times 10}{10 + 10} = 5\ \text{k}\Omega$$

Current in the circuit,

$$I = \frac{V}{R} = \frac{30}{15 \times 10^3} = \frac{2}{10^3}\ \text{A}$$

Current in arm, $AB = I = \dfrac{2}{10^3}$

Potential difference across A and B

$$= \frac{2}{10^3} \times 5 \times 10^3 = 10\ \text{V}$$

24 Current through circuit,

$$I = \frac{P}{V} = \frac{100 \times 10^{-3}}{0.5} = 0.2\ \text{V}$$

Voltage drop across,

$R = 1.5 - 0.5 = 1.0$ V

Hence, $R = \dfrac{1}{0.2} = 5\ \Omega$

25 In forward biased p-n junction, the applied potential is opposite to the junction barrier potential V_B. The consequence of this is the effective barrier potential reduces. Hence, the graph (d) is correctly shown.

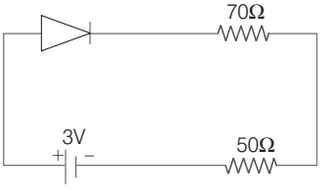
26 Here, emitter is forward biased, and is common between input and output circuit. Thus, the circuit is of n-p-n transistor with a common emitter amplifier mode.

27 As, $V_B = V_{\text{knee}} + IR$

or $4 = 0.7 + 10^{-3} R$

or $R = \dfrac{3.3}{10^{-3}} = 3.3\text{k}\Omega$

28 In the circuit, the upper diode D_1 is reverse biased and the lower diode D_2 is forward biased. Thus, there will be no current across upper diode junction. The effective circuit will be as shown in figure.



Total resistance of circuit,

$R = 50 + 70 + 30 = 150\ \Omega$

Current in circuit,

$$I = \frac{V}{R} = \frac{3}{150} = 0.02\ \text{A}$$

29 (a) $\overline{A \cdot \overline{A}} = \overline{A} + \overline{\overline{A}} = \overline{A} + A = 1$

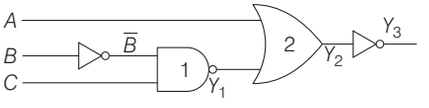
(b) $A \cdot \overline{A} = 0$

(c) $A + \overline{A} = 1$

(d) $A + 1 = 1$

Hence, all the options give the output 1 except option (b).

30



The output at gate 1, $Y_1 = \overline{B} \cdot C$

Output at gate 2, $Y_2 = A + \overline{B} \cdot C$

Final output, $Y_3 = \overline{Y}_2 = \overline{A + \overline{B} \cdot C}$

31 The given circuit represents a circuit of half wave rectifier. In this, during the positive half cycle of input, p-n junction is forward biased. Hence, current flows in the load. But in the negative half cycle of input, p-n junction is reverse biased. Thus, no current flows. So, option (b) is correct.

32 The circuit represents OR gate, as the output at C is 1, when either A or B or both A and B have input at level 1. But output at C is zero, when both A and B are at zero level, since for OR gate, the Boolean expression is $C = (A + B)$.

33 As, $I = Anev_d$ or $I \propto nv_d$

$$\therefore \quad \frac{I_e}{I_h} = \frac{n_e v_e}{n_h v_h}$$

$$\text{or} \quad \frac{n_e}{n_h} = \frac{I_e}{I_h} \times \frac{v_h}{v_e} = \frac{7}{4} \times \frac{4}{5} = \frac{7}{5}$$

34 In a p-n junction, the direction of diffusion current is from p-region to n-region only.

35 Here, p-n junction as forward biased with voltage = 5 – 3 = 2 V

$$\therefore \text{ Current } I = \frac{2}{200}$$

$$= \frac{1}{100} = 10^{-2} \text{ A}$$

36 The common emitter transistor amplifier has input resistance equal to 1 k Ω (approx.), and output resistance equal to 10 kΩ (approx.). The output current in CE amplifier is much larger than the input current. Hence, option (c) is correct.

37 NOT gate inverts the signal applied to it. But in diode, the input and output are in same phase. Thus, NOT gate cannot be built by a diode. Hence, option (d) is correct.

38 As base to emitter region is forward biased. Hence, it will work as simple forward biased diode and resistance is low.

39 NAND or NOR gates are called universal (digital) building blocks because using repeated order of these two types of gates we can produce all the basic gates namely OR, AND or complex gates.

40 Resistivity of a semiconductor decreases with the temperature. The atoms of a semiconductor vibrate with larger amplitudes at higher temperature, thereby increasing its conductivity, not resistivity.