Chapter 3

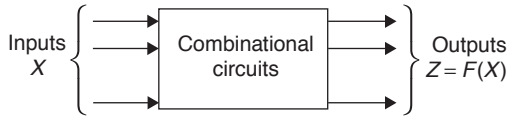
Combinational Circuits

LEARNING OBJECTIVES

- *Combinational logic design*
- *Arithmetic circuit*
- *Half adder*
- *Full adder*
- *Half subtractor*
- *Full subtractor*
- *n-bit comparator*
- *Parity bit generator and parity bit checker*
- *Code converter*
- *Decoder*
- *Designing high order decoders from lower order decoder*
- *Combinational logic implementation*
- *Encoders*
- *Multiplexer*
- *Demultiplexer*

Introduction

Combinational logic is a type of logic circuit whose output is a function of the present input only.



Combinational Logic Design

The design of combinational circuit starts from the problem, statement and ends with a gate level circuit diagram.

The design procedure involves the following steps:

1. Determining the number of input variables and output variables required, from the specifications.
2. Assigning the letter symbols for input and output.
3. Deriving the truth table that defines the required relationship between input and output.
4. Obtaining the simplified Boolean function for each output by using K-map or algebraic relations.
5. Drawing the logic diagram for simplified expressions.

We will discuss combinational circuits under the following categories:

- Arithmetic circuits
- Code converters
- Data processing circuits

Arithmetic Circuits

Arithmetic circuits are the circuits that perform arithmetic operation. The most basic arithmetic operation is addition.

Half Adder

Addition is an arithmetic operation, and here to implement addition in digital circuits we have to implement by logical gates. So the addition of binary numbers will be represented by the logical expressions. Half adder is an arithmetic circuit which performs the addition of two binary bits, and the result is viewed in two output—sum and carry.

The sum 'S' is the X-OR of 'A' and 'B' where A and B are inputs.

$$\therefore \quad S = A\overline{B} + B\overline{A} = A \oplus B$$

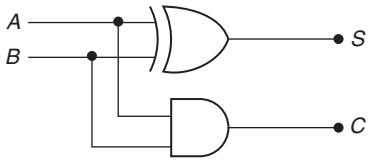
The carry 'C' is the AND of A and B.

$$\therefore C = AB$$

Table 1 *Truth Table*

Inputs		Outputs	
A	***B***	***S***	***C***
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

So, half adder can be realized by using one X-OR gate and one AND gate.

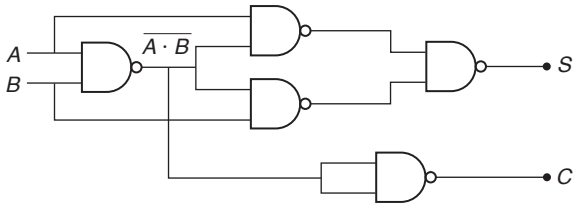


Half adder can also be realized by universal logic such as only NAND gate or only NOR gate as given below.

NAND logic

$$S = A\bar{B} + \bar{A}B$$
$$= A\bar{B} + A\bar{A} + \bar{A}B + B\bar{B}$$
$$= A(\bar{A} + \bar{B}) + B(\bar{A} + \bar{B})$$
$$= \overline{\overline{A\bar{A}B} \cdot \overline{B\bar{A}B}}$$

$$C = AB = \overline{\overline{A \cdot B}}$$

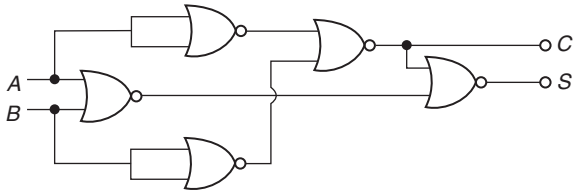


Half adder using NAND logic

NOR logic

$$S = A \cdot \bar{B} + \bar{A}B$$
$$= A\bar{B} + A\bar{A} + \bar{A}B + B\bar{B}$$
$$= A(\bar{A} + \bar{B}) + B(\bar{A} + \bar{B})$$
$$= (A + B)(\bar{A} + \bar{B})$$
$$= \overline{\overline{A + B} + \overline{(\bar{A} + \bar{B})}}$$

$$C = A \cdot B = \overline{\overline{A \cdot B}} = \overline{\bar{A} + \bar{B}}$$



Half adder using NOR logic

Full Adder

Full adder is an arithmetic circuit that performs addition of two bits with carry input. The result of full adder is given by two outputs—sum and carry. The full adder circuit is used in parallel adder circuit as well as in serial adder circuit.

For full adder, if total number of 1's is odd at input lines, the sum output is equal to logic 1, and if total number of 1's at input lines are more than or equal to 2, then the carry output is logic 1.

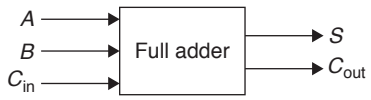


Figure 1 Block diagram

Table 2 *Truth Table*

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$S = \bar{A}\bar{B}C_{in} + \bar{A}B\overline{C_{in}} + A\bar{B}\,\overline{C_{in}} + ABC_{in}$$
$$= A \oplus B \oplus C_{in}$$

$$C_{out} = \bar{A}BC_{in} + A\bar{B}C_{in} + AB\overline{C_{in}} + ABC_{in}$$
$$= AB + (A \oplus B)\,C_{in}$$
$$= AB + A\,C_{in} + B\,C_{in}$$

Full adder can also be realized using universal logic gates, i.e., either only NAND gates or only NOR gates as explained below.

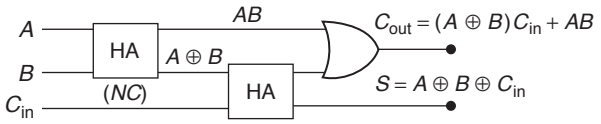


Figure 2 Block diagram of full adder by using Half adder

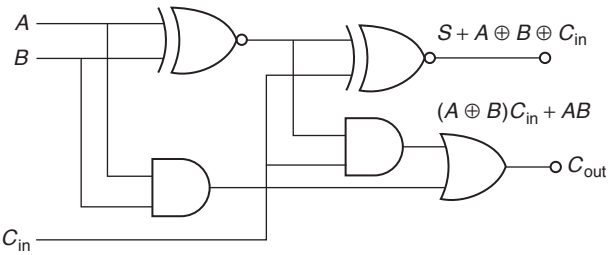


Figure 3 Logic diagram of full adder

NAND logic

$$A \oplus B = \overline{\overline{A\overline{AB}}\;\;\overline{B\overline{AB}}}$$

So $A \oplus B \oplus C_{in}$

Let $A \oplus B = x$ then $s = \overline{\overline{X \cdot \overline{XC_{in}}}\;\;\overline{C_{in}\overline{X \cdot C_{in}}}}$

$$= X \oplus C_{in}$$

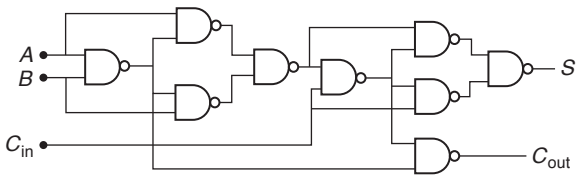


Figure 4 Logic diagram of a full adder using only 2-input NAND gates

NOR logic

Full adder outputs

Sum = $a \oplus b \oplus c$, carry = $ab + bc + ac$ are self dual functions

[$\because$ A function is called as self dual if its dual is same as the function itself $f^D = f$]

For self dual functions, the number of NAND gates are same as number of NOR gates.

By taking the dual for above NAND gate implementation, all gates will become NOR gates, and the output is dual of the sum and carry, but they are self dual ($f^D = f$).

So, output remain same, and only 9 NOR gates are required for full adder, structure similar to NAND gate circuit.

Half Subtractor

Half subtractor is an arithmetic circuit which performs subtraction of one bit (subtrahend) from other bit (minuend), and the result gives difference and borrow each of one bit. The borrow output is logic 1 only if there is any subtraction of 1 from 0.

When a bit 'B' is subtracted from another bit 'A', a difference bit (d) and a borrow bit (b) result according to the rule given below.

Table 3 *Truth Table*

A	B	d	b
0	0	0	0
1	0	1	0
1	1	0	0
0	1	1	1

$$d = A\bar{B} + B\bar{A}$$
$$= A \oplus B$$
$$b = \bar{A}B$$

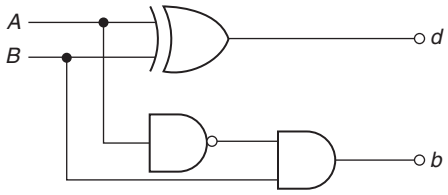


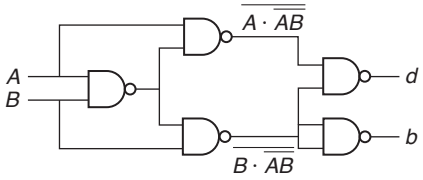
Figure 5 Logic diagram of a half subtractor

A half subtractor can also realized using universal logic either using only NAND gates or only NOR gates as explained below.

NAND logic

$$d = A \oplus B$$
$$= \overline{A\overline{AB}} \cdot \overline{B\overline{AB}}$$

$$b = \bar{A}B = B(\bar{A} + \bar{B}) = B(\overline{AB}) = \overline{B \cdot \overline{AB}}$$



NOR logic

$$d = A \oplus B$$
$$= A\bar{B} + \bar{A}B$$
$$= A\bar{B} + B\bar{B} + \bar{A}B + A\bar{A}$$
$$= \bar{B}(A + B) + \bar{A}(A + B)$$
$$= \overline{B + \overline{A + B}} + \overline{A + \overline{A + B}}$$
$$b = \bar{A}B$$
$$= \bar{A}(A + B)$$
$$= \overline{\overline{\bar{A}(A + B)}}$$
$$= \overline{A + \overline{(A + B)}}$$

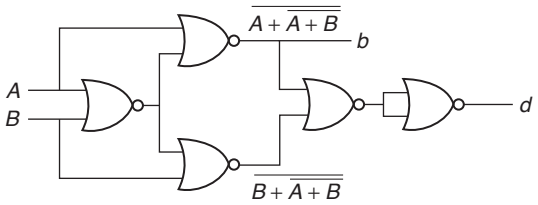


Figure 6 Logic diagram of half subtractor using NOR gate

Full Subtractor

Full subtractor is an arithmetic circuit similar to half subtractor but it performs subtraction with borrow, it involves subtraction of three bits—minuend, subtrahend and borrow-in, and two outputs—difference and borrow. The subtraction of 1 from 0 results in borrow to become logic 1. The presence of odd number of 1's at input lines make difference as logic 1.

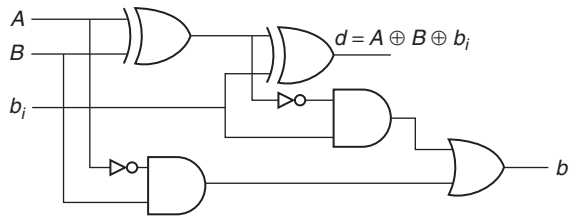
Table 4 *Truth Table*

A	B	b_i	d	b
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$d = \bar{A}\bar{B}b_i + \bar{A}B\bar{b_i} + A\bar{B}\bar{b_i} + ABb_i$$
$$= b_i(AB + \bar{A}\bar{B}) + \bar{b_i}(A\bar{B} + \bar{A}B)$$
$$= b_i(\overline{A \oplus B}) + \bar{b_i}(A \oplus B)$$
$$= A \oplus B \oplus b_i$$

and

$$b = \bar{A}\,\bar{B}b_i + \bar{A}B\bar{b}_i + \bar{A}Bb_i$$
$$= \bar{A}B + (\overline{A \oplus B})b_i$$



NAND logic

$$d = A \oplus B \oplus b_i$$
$$= \overline{\overline{(A \oplus B)(\overline{A \oplus B})b_i}}\ \overline{\overline{b_i(\overline{A \oplus B})b_i}}$$
$$b = \bar{A}B + b_i(\overline{A \oplus B})$$
$$= \overline{\overline{\bar{A}B + b_i(\overline{A \oplus B})}}$$
$$= \overline{\overline{\bar{A}B}\ \overline{b_i\ (A \oplus B)}}$$
$$= \overline{\overline{B(\bar{A} + \bar{B})}\ b_i\left[\overline{b_i} + \overline{(A \oplus B)}\right]}$$

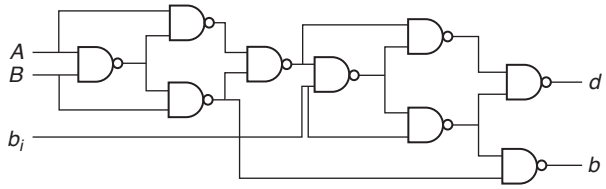


Figure 7 Logic diagram of a full subtractor using NAND logic

NOR logic

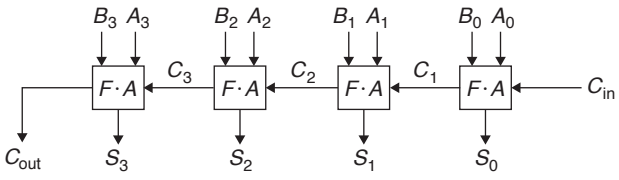
Output of full subtractor is also self dual in nature. So, same circuit, with all NAND gates, replaced by NOR gates gives the NOR gate full subtractor. 9 NOR gates required.

Example 1: How many NAND gates are required for implementation of full adder and full subtractor respectively?
(A) 11, 10 (B) 11, 11 (C) 9, 9 (D) 9, 10

Solution: (C)
From the circuit diagrams in the previous discussion, full adder requires 9 NAND gates and full subtractor requires 9 NAND gates.

Binary Adder

A binary adder is a digital circuit that produces the arithmetic sum of two binary numbers.



Four bit parallel adder the output carry from each full adder is connected to the input carry of next full adder.

The bits are added with full adders, starting from the LSB position to form the sum bit and carry bit.

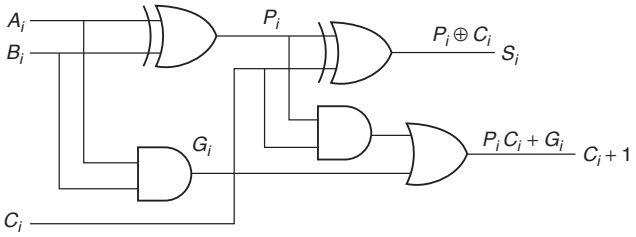
The longest propagation delay time in parallel adder is the time it takes the carry to propagate through the full adders.

For n-bit parallel adders consider t_{pds} is the propagation delay for sum of each full adder and t_{pdc} is the propagation delay of carry.

The total time required to add all n-bits at the nth full adder is

$$T_S = t_{pds} + (n-1)t_{pdc}$$

So propagation delay increases with number of bits. To overcome this difficulty we use look ahead carry adder, which is the fastest carry adder.



Consider the full adder circuit for ith stage, in parallel adder, with two binary variables A_i, B_i, input carry C_i are:

Carry propagate (P_i) and carry generate (G_i)

$$P_i = A_i \oplus B_i$$
$$G_i = A_i \cdot B_i$$

The output sum and carry can be expressed as

$$S_i = P_i \oplus C_i$$
$$C_{i+1} = P_i C_i + G_i$$

Now, the Boolean functions for each stage can be calculated as substitute $i = 0$

C_0 is input carry

$$C_1 = G_0 + P_0\,C_0$$

Substitute $i = 1, 2 \ldots$

$$C_2 = G_1 + P_1C_1 = G_1 + P_1\,(G_0 + P_0C_0)$$
$$= G_1 + P_1\,G_0 + P_1\,P_0\,C_0$$
$$C_3 = G_2 + P_2\,C_2 = G_2 + P_2\,(G_1 + P_1\,G_0 + P_1\,P_0\,C_0)$$
$$= G_2 + P_2\,G_1 + P_2\,\mathrm{P}_1\,G_0 + P_2\,P_1\,P_0\,C_0$$

Since the Boolean function for each output carry is expressed in SOP form, each function can be implemented with AND–OR form or two level NAND gates.

From the above equations we can conclude that this circuit can perform addition in less time as C_3 does not have to wait for C_2 and C_1 to propagate. C_3, C_2, C_1 can have equal time delays.

The gain in speed of operation is achieved at the expense of additional complexity (hardware).

n-bit Comparator

The comparison of two numbers is an operation that determines whether one number is greater than, less than, or equal to the other number.

A magnitude comparator is a combinational circuit that compares two input numbers A and B, and specifies the output with three variables, $A > B$, $A = B$, $A < B$:

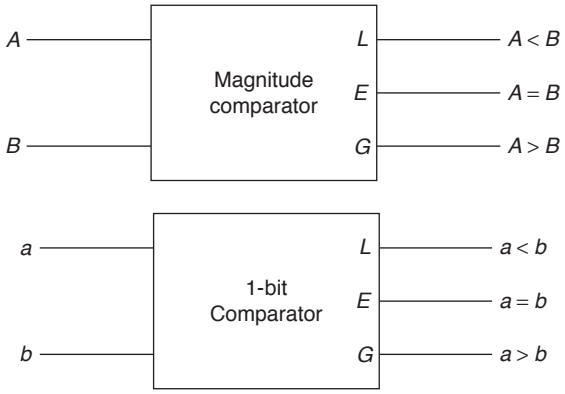


Figure 8 1-bit comparator will have only 1 bit input *a*, *b*.

a	b	a < b	a = b	a > b
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

By considering minterms for each output.

$$(a < b) = a'b$$
$$(a = b) = a'b' + ab = a \odot b$$
$$(a > b) = ab'$$

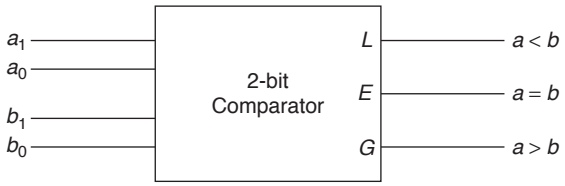
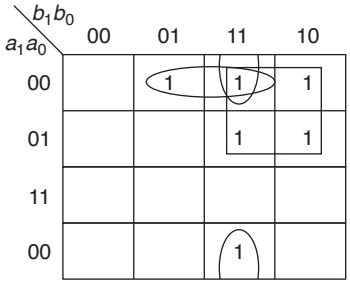


Figure 9 2-bit comparator will have 2-bit inputs a_1 a_0 and b_1 b_0.

a_1	a_0	b_1	b_0	L a < b	E a = b	G a > b
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

$$(a < b) = \Sigma(1, 2, 3, 6, 7, 11)$$
$$(a > b) = \Sigma(4, 8, 9, 12, 13, 14)$$
$$(a = b) = \Sigma(0, 5, 10, 15)$$



$$a < b = a_1'a_0'b_0 + a_0'b_1b_0 + a_1'b_1$$
$$L = \overline{a_1}b_1 + (a_1 \odot b_1)\overline{a_0}b_0$$

Similarly, $a > b = a_0b_1'b_0' + a_1a_0b_0' + a_1b_1'$

$$G = a_1\overline{b_1} + (a_1 \odot b_1)a_0\overline{b_0}$$

$a = b$ is possible when $a_1 = b_1$, $a_0 = b_0$

So $(a = b) = (a_1 \odot b_1)(a_0 \odot b_0)$

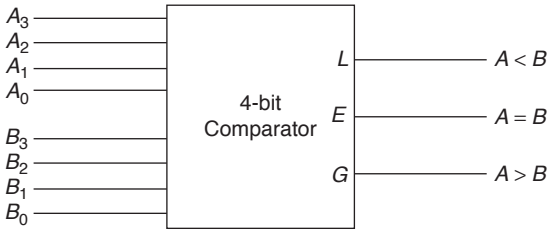


Figure 10 4-bit comparator will compare 2 input numbers each of 4-bits A_3 A_2 A_1 A_0 and B_3 B_2 B_1 B_0 ($A = B$) output will be 1 when each bit of input *A* is equal to corresponding bit in input *B*.

So we can write $(A = B) = (A_3 \odot B_3)\ (A_2 \odot B_2)\ (A_1 \odot B_1)\ (A_0 \odot B_0)$.

To determine whether A is greater or less than B, we inspect the relative magnitudes of pairs of significant bits, starting from MSB. If the two bits of a pair are equal, we compare the next lower significant pair of bits. The comparison continues until a pair of unequal bits is reached.

for $A < B$, $A = 0$, $B = 1$

for $A > B$, $A = 1$, $B = 0$

$$A < B = A_3'B_3 + (A_3 \odot B_3)\ A_2'B_2 + (A_3 \odot B_3)(A_2 \odot B_2) \times A_1'B_1 + (A_3 \odot B_3)(A_2 \odot B_2)\ (A_1 \odot B_1)\ A_0'B_0$$

$$A > B = A_3B_3' + (A_3 \odot B_3)\ A_2B_2' + (A_3 \odot B_3)\ (A_2 \odot B_2) \times A_1B_1' + (A_3 \odot B_3)(A_2 \odot B_2)\ (A_1 \odot B_1)\ A_0B_0'$$

4-bit comparator will have total 8 inputs and $2^8 = 256$ input combinations in truth table.

For 16 combinations $(A = B) = 1$, and for 120 combinations $A < B = 1$.

For remaining 120 combination $A > B = 1$

Parity Bit Generator and Parity Bit Checker

When digital information is transmitted, it may not be received correctly by the receiver. To detect one bit error at receiver we can use parity checker.

For detection of error an extra bit, known as parity bit, is attached to each code word to make the number of 1's in the code even (in case of even parity) or odd (in case of odd parity).

For n-bit data, we use n-bit parity generator at the transmitter end. With 1 parity bit and n-bit data, total $n + 1$ bit will be transmitted. At the receiving end $n + 1$ parity checker circuit will be used to check correctness of the data.

For even parity transmission, parity bit will be made 1 or 0 based on the data, so that total $n + 1$ bits will have even number of 1's. For example, if we want to transmit data 1011 by even parity transmission, then we will use parity bit as 1, so data will have even number of 1's, i.e., data transmitted will be 11011. At the receiving end this data will be received and checked for even number of ones.

To transmit data $B_3B_2B_1B_0$ using even parity, we will transmit sequence $P\,B_3B_2B_1B_0$, where $P = B_3 \oplus B_2 \oplus B_1 \oplus B_0$. (Equation for parity generator)

At the receiving end we will check data received $PB_3B_2B_1B_0$ for error, $E = P \oplus B_3 \oplus B_2 \oplus B_1 \oplus B_0$ (equation for parity checker). If $E = 0$ (no error), or if $E = 1$ (1 bit error).

We use EX-OR gates for even parity generator/checker as EX-OR of bits gives output 1 if there are odd number of 1's else EX-OR output is 0.

Odd parity generator/checker is complement of even parity generator/checker. Odd parity circuits check for presence of odd number of 1's in data.

Code Converters

There are many situations where it is desired to convert from one code to another within a system. For example, the information from output of an analog to digital converter is often in gray code, before it can be processed in arithmetic unit, conversion to binary is required.

Let us consider simple example of 3-bit binary to gray code converter. This will have input lines supplied by binary codes and output lines must generate corresponding bit combination in gray code. The combination circuit code converter performs this transformation by means of logic gates.

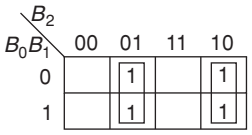
The output logic expression derived for code converter can be simplified by using the usual techniques including 'don't-care' if any present. For example, BCD code uses only codes from 0000 to 1001 and remaining combinations are treated as don't-care combinations. Similarly, EXS-3 uses only combinations from 0011 to 1100 and remaining combinations are treated as don't-care.

The relationship between the two codes is shown in the following truth table:

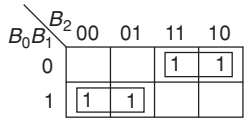
Decimal	B_2	B_1	B_0	G_2	G_1	G_0
0	0	0	0	0	0	0
1	0	0	1	0	0	1
2	0	1	0	0	1	1
3	0	1	1	0	1	0
4	1	0	0	1	1	0
5	1	0	1	1	1	1
6	1	1	0	1	0	1
7	1	1	1	1	0	0

For conversion we have to find out minimized functions of

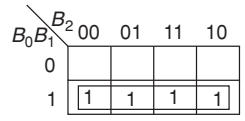
$$G_2(B_2, B_1, B_0) = \sum m(4, 5, 6, 7)$$
$$G_1(B_2, B_1, B_0) = \sum m(2, 3, 4, 5)$$
$$G_0(B_2, B_1, B_0) = \sum m(1, 2, 5, 6)$$



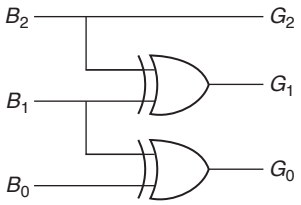
$$G_0(B_2, B_1, B_0) = B'_1B_0 + B_1B'_0 = B_1 \oplus B_0$$



$$G_1(B_2, B_1, B_0) = B'_1B_2 + B_1B'_2 = B_2 \oplus B_1$$



$$G_2(B_2, B_1, B_0) = B_2$$



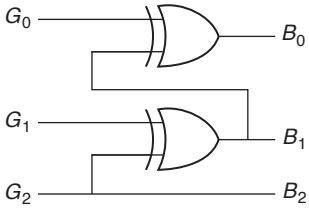
In similar fashion we can derive n-bit binary to gray code conversion as

$$G_n = B_n$$
$$G_{n-1} = B_{n-1} \oplus B_n$$
$$G_{i-1} = B_{i-1} \oplus B_i$$

Thus conversion can be implemented by $n - 1$ X-OR gates for n-bits.

For reverse conversion of gray to binary, by following similar standard principle of conversion, we will get

$$B_0 = G_0 \oplus G_1 \oplus G_2,\ B_1 = G_1 \oplus G_2,\ B_2 = G_2$$



In general for n-bit gray to binary code conversion

$$B_i = G_n \oplus G_{n-1} \oplus G_{n-2} \ldots \oplus G_{i-1} \oplus G_i$$

$B_n = G_n$ (MSB is same in gray and binary). It also requires $n-1$ X-OR gates for n-bits.

Example 2: Design 84-2-1 to XS-3 code converter.

Solution: Both 84-2-1 and *XS*-3 are *BCD* codes, each needs 4-bits to represent. The following table gives the relation between these codes. 84-2-1 is a weighted code, i.e., each position will have weight as specified. *XS*-3 is non-weighted code; the binary code is 3 more than the digit in decimal.

Decimal	84-2-1 $B_3B_2B_1B_0$	*XS*-3 $X_3X_2X_1X_0$
0	0000	0011
1	0111	0100
2	0110	0101
3	0101	0110
4	0100	0111
5	1011	1000
6	1010	1001
7	1001	1010
8	1000	1011
9	1111	1100

We will consider minterm don't-care combinations as 1, 2, 3, 12, 13, 14. For these combinations 84-2-1 code will not exist and the remaining minterms can be found from truth table.

$$X_0(B_3, B_2, B_1, B_0) = \sum m(0, 4, 6, 8, 10) + \sum \Phi(1, 2, 3, 12, 13, 14) = \overline{B_0}$$

$$X_1(B_3, B_2, B_1, B_0) = \sum m(0, 4, 5, 8, 9, 15) + \sum \Phi(1, 2, 3, 12, 13, 14) = \overline{B_1}$$

$$X_2(B_3, B_2, B_1, B_0) = \sum m(4, 5, 6, 7, 15) + \sum \Phi(1, 2, 3, 12, 13, 14) = B_2$$

$$X_3(B_3, B_2, B_1, B_0) = \sum m(8, 9, 10, 11, 15) + \sum \Phi(1, 2, 3, 12, 13, 14) = B_3$$

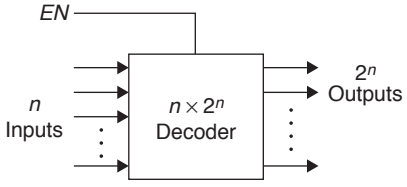
Decoder

A binary code of n-bits is capable of representing up to 2^n elements of distinct elements of coded information.

The three inputs are decoded into eight outputs, each representing one of the minterms of the three input variables.

A decoder is a combinational circuit that converts binary information from n input lines to a maximum 2^n unique output lines.

A binary decoder will have n inputs and 2^n outputs.



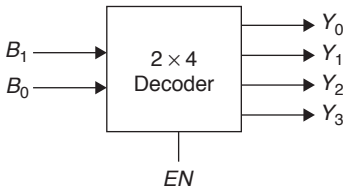


Figure 11 2 × 4 decoder

Table 5 *Truth Table*

EN	B_1	B_0	Y_3	Y_2	Y_1	Y_0
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

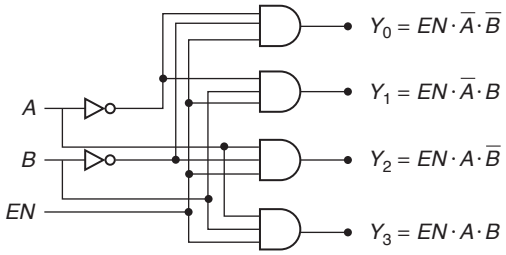


Figure 12 2 × 4 decoder

Decoder outputs are implemented by AND gates, but realization of AND gates at circuit level is done by the NAND gates (universal gates). So, the decoders available in IC form are implemented with NAND gates, i.e., the outputs are in complemented form and outputs are maxterms of the inputs rather than minterms of inputs as in AND gate decoders.

Furthermore, decoders include one or more enable inputs to control the circuit operation. Enable can be either active low/high input.

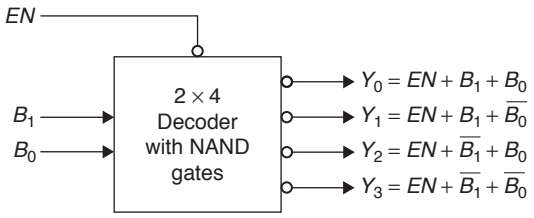


Figure 13 Active low 2 × 4 decoder

Table 6 *Truth Table*

EN	B_1	B_0	Y_3	Y_2	Y_1	Y_0
1	X	X	1	1	1	1
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1

The block diagram shown here is 2 × 4 decoder with active low output and active low enable input.

The logic diagram is similar to the previous 2 × 4 decoder, except, all AND gates are replaced by NAND gates and *EN* will have inverter, *EN* is connected to all NAND inputs, as $\overline{EN}$ is active low input for this circuit.

The decoder is enabled when EN is equal to 0.

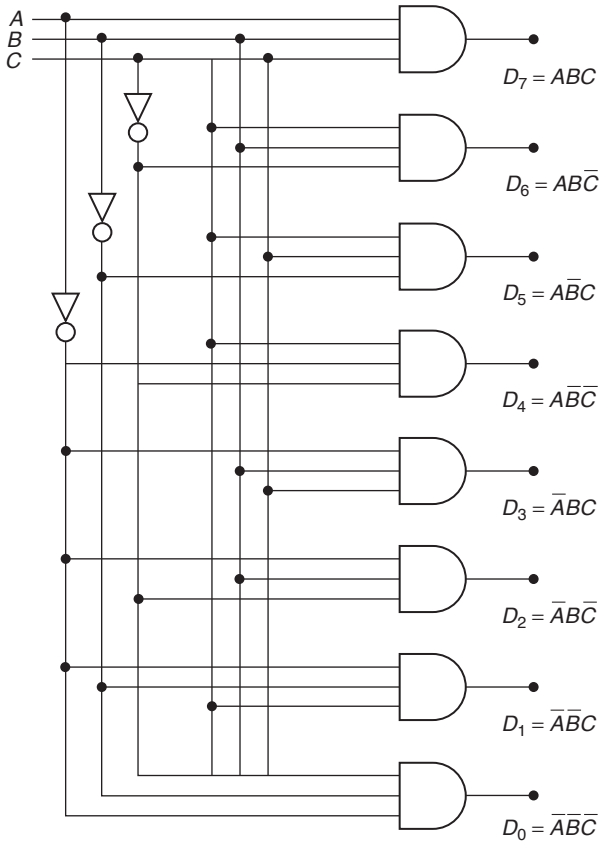
As shown in the truth table, only one output can be equal to 0 at any given time, all other outputs are equal to 1. The output whose value is equal to 0 represents the minterm selected by inputs, enable.

Consider a 3–8 line decoder

Table 7 *Truth Table*

Inputs			Outputs							
A	**B**	**C**	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

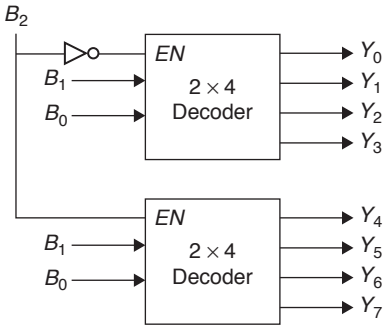
A 3–8 decoder has 3 input lines and 8 output lines, based on the combination of inputs applied for the 3 inputs, one of the 8 output lines will be made logic 1 as shown in the truth table. So, each output will have only one minterm.



Designing High Order Decoders from Lower Order Decoders

Decoder with enable input can be connected together to form larger decoder circuit.

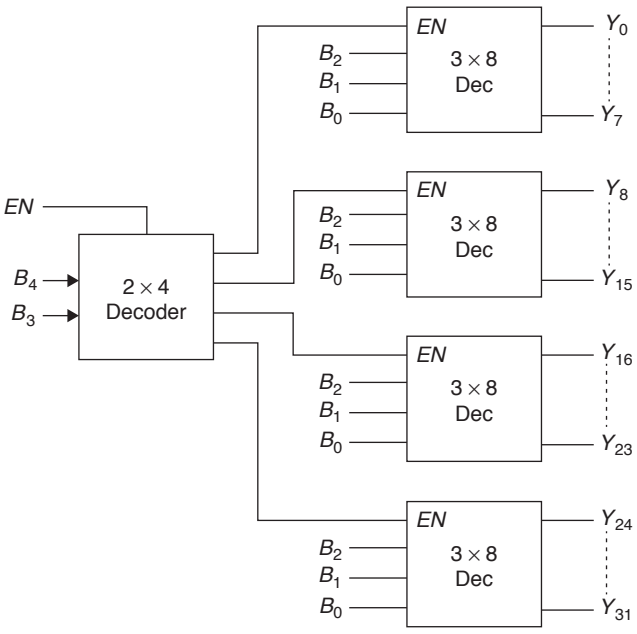
The following configuration shows 3 × 8 decoder with 2 × 4 decoders.



When $B_2 = 0$, top decoder is enabled and other is disabled, for 000–011 inputs, outputs are Y_0–Y_3, respectively, and other outputs are 0.

For $B_2 = 1$, the enable conditions are reversed.

The bottom decoder outputs generates minterms 100–111, while the outputs of top decoder are all 0's. 5 × 32 decoder with 3 × 8 decoders, 2 × 4 decoders



5 × 32 decoder will have 5 inputs $B_4 B_3 B_2 B_1 B_0$. 3 × 8 decoder will have 8 outputs, so 5 × 32 requires four 3 × 8 decoders, and we need one of the 2 × 4 decoders to select one 3 × 8 decoders and the connections are as shown in the circuit above.

Combinational Logic Implementation

An $n \times 2^n$ decoder provides 2^n minterms of n input variables. Since any Boolean function can be expressed in sum-of-minterms form, a decoder that generates the minterms of

the function, together with an external OR gate that forms their logical sum, provides a hardware implementation of the function.

Similarly, any function with n inputs and m outputs can be implemented with $n \times 2^n$ decoders and m OR gates.

Example 3: Implement full adder circuit by using 2×4 decoder.

Sum = Σ (1, 2, 4, 7), Carry = Σ (3, 5, 6, 7)

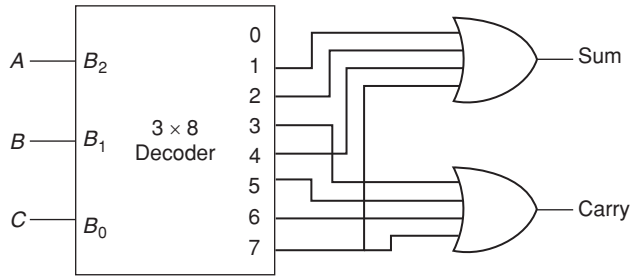


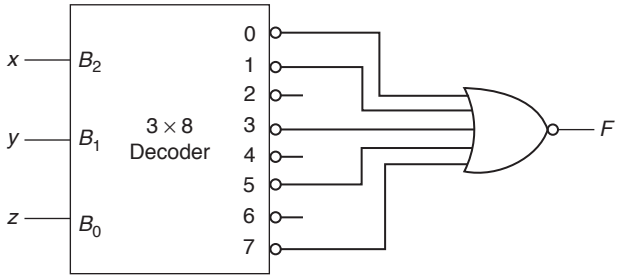
Figure 14 Implementation of full adder circuit with decoder

The 3×8 decoder generates the 8 minterms for A, B, and C. The OR gate for output sum forms the logical sum of minterms 1, 2, 4 and 7. The OR gate for output carry forms the logical sum of minterms 3, 5, 6 and 7.

Example 4: The minimized SOP form of output $F(x, y, z)$ is

(A) $x'y + z'$ (B) $x'y' + z'$

(C) $x'y' + z'$ (D) $x' + y'z$



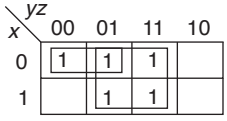
Solution: (C)

The outputs of decoder are in active low state. So, we can express outputs as $\overline{Y_7}, \overline{Y_6} \cdots \overline{Y_0}$

Outputs 0, 1, 3, 5, 7 are connected to NAND gate to form function $F(x, y, z)$

So
$$F = \overline{\overline{Y_0} \cdot \overline{Y_1} \cdot \overline{Y_3} \cdot \overline{Y_5} \cdot \overline{Y_7}}$$
$$= Y_0 + Y_1 + Y_3 + Y_5 + Y_7$$
$$= \Sigma(0, 1, 3, 5, 7)$$

By using K-maps

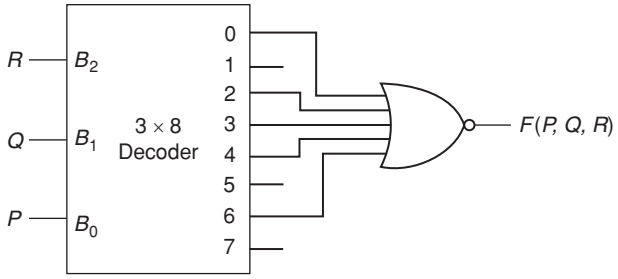


$F = z + x'y'$

Example 5. The minimal *POS* form of output function $f(P, Q, R)$ is

(A) $P\overline{Q} + PR$ (B) $P + \overline{Q}R$

(C) $P(\overline{Q} + R)$ (D) $Q(\overline{P} + R)$



Solution: (C)

The outputs of decoder are in normal form. 0, 2, 3, 4, 6 outputs are connected to NOR gate to form $F(P, Q, R)$

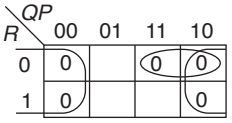
So
$$F = \overline{Y_0 + Y_2 + Y_3 + Y_4 + Y_6}$$
$$= \overline{Y_0} \cdot \overline{Y_2} \cdot \overline{Y_3} \cdot \overline{Y_4} \cdot \overline{Y_6}$$

$Y_0, Y_1, \ldots, Y_7$ indicate minterms, whereas $\overline{Y_0}, \overline{Y_1}, \cdots, \overline{Y_7}$ are maxterms.

So $F = \pi(0, 2, 3, 4, 6)$

Here, from the decoder circuit MSB is R, LSB is P.

By using K-map



$$F(P, Q, R) = P(R + \overline{Q})$$

Encoders

It is a digital circuit that performs the inverse operation of a decoder.

An encoder has 2^n (or fewer) input lines and n output lines.

It is also known as an octal to binary converter.

Consider an 8–3 line encoder:

Table 8 *Truth Table*

Inputs								Outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	A	B	C
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	1	0	0	1	1
0	0	0	0	1	0	0	1	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

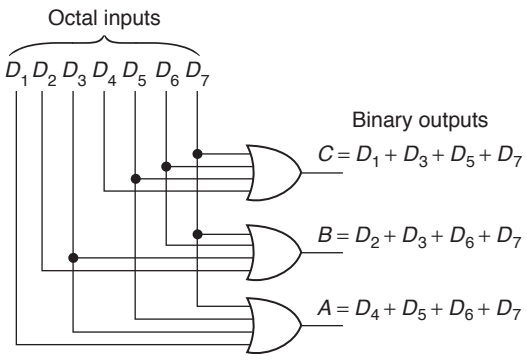


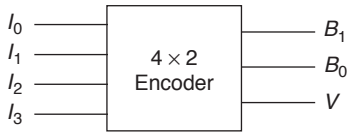
Figure 15 Logic diagram

Priority Encoder

A priority encoder is an encoder circuit that includes the priority function.

When two or more inputs are present, the input with higher priority will be considered.

Consider the 4 × 2 priority encoder.



I_3	I_2	I_1	I_0	B_1	B_0	V
1	X	X	X	1	1	1
0	1	X	X	1	0	1
0	0	1	X	0	1	1
0	0	0	1	0	0	1
0	0	0	0	X	X	0

I_3–I_0 are inputs and B_1 B_0 are binary output bits, valid (V) output is set to 1, when at least one input is present at input ($I_3 - I_0$).

When there is no input present, ($I_3 - I_0 = 0000$) then $V = 0$, for this combination the output B_1B_0 will not be considered.

The higher the subscript number, the higher the priority of the input. Input I_3 has the highest priority, I_2 has the next priority level. Input I_0 has lowest priority level. The Boolean expressions for output B_1 B_0 are

$$B_1 = I_3 + \overline{I}_3 I_2$$
$$= I_3 + I_2$$
$$B_0 = I_3 + \overline{I}_3 \overline{I}_2 I_1$$
$$= I_3 + \overline{I}_2 I_1$$
$$V = I_3 + I_2 + I_1 + I_0$$

Multiplexer

A multiplexer (MUX) is a device that allows digital information from several sources to be converted on to a single line for transmission over that line to a common destination.

The MUX has several data input lines and a single output line. It also has data select inputs that permits digital data on any one of the inputs to be switched to the output line.

Depending upon the binary code applied at the selection inputs, one (out of 2^n) input will be gated to single output. It is one of the most widely used standard logic circuits in digital design. The applications of multiplexer include data selection, data routing, operation sequencing, parallel to serial conversion, and logic function generation.

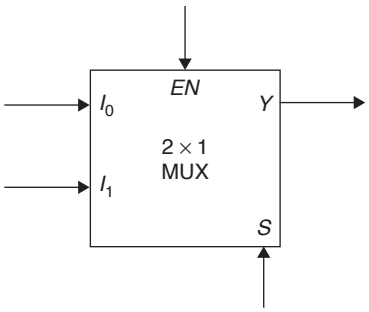
2^n inputs will be controlled by n selection lines and multiplexer will have 1 output, we denote it as $2^n \times 1$ multiplexer (data selector).

In other words, a multiplexer selects 1 out of n input data sources and transmits the selected data to a single output channel, this is called as multiplexing.

Basic 2 × 1 Multiplexer

The figure shows 2 × 1 multiplexer block diagram; it will have 2 inputs—I_0 and I_1, one selection line S, and one output Y. The function table is as shown here.

EN	S	Y
0	x	0
1	0	I_0
1	1	I_1

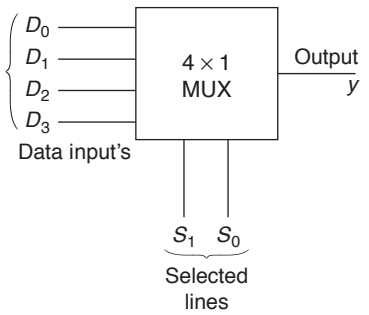


The output equation of 2 × 1 multiplexer is $Y = EN(I_0\overline{S} + I_1 S)$.

When enable is 1, the multiplexer will work in normal mode, else the multiplexer will be disabled.

Sometimes enable input will be active low enable $\overline{EN}$, then $Y = \overline{EN}(I_0\overline{S} + I_1 S)$.

The 4 × 1 Multiplexer



If a binary zero $S_1 = 0$ and $S_0 = 0$ as applied to the data select line the data input D_0 appear on the data output line and so on.

S_1	S_0	y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

$$y = \overline{S_1}\ \overline{S_0} D_0 + \overline{S_1} S_0 D_1 + S_1 \overline{S_0} D_2 + S_1 S_0 D_3$$

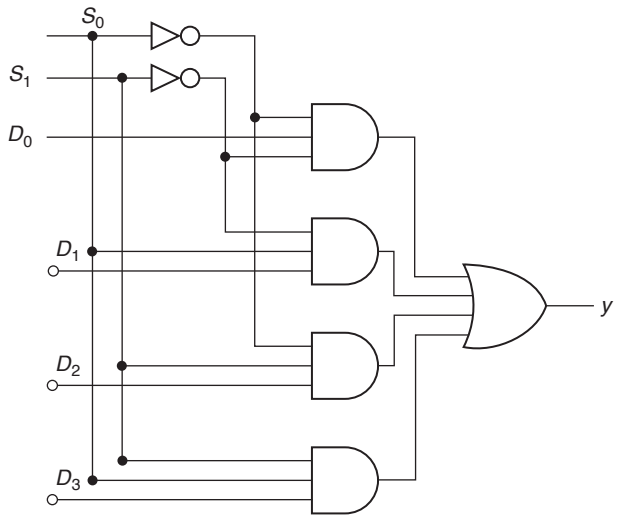


Figure 16 Logic diagram

For 8 × 1 multiplexer with 8 inputs from I_0–I_7 based on selection inputs $S_2 S_1 S_0$, the equation for output

$$Y = I_0 \overline{S_2} \overline{S_1} \overline{S_0} + I_1 \overline{S_2} \overline{S_1} S_0 + I_2 \overline{S_2} S_1 \overline{S_0} + I_3 \overline{S_2} S_1 S_0 + I_4 S_2 \overline{S_1} \overline{S_0} + I_5 S_2 \overline{S_1} S_0 + I_6 S_2 S_1 \overline{S_0} + I_7 S_2 S_1 S_0$$

From multiplexer equation, we can observe, each input is associated with its minterm (in terms of selection inputs).

Basic Gates by Using MUX

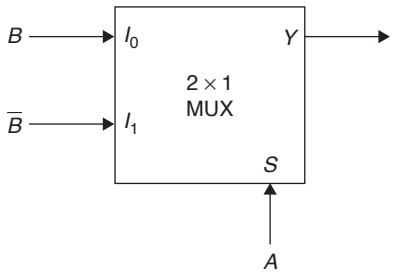


Figure 17 X-OR gate by using 2 × 1 MUX

$Y = \overline{A}B + A\overline{B}$ = X-OR gate, we can interchange inputs A and B also,

By interchanging inputs I_0 and I_1, $Y = \overline{A}\,\overline{B} + AB$, X-NOR gate.

Similarly, we can build all basic gates by using 2 × 1 multiplexer.

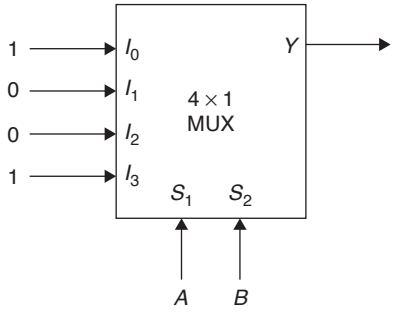
Example 6: If $I_0 = 1$, $I_1 = 0$, $S = A$, then Y is

Solution: $Y = (I_0 \overline{S} + I_1 S) = \overline{A}$. It Implements NOT gate.

Example 7: What should be the connections to implement NAND gate by using 2 × 1 MUX?

Solution: $Y = \overline{AB} = \overline{A} + \overline{B} = \overline{A} + A\overline{B} = 1 \cdot \overline{A} + \overline{B} \cdot A$

By considering $I_0 = 1$, $I_1 = \overline{B}$, $S = A$, we can implement NAND gate, or by interchanging A and B also we can get the same answer.



For the above 4 × 1 multiplexer $Y = \overline{AB} + AB$ = X-NOR gate, similarly to implement 2 input gates by using 4 × 1 multiplexer, the inputs I_0, I_1, I_2, I_3 should be same as the terms in the truth table of that gate.

Logic Function Implementation by Using Multiplexer

Let us consider a full subtractor circuit (borrow) to be implemented by using multiplexer.

Full subtractor borrow (B) is a function of 3 inputs X, Y, Z. The truth table is

X	Y	Z	B	4 × 1 MUX	2 × 1 MUX
0	0	0	0	$B = Z$	$B = Y + Z$
0	0	1	1		
0	1	0	1	$B = 1$	
0	1	1	1		
1	0	0	0	$B = 0$	$B = YZ$
1	0	1	0		
1	1	0	0	$B = Z$	
1	1	1	1		

To implement borrow by using 8 × 1 multiplexer, connect the three variables X, Y, Z directly to selection lines of the multiplexer, and connect the corresponding values of B to inputs, i.e., for $I_0 = 0$, $I_1 = 1$, $I_2 = 1$, etc. as per above truth table.

To implement borrow by using 4 × 1 multiplexer, connect any two variables to selection lines (in this case X, Y) and write output (B) in terms of other variable, for $XY = 00$, output B is same as Z, so connect $I_0 = Z$, similarly 1, 0, Z for remaining inputs.

To implement the function by using 2 × 1 multiplexer, connect 1 variable as selection line (in this case consider X) and write output (B) in terms of other variables, for $X = 0$,

output B is varies as $B = Y + Z$, so connect $I_0 = Y + Z$. For $X = 1$, output B varies as $B = YZ$, connect $I_1 = YZ$.

N–variable function can be implemented by using $2^{N-1} \times 1$ multiplexer without any extra hardware.

Implementation of Higher Order Multiplexer by Using Lower Order Multiplexers

By using lower order multiplexers, we can implement higher order multiplexers, for example by using 4×1 multiplexer, we can implement 8×1 MUX or 16×1 MUX or other higher order multiplexers.

Let us consider implementation of 16×1 MUX by using 4×1 MUX. 16×1 MUX will have inputs I_0–I_{15} and selection lines S_0–S_3, whereas 4×1 MUX will have only 4 input lines, and 2 selection lines, so we require four 4×1 MUX to consider all inputs I_0–I_{15}, and again to select one of the four outputs of these four multiplexers one more 4×1 multiplexer is needed (for which we will connect higher order selection lines S_2 and S_3). So, total of 5, 4×1 multiplexers are required to implement 16×1 MUX.

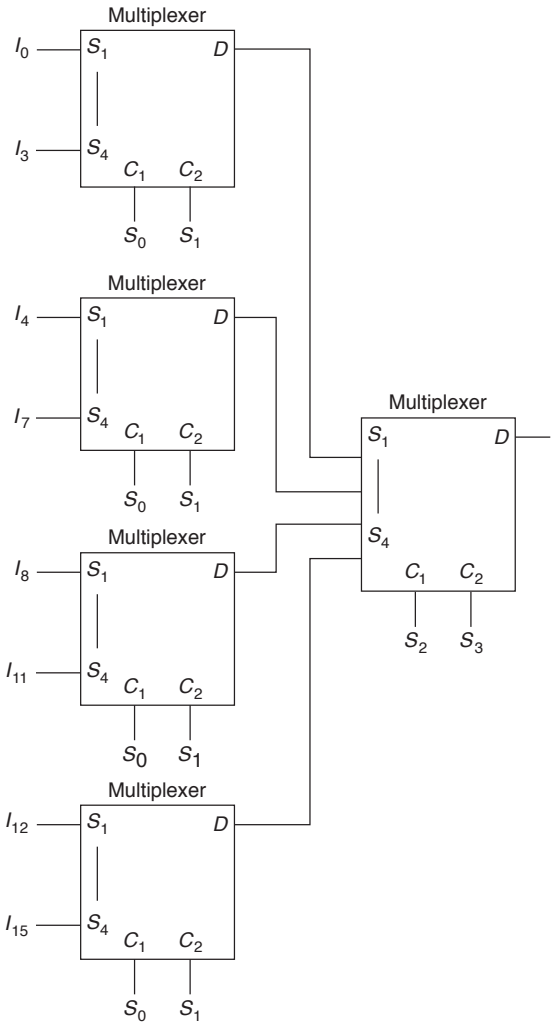


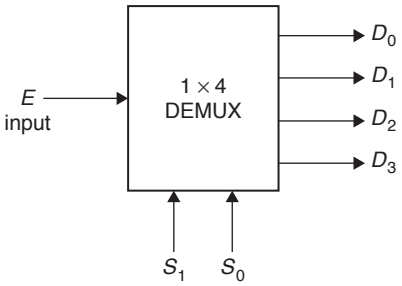
Figure 18 Realization of 16 x 1 multiplexer by using 4 x 1 multiplexers

In a similar fashion, to design 4×1 MUX, we require 3, 2×1 multiplexers, and to design 8×1 multiplexer, we require 7, 2×1 multiplexers.

Demultiplexer

The demultiplexer [DeMUX] basically serves opposite of the multiplexing function. It takes data from one line and distributes them to a given number of output lines.

The other name for demultiplexer is data distributor, as it receives information on a single line and distributes it to a possible 2^n output lines, where n is the number of selection lines, and value of n selects the line.



S_1	S_0	D_3	D_2	D_1	D_0
0	0	0	0	0	E
0	1	0	0	E	0
1	0	0	E	0	0
1	1	E	0	0	0

When $S_1S_0 = 10$; D_2 will be same as input E, and other outputs will be maintained at zero (0).

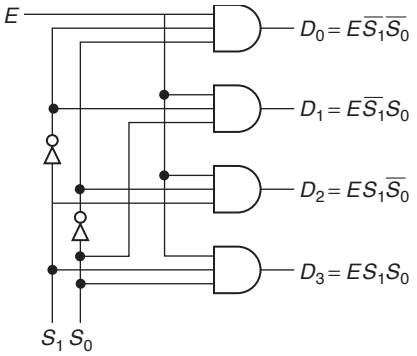
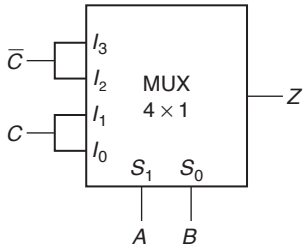


Figure 17 Logic diagram

Solved Examples

Example 1: The multiplexer shown in the figure is a 4 : 1 multiplexer. The output z is

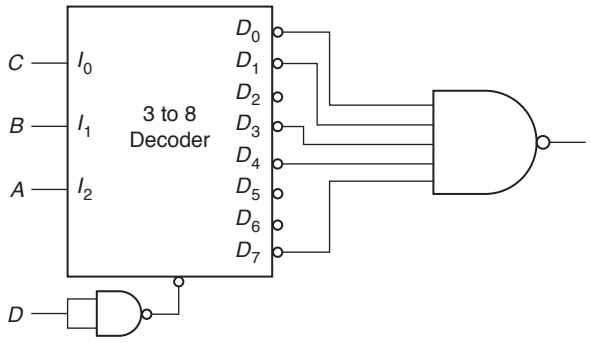


Solution:

A_1	B_0	Z
0	0	C
0	1	C
1	0	$\overline{C}$
1	1	$\overline{C}$

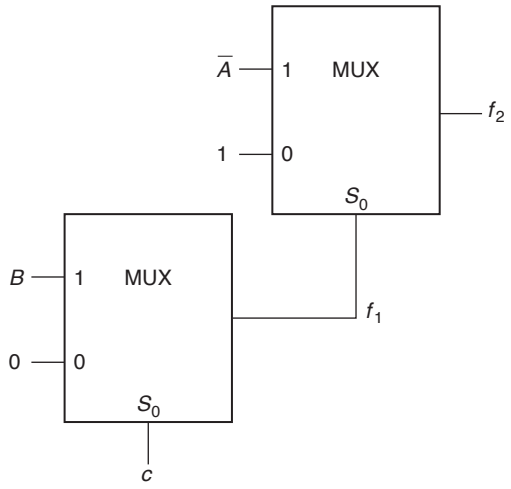
$$\therefore \quad Z = \overline{A}\,\overline{B}C + \overline{A}BC + AB\overline{C} + A\overline{B}\,\overline{C}$$
$$= \overline{B}(\overline{A}C + A\overline{C}) + B(\overline{A}C + A\overline{C})$$
$$= (\overline{A}C + A\overline{C})(B + \overline{B})(x + \overline{x} = 1)$$
$$\therefore \quad = \overline{A}C + A\overline{C} = A \oplus C$$

Example 2: The logic circuit shown in figure implements



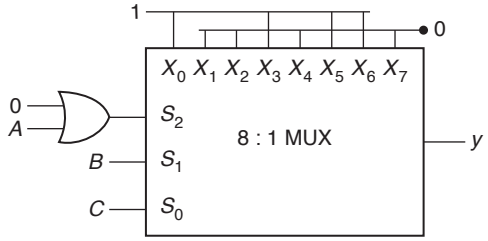
Solution: $z = D(\overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C + \overline{A}BC + A\overline{B}\,\overline{C} + ABC)$
$= D(\overline{A}\,\overline{B}(C + \overline{C}) + BC(\overline{A} + A) + A\overline{B}\,\overline{C})$
$\times D(\overline{B}\,\overline{A} + \overline{B}\,\overline{C} + BC)$
$= D(B \,\Theta\, C + \overline{A}\,\overline{B})$

Example 3. The network shown in figure implements



Solution: $f_1 = \overline{C}0 + CB = CB, f_1 = CB$
$F_2 = \overline{f_1} + f_1\overline{A} = \overline{A} \cdot CB + \overline{CB}$
$= \overline{A} + \overline{CB}$
$= \overline{A} + \overline{C} + \overline{B} = \overline{ABC}$
$\therefore$ NAND Gate

Example 4: In the TTL circuit in figure, S_2–S_0 are select lines and x_7–x_0 are input lines. S_0 and X_0 are LSBs. The output Y is

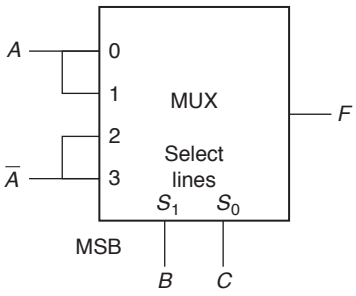


Solution: $S_2 = A, S_1 = B, S_0 = C$

$S_2(A)$	$S_1(B)$	$S_0(C)$	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

$$Y = \overline{A}\,\overline{B}\,\overline{C} + AB\overline{C} + A\overline{B}C + \overline{A}BC$$
$$= \overline{C}(\overline{A}\,\overline{B} + AB) + C(A\overline{B} + \overline{A}B)$$
$$Y = \overline{C}(\overline{A} \oplus B) + C(A \oplus B) = A \oplus B \odot C$$

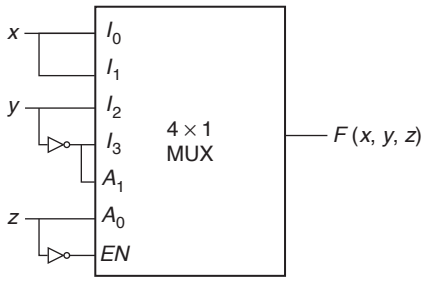
Example 5: The logic realized by the adjoining circuit is



Solution: $F = \overline{B}\,\overline{C}A + \overline{B}CA + B\overline{C}\,\overline{A} + BC\overline{A}$
$\times \overline{C}(\overline{B}A + B\overline{A}) + C(\overline{B}A + B\overline{A})$
$\times A\overline{B} + \overline{A}B(C + \overline{C}) = A \oplus B$

Example 6: Consider the following multiplexer, where I_0, I_1, I_2, I_3 are four date input lines selected by two address line combinations A_1A_0 = 00, 01, 10, 11, respectively and f

is the output of the multiplexer. *EN* is the enable input, the function $f(x, y, z)$ implemented by the below circuit is



Solution: $A_1 = \bar{y} \cdot A_0 = z, EN = \bar{z}$

A_1	A_0	S	I
0	0	$(y\bar{z})$	x
0	1	$(y\ z)$	x
1	0	$(\bar{y}\ \bar{z})$	y
1	1	$(\bar{y} z)$	$\bar{y}$

$$f(x, y, z) = \text{S.I} = (xy + 0 + \bar{y}z) \cdot EN$$
$$= xy \cdot \bar{z}$$

EXERCISES

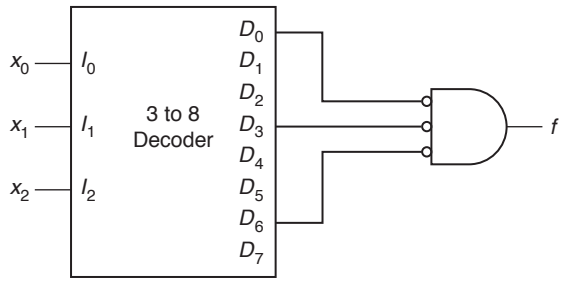
Practice Problems I

Directions for questions 1 to 21: Select the correct alternative from the given choices.

1. The binary number 110011 is to be converted to gray code. The number of gates and type required are
(A) 6, AND (B) 6, X-NOR
(C) 6, X-OR (D) 5, X-OR

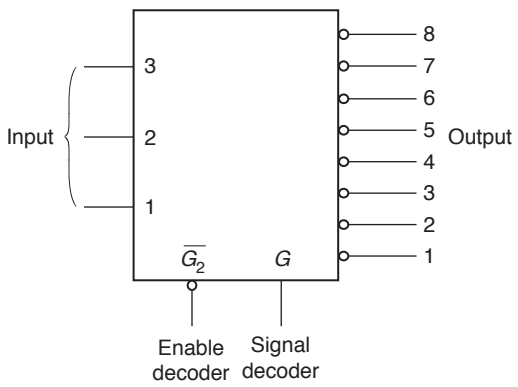
2. The number of 4-to 16-line decoder required to make an 8- to 256-line decoder is
(A) 16 (B) 17
(C) 32 (D) 64

3. $f(x_2, x_1, x_0) = ?$



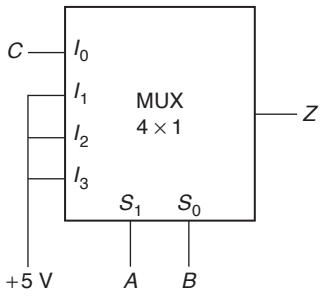
(A) $\pi(1, 2, 4, 5, 7)$ (B) $\Sigma(1, 2, 4, 5, 7)$
(C) $\Sigma(0, 3, 6)$ (D) $\pi(0, 2, 3, 6)$

4. A 3-to-8 decoder is shown below



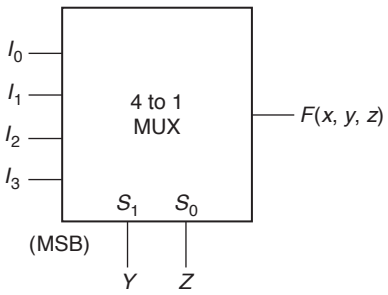
All the output lines of the chip will be high except pin 8, when all the inputs 1, 2, and 3
(A) are high; and G, G_2 are low
(B) are high; and G is low G_2 is high
(C) are high; and G, G_2 are high
(D) are high; and G is high G_2 is low

5. The MUX shown in figure is 4 × 1 multiplexer the output z is



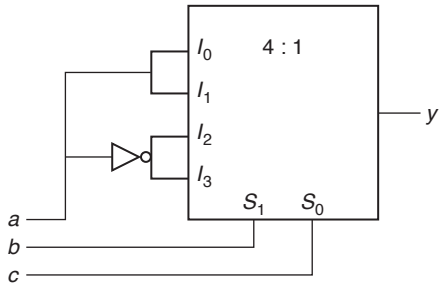
(A) $A\ B\ C$
(B) $A \oplus B \oplus C$
(C) $A\ \Theta\ B\ \Theta\ C$
(D) $A + B + C$

6. If a 4 to 1 MUX (shown below) realizes a three variable function $f(x, y, z) = xy + x\bar{z}$ then which of the following is correct?



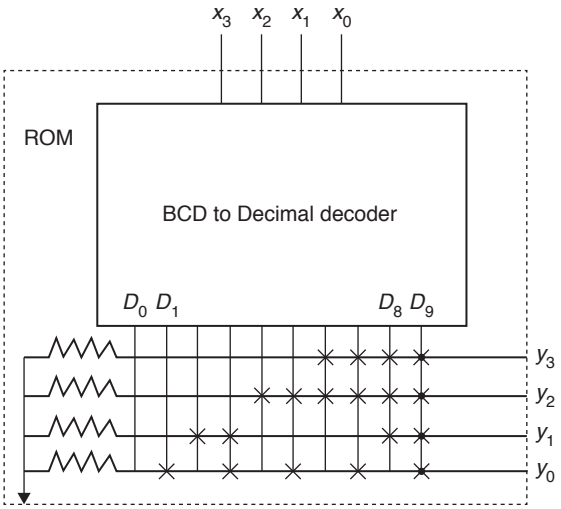
(A) $I_0 = X, I_1 = 0, I_2 = X, I_3 = X$
(B) $I_0 = 0, I_1 = 1, I_2 = Y_1, I_3 = X$
(C) $I_0 = X, I_1 = 1, I_2 = 0, I_3 = X$
(D) $I_0 = X, I_1 = 0, I_2 = X, I_3 = Z$

7. The circuit shown in the figure is same as



(A) two input NAND gate with a and c inputs
(B) two input NOR gate with a and c inputs
(C) two input X-OR gates with a and b inputs
(D) two input X-NOR gate with b and c inputs

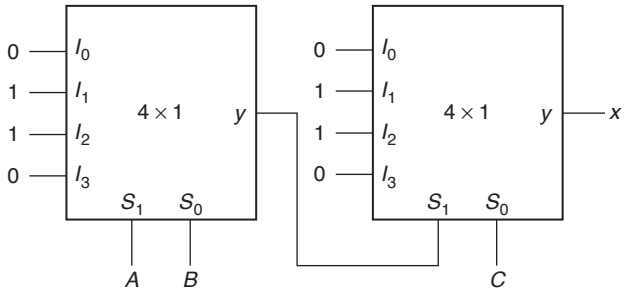
8. If the input x_3, x_2, x_1, x_0 to the ROM in the figure are 8421 BCD numbers, then the outputs y_3, y_2, y_1, y_0 are



(A) gray code numbers (B) 2421 *BCD*
(C) Excess – 3 code numbers (D) 84–2–1

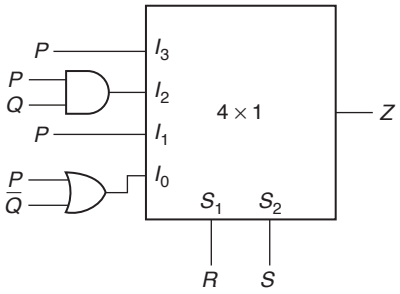
9. A 4-bit parallel full adder without input carry requires
(A) 8 HA, 4 OR gates (B) 8 HA, 3 OR gates
(C) 7 HA, 4 OR gates (D) 7 HA, 3 OR gates

10. In the circuit find X.



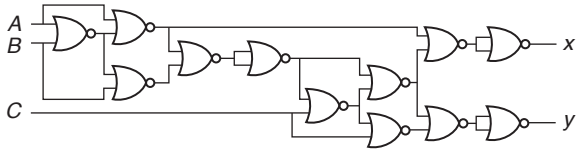
(A) $A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$
(B) $\bar{A}BC + A\bar{B}C + AB\bar{C} + \bar{A}\bar{B}\bar{C}$
(C) $AB + BC + AC$
(D) $\bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C}$

11. Find the function implemented.



(A) $PQ + PS + \bar{Q}\bar{R}\bar{S}$
(B) $P\bar{Q} + PQ\bar{R} + \bar{P}\bar{Q}\bar{S}$
(C) $P\bar{Q}\bar{R} + \bar{P}QR + PQRS + \bar{Q}\bar{R}\bar{S}$
(D) $PQ\bar{R} + PQR\bar{S} + P\bar{Q}\bar{R}S + \bar{Q}\,\bar{R}\,\bar{S}$

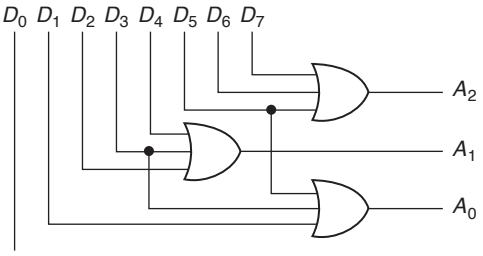
12. Which function is represented by the given circuit?



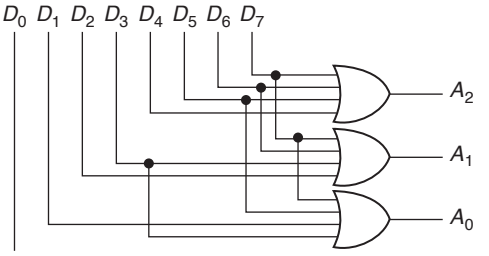
(A) Full adder (B) Full subtractor
(C) Comparator (D) Parity generator

13. Which of the following represents octal to binary encoder?

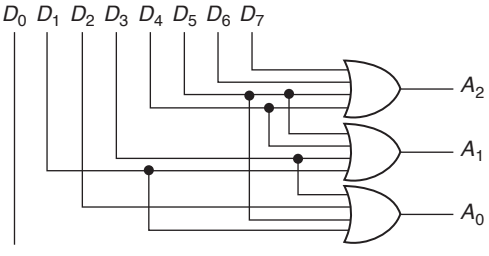
(A)



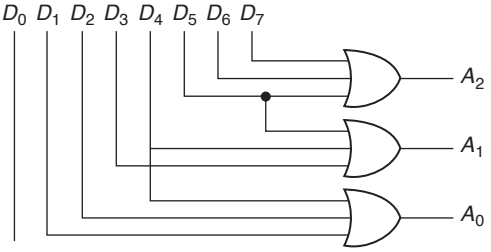
(B)



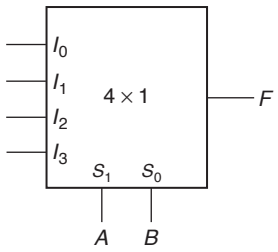
(C)



(D)



14. For a MUX to function as a full adder what should be the input provided to the I_0, I_1, I_2, I_3 if the A and B are the select lines?



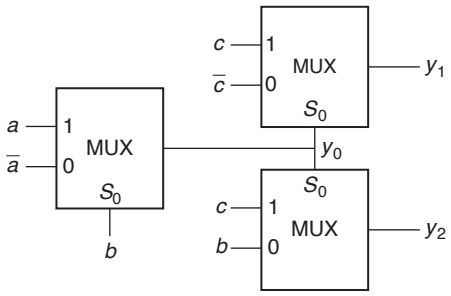
(A) $I_0 = I_1 = C_{in};\ I_2 = I_3 = \overline{C_{in}}$

(B) $I_0 = I_1 = \overline{C_{in}};\ I_2 = I_3 = C_{in}$

(C) $I_0 = I_3 = C_{in};\ I_1 = I_2 = \overline{C_{in}}$

(D) $I_0 = I_3 = \overline{C_{in}};\ I_1 = I_2 = C_{in}$

15. The given circuit act as



(A) Full adder (B) Half adder

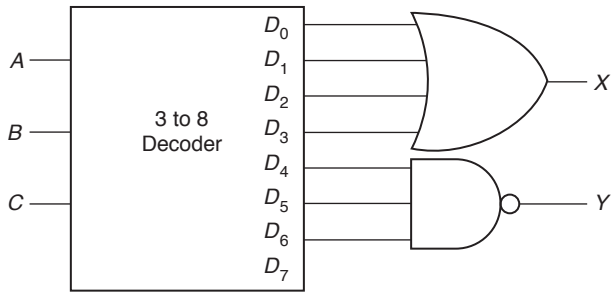
(C) Full subtractor (D) Half subtractor

16. For a 4 × 16 decoder circuit, the outputs of decoder ($y_0, y_1, y_4 \cdot y_5 \cdot y_{10} \cdot y_{11} \cdot y_{14} \cdot y_{15}$) are connected to 8 input NOR gate, the expression of NOR gate output is

(A) $A \oplus D$ (B) $A \odot D$

(C) $A \odot C$ (D) $A \oplus C$

17. The function implemented by decoder is



(A) $X = A'BC' + B'C', y = A + B$

(B) $X = A'C' + B'C', y = 1$

(C) $X = \overline{A},\ y = 0$

(D) $X = \overline{A},\ y = 1$

18. A relay is to operate with conditions that it should be on when the input combinations are 0000, 0010, 0101, and 0111. The states 1000, 1001, 1010 don't occur. For rest of the status, relay should be off. The minimized Boolean expression notifying the relationship is

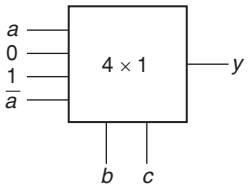
(A) $BC + ACD$

(B) $\overline{B}\overline{D} + \overline{A}BD$

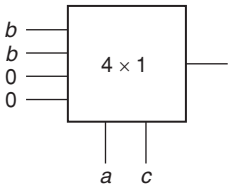
(C) $BD + AC$

(D) $AB + CD$

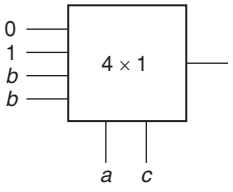
19. If a function has been implemented using MUX as shown, implement the same function with a and c as the select lines



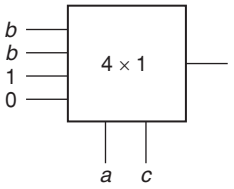
(A)



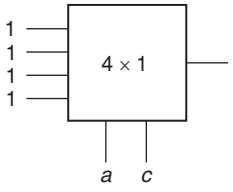
(B)



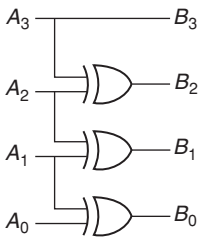
(C)



(D)



20. The circuit is used to convert one code to another. Identify it.



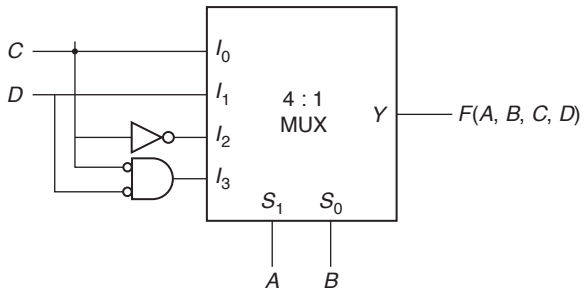
(A) Binary to gray

(B) Gray to binary

(C) Gray to XS–3

(D) Gray to 8421

21. The Boolean function realised by logic circuit is



(A) $F = \Sigma m(0, 1, 3, 5, 9, 10, 14)$

(B) $F = \Sigma m(2, 3, 5, 7, 8, 12, 13)$

(C) $F = \Sigma m(1, 2, 4, 5, 11, 14, 15)$

(D) $F = \Sigma m(2, 3, 5, 7, 8, 9, 12)$

Practice Problems 2

Directions for questions 1 to 21: Select the correct alternative from the given choices.

1. For a binary half subtractor having two input A and B, the correct set of logical expression for the outputs D = (A minus B) and X (borrow) are

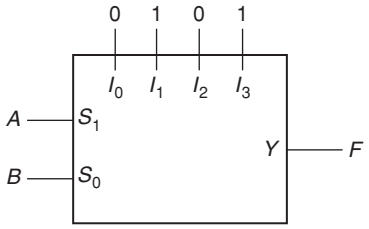
(A) $D = AB + \overline{AB}, X = \overline{A}B$

(B) $D = \overline{AB} + A\overline{B}+, A\overline{B}, X = \overline{A}B$

(C) $D = \overline{A}B + A\overline{B}, X = \overline{A}B$

(D) $D = AB + \overline{A}\,\overline{B}, X = \overline{A}B$

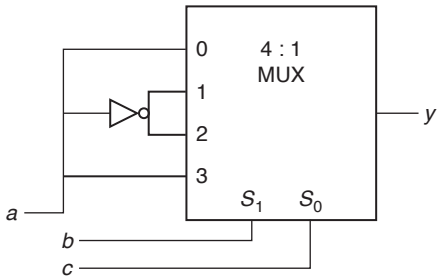
2. The function 'F' implemented by the multiplexer chip shown in the figure is



(A) A (B) B

(C) $\overline{A}B$ (D) $A\overline{B} + \overline{A}B$

3 The following multiplexer circuit is equal to



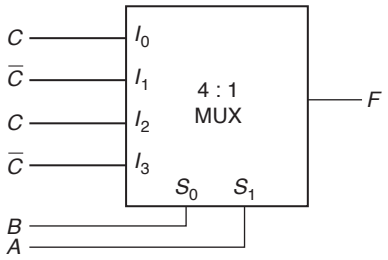
(A) implementation of sum equation of full adder

(B) implementation of carry equation of full adder

(C) implementation of borrow equation of full substractor

(D) all of the above

4 The output 'F' of the multiplexer circuit shown in the figure will be



(A) $AB + B\overline{C} + \overline{C}A + \overline{B}\overline{C}$ (B) $A \oplus B \oplus C$

(C) $A \oplus B$ (D) $B \oplus C$

5. Full subtractor can be implemented by using

(A) 3-to-8 line decoder only

(B) 3-to-8 line decoder and one OR gate

(C) 3-to-8 line decoder and two OR gates

(D) None

6. What are the difference and borrow equations for the above circuit?

(A) $D = x \Theta y \Theta z, B = x'y + yz + zx'$

(B) $D = X \oplus y \oplus z, B = xy + yz + zx$

(C) $D = x \oplus y \oplus z, B = x'y + yz + zx'$

(D) A and C both

7. Combinational circuits are one in which output depends _____, whereas sequential circuit's output depends _____

(A) only on present input, only on past input

(B) only on present input, only on past and future input

(C) only on present input, only on present input and past output

(D) on present input, on past and present output

8. The sum output of the half adder is given by (assume A and B as inputs)

(A) $S = AB(\overline{A+B})$ (B) $S = (A+B)\overline{AB}$

(C) $S = (A+B)(AB)$ (D) $S = (\overline{A}+\overline{B})(\overline{AB})$

9. MUX implements which of the following logic?

(A) NAND–XOR (B) AND–OR

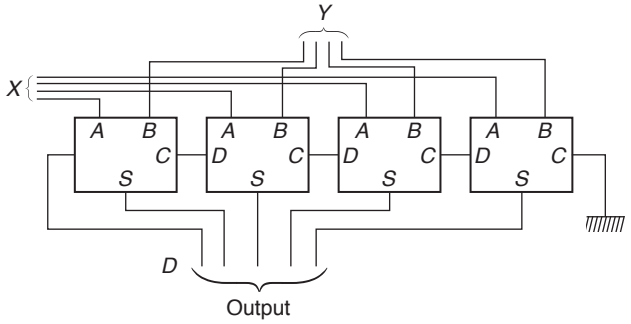
(C) OR–AND (D) XOR–NOT

10. A DeMUX can be used as a

(A) Comparator (B) Encoder

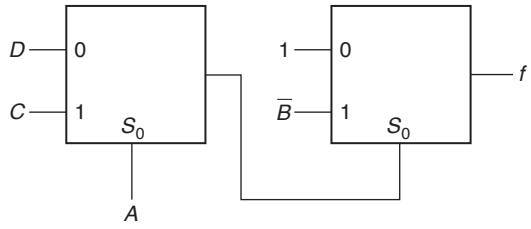
(C) Decoder (D) Adder

11. If we have inputs as A, B and C and output as S and D. We are given that $S = A \oplus B \oplus C$. $D = BC + \overline{A}B + \overline{A}C$. Which of the circuit is represented by it?



(A) 4-bit adder giving $X + Y$
(B) 4-bit subtractor giving $X - Y$
(C) 4-bit subtractor giving $Y - X$
(D) 4-bit adder giving $X + Y + S$

12. The Boolean function f implemented in the figure using two input multiplexers is



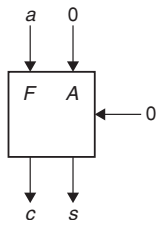
(A) $A\overline{C} + \overline{A}\overline{D} + \overline{D}C + \overline{A}\overline{B}D + A\overline{B}C$
(B) $\overline{A} + A\overline{C} + \overline{A}\overline{D} + \overline{D}\overline{C}$
(C) $\overline{B} + A\overline{C} + \overline{A}\overline{D} + \overline{D}\overline{C}$
(D) $AC + AD + A + B$

13. The carry generate and carry propagate function of the look ahead carry adder is
(A) $CG = A + B$, $CP = A \oplus B$
(B) $CG = A \oplus B$, $CP = A + B$
(C) $CG = AB$, $CP = A \oplus B$
(D) $CG = AB$, $CP = A + B$

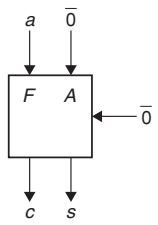
14. If we have a comparator and if E represents the condition for equality i.e., $(A_n \oplus B_n)$, if A_n and B_n are to be compared then the expression $A_3\overline{B}_3 + E_3A_2\overline{B}_2 + E_3E_2A_1\overline{B}_1 + E_3E_2E_1A.\overline{B}$. represents which of the condition for a 4-bit number?
(A) $A > B$ (B) $B > A$
(C) $A = B$ (D) None of these

15. When full adder is used to function as a 1-bit incrementor, which of the circuit configurations must be used?

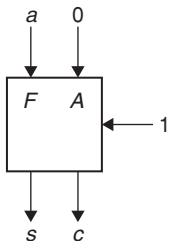
(A)



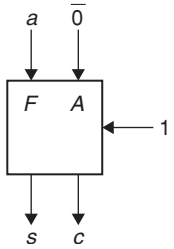
(B)



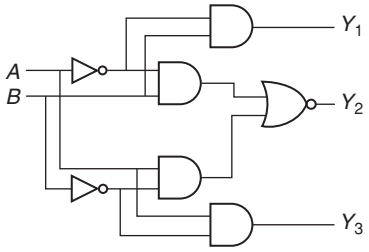
(C)



(D)



16. Identify the circuit.



(A) Half adder
(B) Full adder
(C) 1-bit magnitude comparator
(D) Parity generator

17. In order to implement n variable function (without any extra hardware) the minimum order of MUX is
(A) $2^n \times 1$ (B) $2^n \times 1$
(C) $(2^n - 1) \times 1$ (D) $(2^{n-1}) \times 1$

18. A full adder circuit can be changed to full subtractor by adding a
(A) NOR gate (B) NAND gate
(C) Inverter (D) AND gate

19. The half adder when implemented in terms of NAND logic is expressed as
(A) $A \oplus B$ (B) $\overline{A \cdot \overline{AB} \cdot B \cdot \overline{AB}}$
(C) $\overline{A \cdot \overline{AB}} \cdot \overline{B \cdot \overline{AB}}$ (D) $\overline{A \cdot \overline{ABB} \cdot \overline{AB}}$

20. For a DeMUX to act as a decoder, what is the required condition?
(A) Input should be left unconnected and select lines behave as a input to decoder
(B) Input should be always 0 and select line behave as inputs to decoder
(C) Both are same
(D) Input should become enable and select lines behave as inputs to decoder

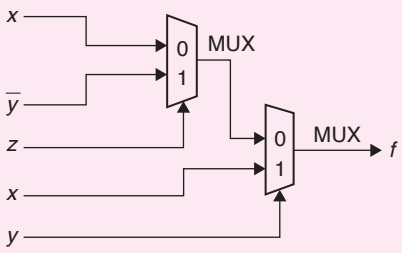
21. For a full subtractor, which of the combination will give the difference?
(A) $\overline{(A \oplus B)\overline{(A \oplus B)b_i}} \cdot \overline{b_i\overline{(A \oplus B)b_i}}$
(B) $\overline{B \cdot \overline{AB} \cdot \overline{b_i(A \oplus B)}}$
(C) $\overline{\overline{A} + \overline{B}} + \overline{b_i} + \overline{\overline{A \oplus B}}$
(D) None of these

Previous Years' Questions

1. A 4-bit carry look ahead adder, which adds two 4-bit numbers, is designed using AND, OR, NOT, NAND, NOR gates only. Assuming that all the inputs are available in both complemented and uncomplemented forms and the delay of each gate is one time unit, what is the overall propagation delay of the adder? Assume that the carry network has been implemented using two-level AND–OR logic. **[2004]**

(A) 4 time units (B) 6 time units
(C) 10 time units (D) 12 time units

2.



Consider the circuit above. Which one of the following options correctly represents $f(x, y, z)$? **[2006]**

(A) $x\bar{z} + xy + \bar{y}z$ (B) $x\bar{z} + xy + \overline{\bar{y}z}$
(C) $xz + xy + \overline{\bar{y}z}$ (D) $xz + x\bar{y} + \bar{y}z$

3. Given two 3-bit numbers $a_2a_1a_0$ and $b_2b_1b_0$ and c, the carry in, the function that represents the carry generate function when these two numbers are added is **[2006]**

(A) $a_2b_2 + a_2a_1b_1 + a_2a_1a_0b_0 + a_2a_0b_1b_0 + a_1b_2b_1 + a_1a_0b_2b_0 + a_0b_2b_1b_0$
(B) $a_2b_2 + a_2b_1b_0 + a_2a_1b_1b_0 + a_1a_0b_2b_1 + a_1a_0b_2 + a_1a_0b_2b_0 + a_2a_0b_1b_0$
(C) $a_2 + b_2 + (a_2 \oplus b_2)\,(a_1 + b_1 + (a_1 \oplus b_1)(a_0 + b_0))$
(D) $a_2b_2 + \overline{a_2}a_1b_1 + \overline{a_2a_1}a_0b_0 + \overline{a_2}a_0\overline{b_1}b_0 + a_1\overline{b_2}b_1 + \overline{a_1}a_0\overline{b_2}b_0 + a_0\overline{b_2b_1}b_0$

4. We consider the addition of two 2's complement numbers $b_{n-1}b_{n-2} \ldots b_0$ and $a_{n-1}a_{n-2} \ldots a_0$. A binary adder for adding unsigned binary numbers is used to add the two numbers. The sum is denoted by $c_{n-1}c_{n-2} \ldots c_0$ and the carry-out by c_{out}. Which one of the following options correctly identifies the overflow condition? **[2006]**

(A) $c_{out}\overline{(a_{n-1} \oplus b_{n-1})}$
(B) $a_{n-1}b_{n-1}\overline{c_{n-1}} + \overline{a_{n-1}}\,\overline{b_{n-1}}c_{n-1}$
(C) $c_{out} \oplus c_{n-1}$
(D) $a_{n-1} \oplus b_{n-1} \oplus c_{n-1}$

5. Consider numbers represented in 4-bit gray code. Let $h_3h_2h_1h_0$ be the gray code representation of a number n and let $g_3g_2g_1g_0$ be the gray code of $(n + 1)$ modulo 16 value of the number. Which one of the following functions is correct? **[2006]**

(A) $g_0(h_3h_2h_1h_0) = \Sigma(1, 2, 3, 6, 10, 13, 14, 15)$
(B) $g_1(h_3h_2h_1h_0) = \Sigma(4, 9, 10, 11, 12, 13, 14, 15)$
(C) $g_2(h_3h_2h_1h_0) = \Sigma(2, 4, 5, 6, 7, 12, 13, 15)$
(D) $g_3(h_3h_2h_1h_0) = \Sigma(0, 1, 6, 7, 10, 11, 12, 13)$

6. How many 3-to-8 line decoders with an enable input are needed to construct a 6-to-64 line decoder without using any other logic gates? **[2007]**

(A) 7 (B) 8
(C) 9 (D) 10

7. Suppose only one multiplexer and one inverter are allowed to be used to implement any Boolean function of n variables. What is the minimum size of the multiplexer needed? **[2007]**

(A) 2^n line to 1 line (B) 2^{n+1} line to 1 line
(C) 2^{n-1} line to 1 line (D) 2^{n-2} line to 1 line

8. In a look-ahead carry generator, the carry generate function G_i and the carry propagate function P_i for inputs A_i and B_i are given by:

$P_i = A_i \oplus B_i$ and $G_i = A_iB_i$

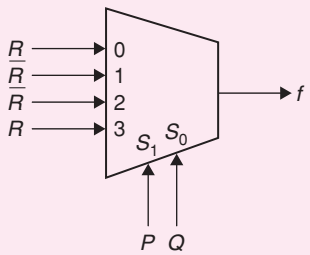
The expressions for the sum bit S_i and the carry bit C_{i+1} of the look-ahead carry adder are given by:

$S_i = P_i \oplus C_i$ and $C_{i+1} = G_i + P_iC_i$, where C_0 is the input carry.

Consider a two-level logic implementation of the look-ahead carry generator. Assume that all P_i and G_i are available for the carry generator circuit and that the AND and OR gates can have any number of inputs. The number of AND gates and OR gates needed to implement the look-ahead carry generator for a 4-bit adder with S_3, S_2, S_1, S_0 and C_4 as its outputs are respectively: **[2007]**

(A) 6, 3 (B) 10, 4
(C) 6, 4 (D) 10, 5

9. The Boolean expression for the output f of the multiplexer shown below is



(A) $\overline{P \oplus Q \oplus R}$
(B) $P \oplus Q \oplus R$
(C) $P + Q + R$
(D) $\overline{P + Q + R}$

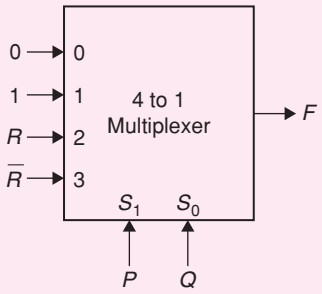
10. The amount of ROM needed to implement a 4-bit multiplier is **[2012]**
(A) 64 bits
(B) 128 bits
(C) 1K bits
(D) 2K bits

11. In the following truth table, $V = 1$ if and only if the input is valid.

Inputs				Outputs		
D_0	D_1	D_2	D_3	X_0	X_1	V
0	0	0	0	x	x	0
1	0	0	0	0	0	1
x	1	0	0	0	1	1
x	x	1	0	1	0	1
x	x	x	1	1	1	1

What function does the truth table represent? **[2013]**
(A) Priority encoder
(B) Decoder
(C) Multiplexer
(D) Demultiplexer

12. Consider the 4-to-1 multiplexer with two select lines S_1 and S_0 given below.



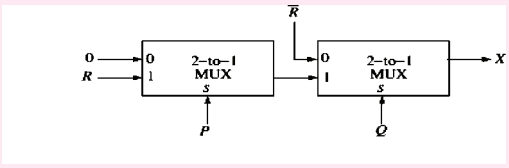
The minimal sum-of-products form of the Boolean expression for the output F of the multiplexer is **[2014]**
(A) $\overline{P}Q + Q\overline{R} + P\overline{Q}R$
(B) $\overline{P}Q + \overline{P}Q\overline{R} + PQ\overline{R} + P\overline{Q}R$
(C) $\overline{P}QR + \overline{P}Q\overline{R} + Q\overline{R} + P\overline{Q}R$
(D) $PQ\overline{R}\ \overline{P}QR + \overline{P}Q\overline{R} + Q\overline{R} + P\overline{Q}R$

13. Consider the following combinational function block involving four Boolean variables x, y, a, b, where x, a, b are inputs and y is the output. **[2014]**
$f(x, y, a, b)$
{
if (x is 1) $y = a$;
else $y = b$;
}
Which one of the following digital logic blocks is the most suitable for implementing this function?
(A) Full adder
(B) Priority encoder
(C) Multiplexer
(D) Flip–flop

14. Let $\oplus$ denote the Exclusive OR (X-OR) operation. Let '1' and '0' denote the binary constants. Consider the following Boolean expression for F over two variables P and Q:
$F(P, Q) = ((1 \oplus P) \oplus (P \oplus Q)) \oplus ((P \oplus Q) \oplus (Q \oplus 0))$ **[2014]**
The equivalent expression for F is
(A) $P + Q$
(B) $\overline{P + Q}$
(C) $P \oplus Q$
(D) $\overline{P \oplus Q}$

15. A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit ripple-carry binary adder is implemented by using four full adders. The total propagation time of this 4-bit binary adder in microseconds is _____ **[2015]**

16. Consider the two cascaded 2-to-1 multiplexers as shown in the figure.



minimal sum of products form of the output x is
The minimal sum of products form of the output X is **[2016]**
(A) $\overline{P}\ \overline{Q} + PQR$
(B) $\overline{P}\ Q + QR$
(C) $PQ + \overline{P}\ \overline{Q}\ R$
(D) $\overline{P}\ \overline{Q} + PQR$

17. When two 8-bit numbers $A_7 \ldots A_0$ and $B_7 \ldots B_0$ in 2's complement representation (with A_0 and B_0 as the least significant bits) are added using a **ripple-carry adder**, the sum bits obtained are $S_7 \ldots S_0$ and the carry bits are $C_7 \ldots C_0$. An overflow is said to have occurred if **[2017]**
(A) the carry bit C_7 is 1
(B) all the carry bits $(C_7, \ldots, C_0)$ are 1
(C) $(A_7 \cdot B_7 \cdot \overline{S_7} + \overline{A_7} \cdot \overline{B_7} \cdot S_7)$ is 1
(D) $(A_0 \cdot B_0 \cdot \overline{S_0} + \overline{A_0} \cdot \overline{B_0} \cdot S_0)$ is 1

Answer Keys

Exercises

Practice Problems 1

1. D	**2.** B	**3.** B	**4.** D	**5.** D	**6.** A	**7.** C	**8.** B	**9.** D	**10.** A
11. A	**12.** B	**13.** B	**14.** C	**15.** C	**16.** D	**17.** D	**18.** B	**19.** C	**20.** A
21. D									

Practice Problems 2

1. C	**2.** B	**3.** A	**4.** D	**5.** C	**6.** C	**7.** C	**8.** B	**9.** B	**10.** C
11. B	**12.** C	**13.** C	**14.** A	**15.** C	**16.** C	**17.** B	**18.** C	**19.** C	**20.** D
21. A									

Previous Years' Questions

1. B	**2.** A	**3.** A	**4.** B	**5.** C	**6.** C	**7.** C	**8.** B	**9.** B	**10.** D
11. A	**12.** A	**13.** C	**14.** D	**15.** 19.2	**16.** D	**17.** C			