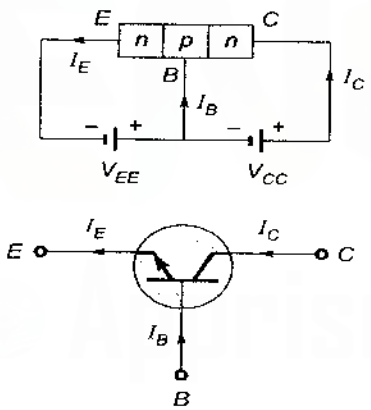
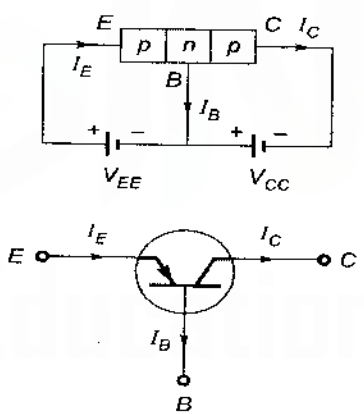
Bipolar Junction Transistors

3

- A transistor is 3 layer, 3 terminal, 2 junction semiconductor device.
- It consist of either two *n*-type and one *p*-type layers of material called *npn* transistor or two *p*-type and one *n*-type material called *pnp* transistor.
- In transistor current flows due to both majority as well as minority carrier that's why called a bipolar device.
- It is a current controlled device.
- Its input impedance is low and output impedance is high.
- Thermal stability is lesser because of leakage current or reverse saturation current.
- In transistor all the major currents are diffusion currents.
- Base current is recombination current.
- A transistor represented by two diode connected back to back cannot work as transistor as there is no bonding between base and collector.
- Current conduction in *pnp* transistor is carried out by hole whereas in *npn* transistor it is due to electrons.



(a) *npn* transistor

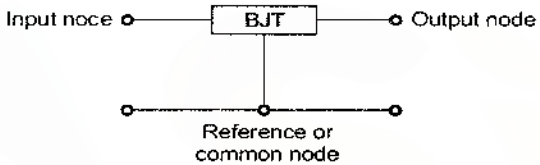


(a) *pnp* transistor

Transistor Sections

1. **Emitter:** It is heavily doped as comparison to other regions. The main function of this region is to supply majority charge carrier i.e. either electrons or holes.
2. **Base:** This section is very lightly doped and very thin as compare to other section. Its main function is to transfer the majority carriers from emitter to collector.
3. **Collector:** This sect on is moderately doped and has largest area than other two regions because it collects the charge carries from emitter and base. There is a large amount of heat liberation and so it is provided with large area to dissipate the heat.

BJT Configuration



Based on the reference node a BJT can be used in 3 configuration as given in table below:

Configuration	Input node	Output node
Common Base (CB)	*E*	*C*
Common Emitter (CE)	*B*	*C*
Common Collector (CC)	*B*	*E*

Mode of Operation

Mode	Emitter-base junction	Collector-base junction	Properties	Application
Cut-off	Reverse bias	Reverse bias	Very high internal resistance	OFF-switch
Active	Forward bias	Reverse bias	Excellent transistor action	Amplifier
Saturation	Forward bias	Forward bias	Very low internal resistance	ON-switch
Reverse active	Reverse bias	Forward bias	Very poor transistor action	Attenuator (Practically not used)

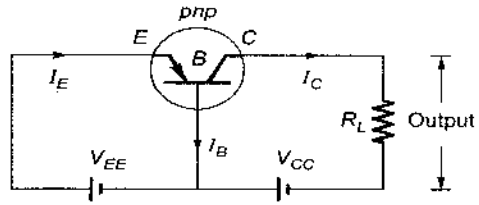
1. Common Base Configuration

$$I_E = I_B + I_C + I_{CBO}$$

or $$I_E = I_B + I_C$$

where, I_E = Emitter current

I_B = Base current



Common base *pnp* transistor

I_C = Collector current

I_{CBO} = Collector to base leakage current

Note:

$I_B \approx 2\%$ of I_E ; $I_C \approx 98\%$ of I_E.

Current amplification factor (α)

When no signal is applied then the ratio of the collector current to emitter current is called current amplification factor or current gain.

$$\alpha = \frac{I_C}{I_E} = 98\%$$

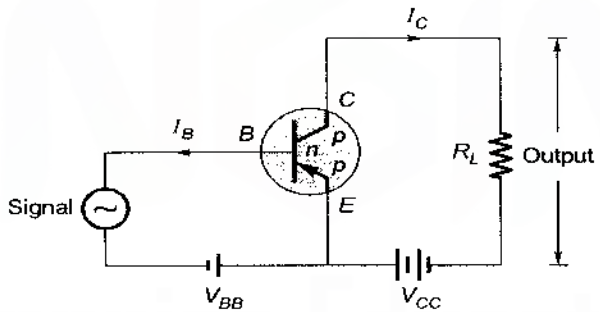
Note:

α of a transistor is a measure of the quality of transistor. Higher is the value of α better is the transistor as I_C approaches I_E.

Collector current also be expressed as

$$\boxed{I_C = \alpha I_E + I_{CBO}}$$

2. Common Emitter Configuration



Common emitter *pnp* transistor

Base current amplification factor (β)

When no signal is applied, then the ratio of collector current to the base current is called β.

$$\boxed{\beta = \frac{I_C}{I_B}} \quad ; \quad \text{Also} \quad \boxed{\alpha = \frac{\beta}{1+\beta}}$$

Note:

- β ranges from 20 to 500.
- This configuration is used when appreciable current gain as well as voltage gain is required.

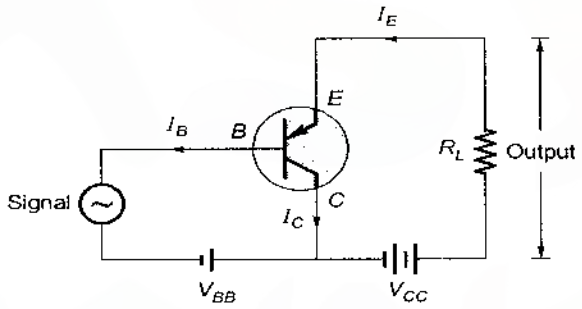
Total collector current

$$\boxed{I_C = \beta I_B + I_{CEO}} \text{ (or) } \boxed{I_C = \beta I_B + (1+\beta) I_{CBO}}$$

where, I_{CEO} = Collector to emitter leakage current

$$\boxed{I_{CEO} = (1+\beta) I_{CBO}}$$

3. Common Collector Configuration



Common emitter *pnp* transistor

Current amplification factor (γ)

When no signal is applied then the ratio of emitter current to the base current is called γ of the transistor.

$$\boxed{\gamma = \frac{I_E}{I_B}} \quad ; \quad \boxed{\gamma = 1 + \beta = \frac{1}{1-\alpha}}$$

Total emitter current

$$\boxed{I_E = (1+\beta) I_B + (1+\beta) I_{CBO}}$$

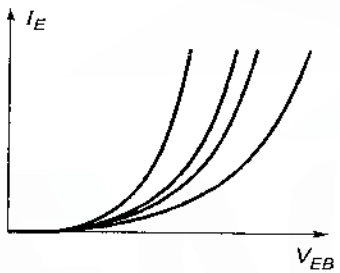
Note:

- This configuration has very high input resistance ≈ 750 kΩ and very low output resistance.
- Voltage gain is always less than one so never used for amplification purpose.
- This configuration is used for impedance matching i.e. driving a low impedance load from a high impedance source.

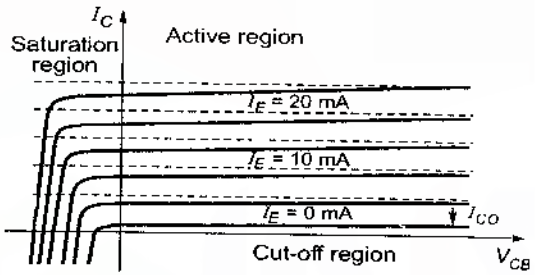
Characteristics	CB Configuration	CE Configuration	CC Configuration
Input resistance	Very low (40 Ω)	Low (50 kΩ)	Very high (750 kΩ)
Output resistance	Very high (1 MΩ)	High (10 kΩ)	Low (50 Ω)
Current gain	Less than unity	High (100)	High (100)
Voltage gain	Small (150)	High (500)	Less than unity
Leakage current	Very small	Very large	Very large
Applications	For high frequency applications	For audio frequency applications	For impedance matching
Phase shift between input and output	0°	180°	0°

Input and Output Characteristics of Different Configuration

The collector current I_C is completely determined by the input current I_E and the V_{CB} voltage.

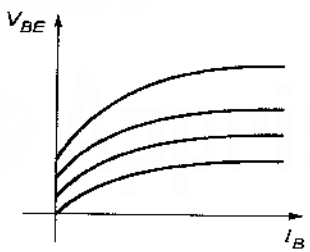


Input characteristics of CB configuration

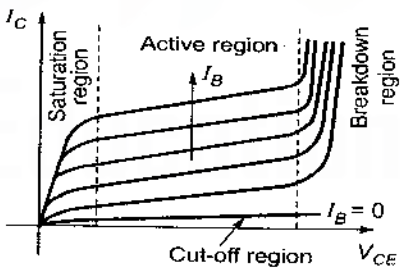


Output characteristics of CB configuration

The curve between I_B and V_{BE} for different values of V_{CE} are shown in figure.



Input characteristics of CE configuration

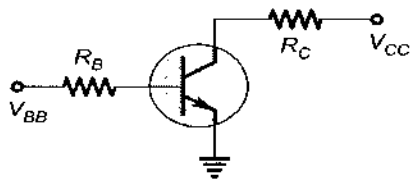


Output characteristics of CE configuration

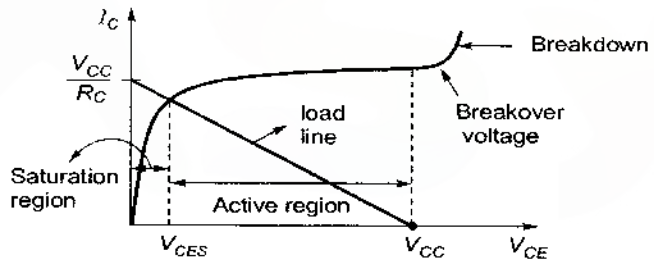
The output characteristics are the curve between V_{CE} and I_C for various values of I_B.

DC Load Lines

- DC load line is the locus of all possible operating point at which BJT remains in active region.



- If base current $I_B < \frac{I_{C\,sat}}{\beta}$ then transistor operate in active region.



- If $I_B > \frac{I_{C\,sat}}{\beta}$ then it operates in saturation region.
- Collector current $I_C = \frac{V_{CC} - V_{CE}}{R_C}$ for above figure.

  at saturation, $\boxed{V_{CE} = V_{CES}}$.
- $V_{CE} = V_{CC}$ at cutoff when $I_C = 0$.
- Maximum value of current

$$I_{C\max} = \frac{V_{CC}}{R_C} \qquad \text{[Taking } V_{CE} = 0 \text{ at saturation]}$$

  This is the ideal case.
- *Power dissipated* in a transistor is

$$P_D = I_C V_{CE}$$

Remember:

Power dissipation is maximum in active region and minimum in cutoff region and saturation region.

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