Digital ICs Family

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A group of compatible ICs with the same logic levels and supply voltages for performing various logic functions have been fabricated using a specific circuit configuration, is called "logic family".

Characteristics of Logic Families

1. Propagation Time Delay (t_{pd})

This is the average transition delay time for the signal to propagate from input to output when signal changes its value. This determines how fast the logic system can operate.

Delay time:

$$t_{pd} = \frac{t_{PHL} + t_{PLH}}{2} \text{ ns}$$

where t_{PLH} = Delay time in going form LOW logic to HIGH logic
t_{PHL} = Delay time in going form HIGH logic to LOW logic

Remember:

- The delay times are measured between the 50% points on the input and output transitions.
- In BJT, $t_{PLH} > t_{PHL}$ due to reverse recovery time.
- In FET, $t_{PLH} < t_{PHL}$ due to large capacitance formed.

2. Power Dissipation (P_D)

- It is the amount of power dissipated in an IC.
- It is determined by the current "I_{CC}" which draws from the V_{CC} supply.

Collector current:

$$I_{CC} = \frac{I_{CCH} + I_{CCL}}{2}$$

where, I_{CCH} = current value when all inputs are HIGH.
I_{CCL} = current value when all inputs are LOW.

Power dissipation:

$$P_{D(avg)} = I_{CC} \times V_{CC} \text{ mW}$$

3. Figure of Merit (FOM)

$$FOM = t_{pd} \times P_{D(avg)} \text{ picoJoules}$$

For the best operation of ICs, figure of merit (FOM) should be as small as possible.

4. Fan-in and Fan-out

The maximum number of inputs which can be applied to a logic gate is known as fan-in. On the other hand, fan out of a logic gate is the number of gates that can be driven by it.

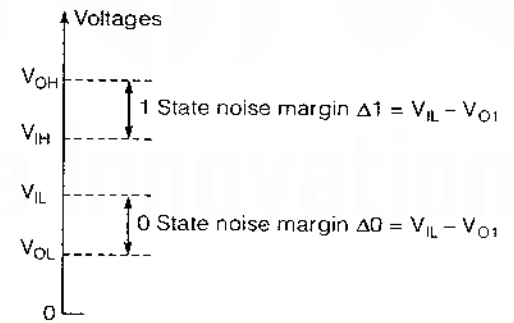
$$\text{Fan out} = \left(\frac{I_{OH}}{I_{IH}}\right) \text{ or } \left(\frac{I_{OL}}{I_{IL}}\right) \text{ ; whichever is minimum}$$

Note:

High fan-out is advantages because it reduces the need for additional drivers to drive more gates.

5. Noise-Margin

It is the property of a logic circuit to withstand unwanted noise voltage at input or the maximum value of noise signal that a system can reject with performance unaffected.



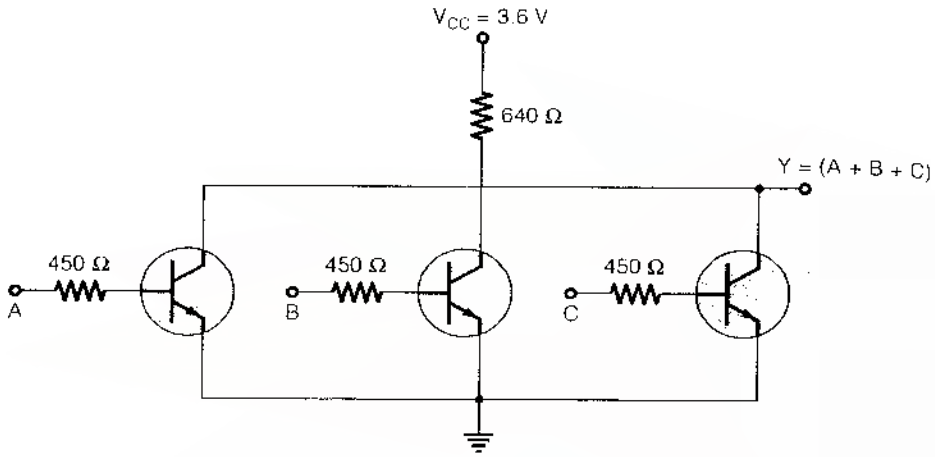
$V_{OH} > V_{IH} > V_{IL} > V_{OL}$

High state N.M. $= V_{NH} = V_{OH(min)} - V_{IH(min)}$

Low state N.m. $= V_{NL} = V_{IL(max)} - V_{OL(max)}$

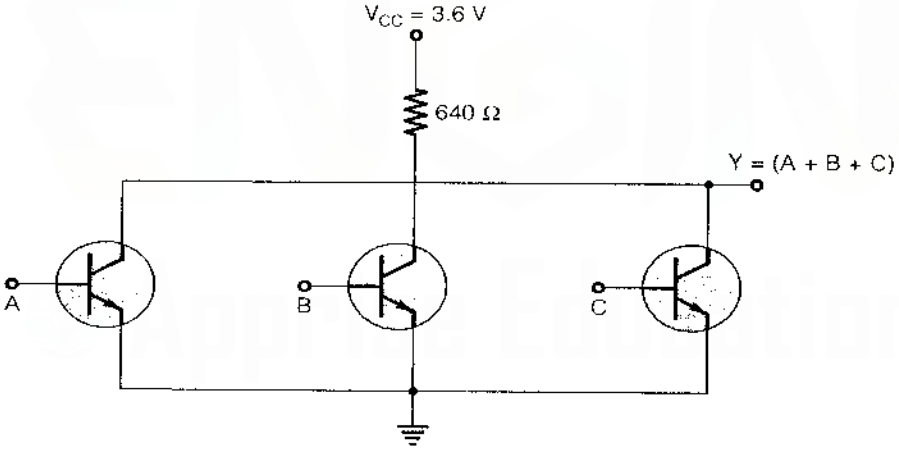
Bipolar Logic Families

Resistor Transistor Logic (RTL)



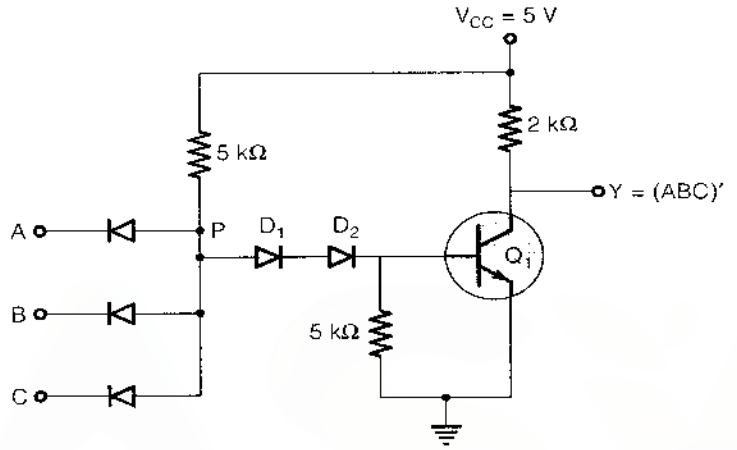
- RTL provides wired AND logic.

Diode Coupled Transistor Logic (DCTL)



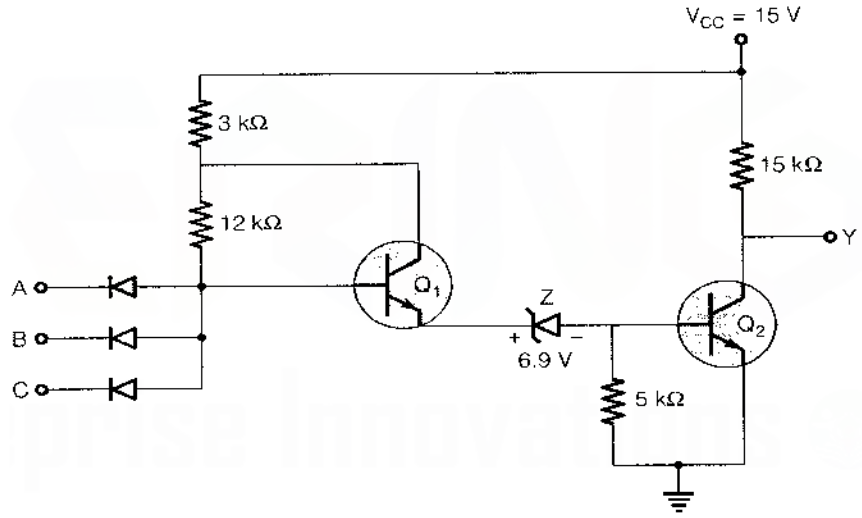
- DCTL provides wired AND logic.
- It suffers from "current Hogging".

Diode Transistor Logic (DTL)



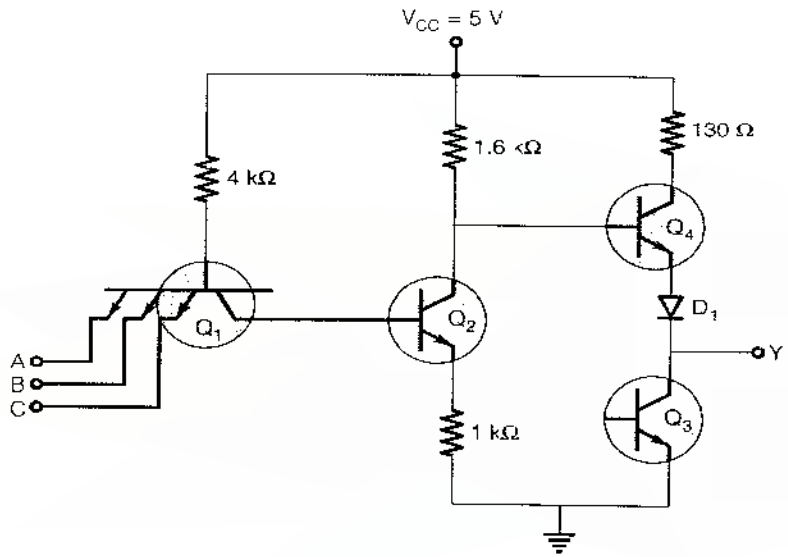
- DTL provides wired AND logic.

High Threshold Logic (HTL)



- HTL circuits has excellent noise margin and largest voltage swing.

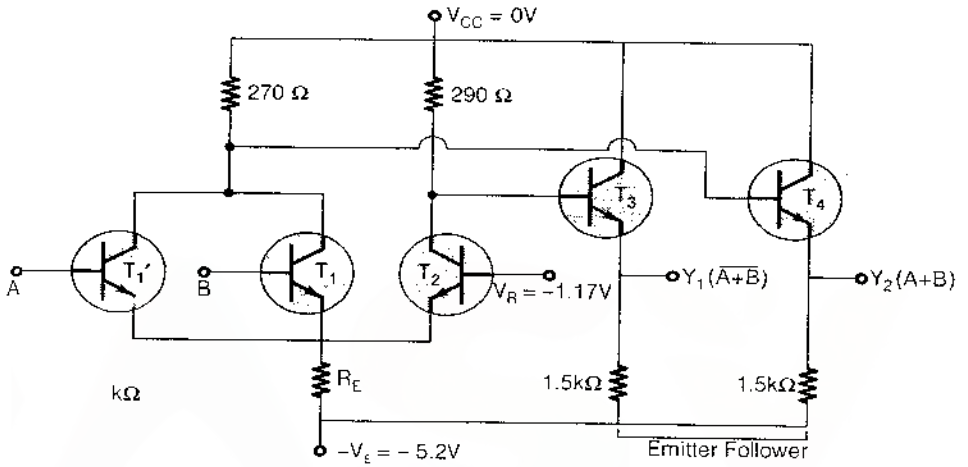
Transistor Transistor Logic (TTL)



TTL gate with totem-pole output

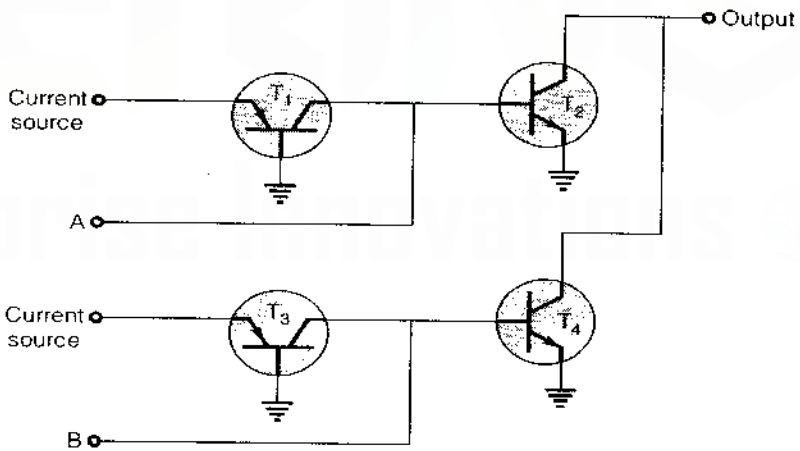
- TTL circuits are classified as:
  - (i) Tristate logic (high impedance logic)
  - (ii) Totem pole logic (active pull-up)
  - (iii) Open collector logic (passive pull-up)
- Tristate logic is used in bus oriented system.
- Totem pole logic does not provide wired logic.
- The advatange of active pull-up over passive pull-up is, reduced power dissipation and increased speed of operation.
- Any floating input TTL is consider as logic '1'.

Emitter Coupled Logic (ECL)



- ECL is a non saturated logic.
- It is the fastest logic among the all hence called "current mode logic".
- It provides wired 'OR' logic.
- It uses negative power supply to avoid noise and glitches.
- Any floating input in ECL is considered as logic '0'.

Integrated Injection Logic (IIL or I^2L)



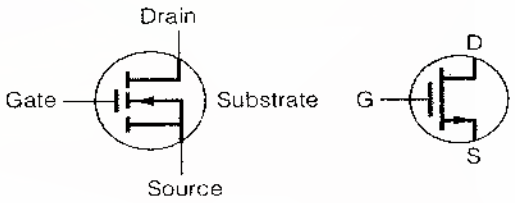
MOS Logic Family

- MOS digital ICs use enhancement MOSFETs exclusively.
- Because of the symmetrical construction of source (S) and drain (D), the MOS transistor can be operated as a bilateral device.

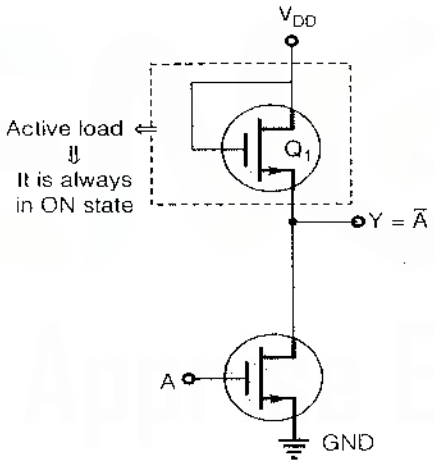
N-Channel MOS (NMOS)

- It is faster than PMOS.
- NMOS conducts whenever input is HIGH.

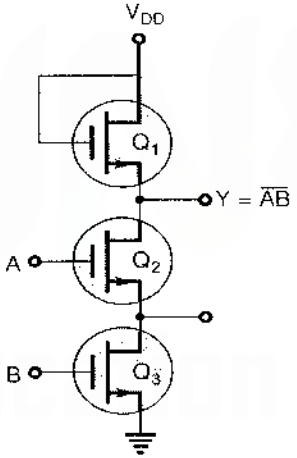
Symbol



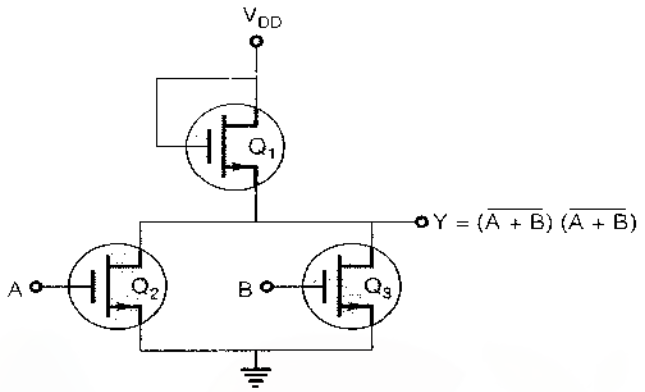
Different Logic Gates by NMOS



Inverter by NMOS



NAND by NMOS

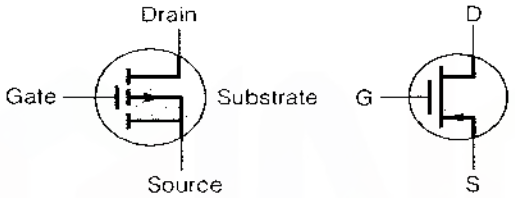


NOR by NMOS

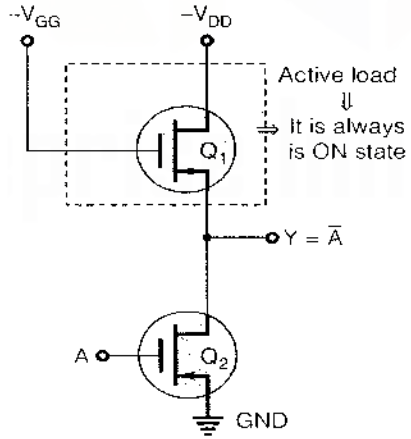
P-channel MOS (PMOS)

- Also called "Pull-Up Network".
- PMOS uses FETs having heavily doped P-channel.
- PMOS conducts whenever input is LOW.

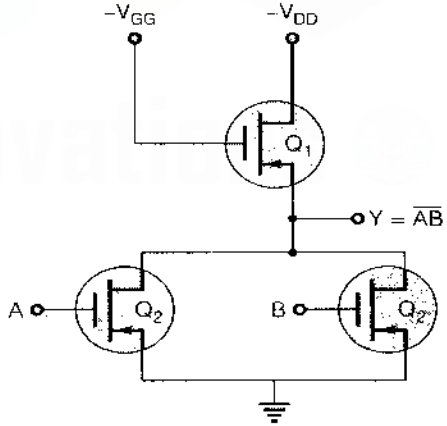
Symbol



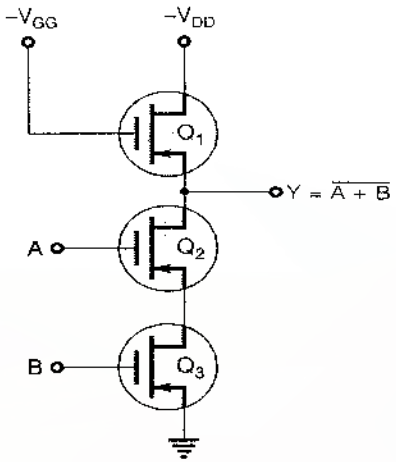
Different logic gates by PMOS



Inverter by PMOS



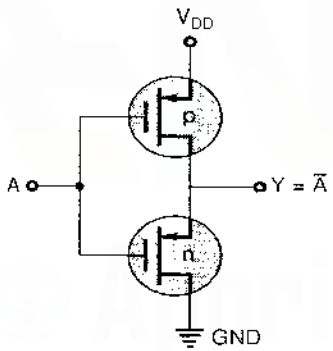
NAND by NMOS

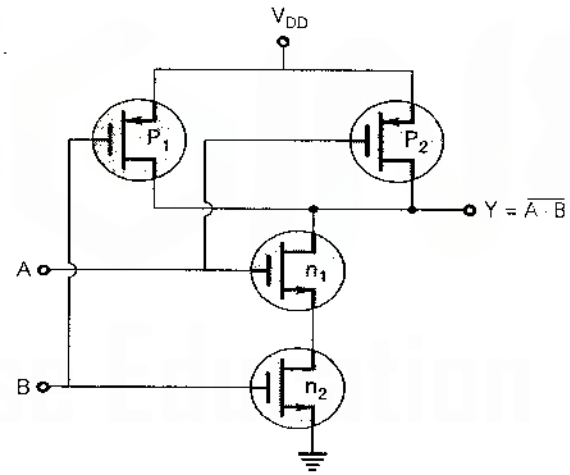


NOR by PMOS

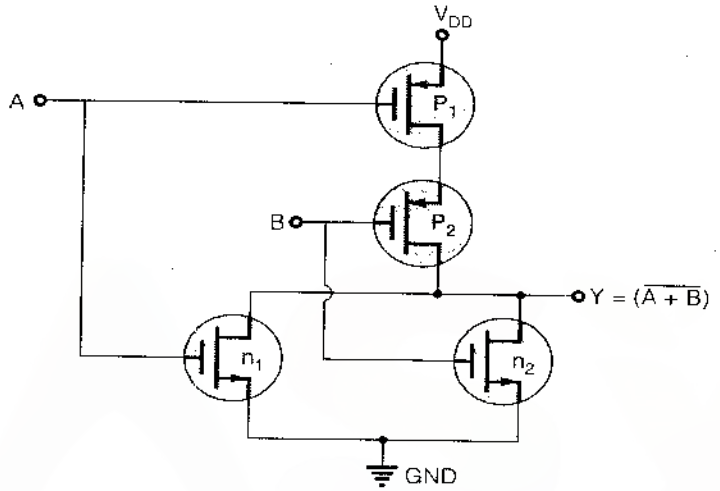
Complementary MOS (CMOS)

Different logic gates by NMOS





NOR by CMOS



- Lower power dissipation.
- Excellent noise immunity.
- High packing density.
- Wide range of supply voltages.
- High speed.

Comparison of Various Logic Families

Logic parameter	Basic GATE	Fan-out	Power dissipation (mW)	T_{PD} (nsec)	F.O.M (pJ)	N.M. (volt)
RTL	NOR	5	12	50	500	0.2
DTL	NAND	8	8-12	30	240	0.75
HTL	NAND	10	55	90	5000	4-5
TTL	NAND	10	12-22	12-6	144-132	0.4
ECL	OR/NOR	25	40-55	4-1	55-160	0.3
MOS	NAND/NOR	20	0.2-10	300	60	1-5
CMOS	NAND/NOR	>50	0-0.01	70	0.7	$\frac{V_{DD}}{2}$

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