DAY THIRTY FIVE

# Gate Circuit

*Learning & Revision for the Day*

- Logic Gates and Truth Table
- The OR Gate
- The AND Gate
- The NOT Gate
- Combination of Logic Gates
- Transistor as a Switch

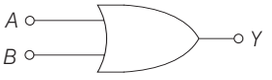
## Logic Gates and Truth Table

**Logic Gates** The digital circuit that can be analysed with the help of Boolean algebra is called logic gate or logic circuit. A logic gate has two or more inputs but only one input. There are primarily three logic gates namely the OR gate, the AND gate and the NOT gate.

**Truth Table** The operation of a logic gate or circuit can be represented in a table which contains all possible inputs and their corresponding outputs is called the truth table. To write the truth table, we use binary digits 1 and 0.

## The OR Gate

The OR gate is a device has two or more inputs and one output. This device combines two inputs to give one output. The logic symbol of OR gate is




The Boolean expression for OR gate is

$$Y = A + B$$

This indicates $Y$ equals $A$ OR $B$.

**Truth table for OR gate ($Y = A + B$)**

| $A$ | $B$ | $Y$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

The output of an OR gate assumes 1 if one of more inputs assume 1. The output is high when either of inputs $A$ or $B$ is high, but not if both $A$ and $B$ are low.

## The AND Gate

The AND gate a device has also two or more inputs and one output. The output of AND gate is equal to product of its inputs. The logic symbol of AND gate is


The logic symbol of AND gate is given as under. The Boolean expression for AND gate is $Y = A \cdot B$, this indicates $Y$ equals to $A$ AND $B$.

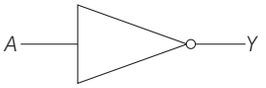
**Truth table for AND gate ($Y = A \cdot B$)**

| *A* | *B* | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

The output of an AND gate is 1 only, when all the inputs assume 1.

## The NOT Gate

The NOT gate is a device which has only one input and only one output. Its output is complement of input. The logic symbol of NOT gate is as shown in figure.




The Boolean expression for NOT gate is

$$Y = \overline{A},$$

which indicates $Y$ equals NOT $A$.

**Truth Table for NOT gate ($Y = \overline{A}$)**

| *A* | *Y* |
|---|---|
| 0 | 1 |
| 1 | 0 |

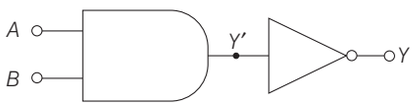
The output of a NOT gate assumes 1, if input is 0 and *vice-versa*. These basic gates (OR, AND and NOT) can be combined in various ways to provide large number of complicated digital circuits.

## Combination of Logic Gates

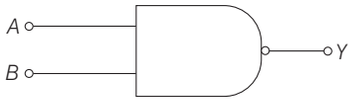
NAND gate and NOR gate are used to make any gate.

### 1. NAND Gate

In this type of gate, the output of AND gate is fed to input of a NOT gate and final output is obtained at output of NOT gate.




The logic symbol of NAND gate is shown as



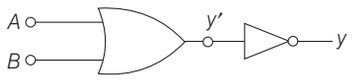

The Boolean expression of NAND gate is $Y = \overline{A \cdot B}$, which indicates '$A$ AND $B$ are negated'.

**Truth table for NAND gate**

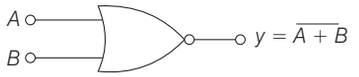
| *A* | *B* | *Y′* | *Y* |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

### 2. NOR Gate

In this type of gate, the output of OR gate is fed to input of the NOT gate and final output is obtained at output of the NOT gate.




The logic symbol of NOR gate is shown as




The Boolean expression for NOR gate is $Y = \overline{A + B}$, which indicates that '$A$ OR $B$ are negated'

**Truth table for NOR gate**

| *A* | *B* | *Y′* | *Y* |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 |

NOTE

- NAND and NOR gates are known as universal gate.
- The Boolean expressions obey the commutative law, associative law as well as distributive law.

Commutative law

(i) $A + B = B + A$ (ii) $A \cdot B = B \cdot A$

Associative law

(iii) $A + (B + C) = (A + B) + C$ (iv) $(A \cdot B) \cdot C = A \cdot (B \cdot C)$

Distributive law

(v) $A \cdot (B + C) = A \cdot B + A \cdot C$

(vi) $A + \overline{A} \cdot B = A + B$

(vii) $A + A \cdot B = A$

(viii) $A \cdot (A + B) = A$

(ix) $A \cdot (\overline{A} + B) = A \cdot B$

(x) $\overline{A \cdot B} = \overline{A} + \overline{B}$

(xi) $\overline{A + B} = \overline{A} \cdot \overline{B}$

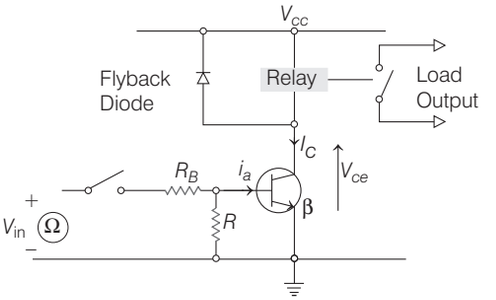
(xii) $\overline{\overline{A}} = A$

## Transistor as a Switch

The circuit resembles that of the **Common-Emitter** circuit. The difference this time is that to operate the transistor as a switch the transistor needs to be turned either fully "OFF" (Cut-off) fully "ON" (Saturated).

An ideal transistor switch would have an infinite resistance when turned 'OFF' resulting in zero current flow and zero resistance, when turned "ON", resulting in maximum current flow.

In practice, when turned "OFF', small leakage currents flow through the transistor and when fully "ON" the device has a low resistance value causing a small saturation voltage ($V_{ce}$) across it. In both the cut-off and saturation regions, the power dissipated by the transistor is at its minimum.




DAY PRACTICE SESSION 1

# FOUNDATION QUESTIONS EXERCISE

***1*** The output of a two input OR gate is fed to a NOT gate, the new gate obtained is

(a) OR gate (b) NOT gate
(c) NOR gate (d) NAND gate

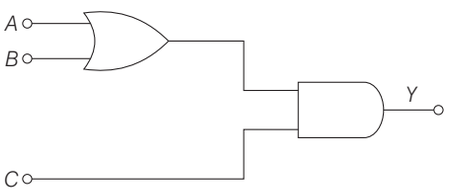
***2*** Which of the following is the truth table for NOT gate?

(a) $\begin{bmatrix}1 & 1\\ 0 & 0\end{bmatrix}$ (b) $\begin{bmatrix}1 & 0\\ 0 & 0\end{bmatrix}$ (c) $\begin{bmatrix}0 & 1\\ 1 & 0\end{bmatrix}$ (d) $\begin{bmatrix}0 & 1\\ 1 & 1\end{bmatrix}$

***3*** The output of OR gate is high

(a) if either or both the inputs are 1
(b) only if both inputs are 1
(c) if either input is zero
(d) if both inputs are zero

***4*** To get an output 1 from the circuit as shown in the figure, the input must be

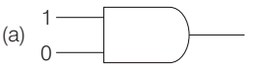


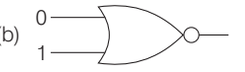

(a) $A = 0, B = 1, C = 0$
(b) $A = 1, B = 0, C = 0$
(c) $A = 1, B = 0, C = 1$
(d) $A = 1, B = 1, C = 0$

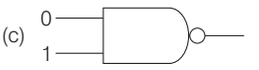
***5*** Digital circuit can be made by the repetitive use of

(a) OR gates (b) AND gates
(c) NOT gates (d) NAND gates

***6*** Which of the following gates will have an output of 1 ?

(a) 

(b) 

(c) 

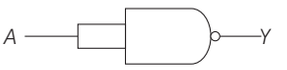
(d) None of these

***7*** The following truth table is for

| *A* | *B* | *Y* |
|---|---|---|
| 1 | 1 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 0 | 0 | 1 |

(a) NAND (b) AND (c) XOR (d) NOT

***8*** Which of the following is the truth table for the circuit below?




(a)

| *A* | *Y* |
|---|---|
| 1 | 0 |
| 0 | 1 |

(b)

| *A* | *Y* |
|---|---|
| 0 | 0 |
| 1 | 1 |

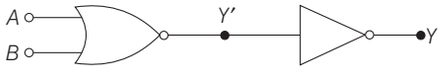
(c)

| *A* | *Y* |
|---|---|
| 1 | 1 |
| 0 | 1 |

(d)

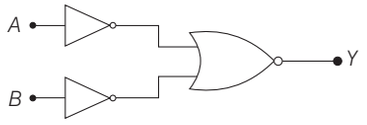
| *A* | *Y* |
|---|---|
| 0 | 1 |
| 0 | 0 |

**9** The circuit as shown in figure below will act as



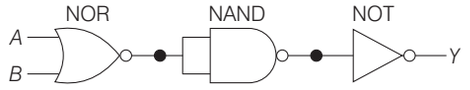

(a) OR gate (b) AND gate
(c) XOR gate (d) None of these

**10** The circuit as shown below will acts as




(a) AND gate (b) OR gate
(c) NAND gate (d) NOR gate

**11** The circuit is equivalent to



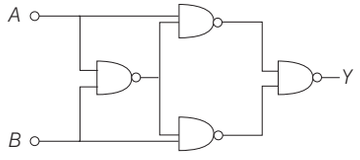

(a) AND gate (b) NAND gate
(c) NOR gate (d) OR gate

**12** The output of an OR gate is connected to both the inputs of a NAND gate. The combination will serve as a

**→ AIEEE 2011**

(a) OR gate (b) NOT gate
(c) NOR gate (d) AND gate

**13** Truth table for system of four NAND gates as shown in figure is **→ AIEEE 2012**




(a)

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

(b)

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

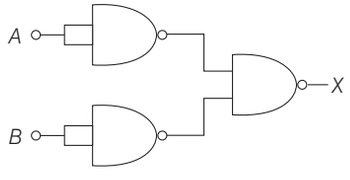
(c)

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

(d)

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

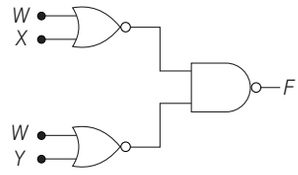
**14** The combination of gates shown below yields




**→ AIEEE 2010**

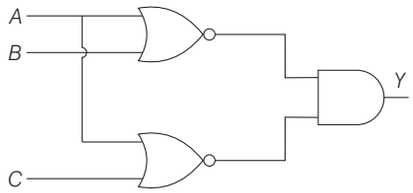
(a) OR gate (b) NOT gate
(c) NOR gate (d) NAND gate

**15** The diagram of a logic circuit is given below. The output $F$ of the circuit is given by




(a) $W \cdot (X + Y)$ (b) $W \cdot (X \cdot Y)$
(c) $W + (X \cdot Y)$ (d) $W + (X + Y)$

**16** The output, $Y$ of given logic circuit is




(a) $A \cdot (B + C)$ (b) $A \cdot (B \cdot C)$
(c) $(\overline{A+B}) \cdot (\overline{A+C})$ (d) $A + B + C$

**17** What will be the input of $A$ and $B$ for the Boolean expression $(\overline{A+B}) \cdot (\overline{A \cdot B}) = 1$?

(a) 0, 0 (b) 0, 1
(c) 1, 0 (d) 1, 1

**18** Which of the following is not equal to 1 in Boolean algebra?

(a) $A + 1$ (b) $A \cdot \overline{A}$
(c) $A + \overline{A}$ (d) $\overline{\overline{A \cdot A}}$

**Direction** (Q.Nos. 19-21) *Each of these questions contains two statements: Statement* I *and Statement* II. *Each of these questions also has four alternative choices, only one of which is the correct answer. You have to select one of the codes (a),(b), (c),(d) given below.*

(a) Statement I is true, Statement II is true; Statement II is the correct explanation for Statement I
(b) Statement I is true, Statement II is true; Statement II is not the correct explanation for Statement I
(c) Statement I is true; Statement II is false
(d) Statement I is false; Statement II is true

**19** **Statement I** The logic gate NOT cannot be built using diode.

**Statement II** The output voltage and the input voltage of the diode have 180° phase difference.

**20** **Statement I** NOT gate is also called invertor.

**Statement II** NOT gate inverts the input signal.

**21** **Statement I** NAND or NOR gates are called digital building blocks.

**Statement II** The repeated use of NAND or NOR gates can produce all the basic or complicated gates.

DAY PRACTICE SESSION 2

# PROGRESSIVE QUESTIONS EXERCISE

***1*** The output of an OR gate is connected to both the inputs of a NAND gate , the truth table is

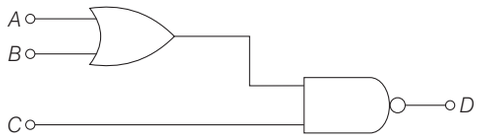
| *A* | *B* | *Y* |
|---|---|---|
| 1 | 0 | 0 |
| 1 | 1 | 1 |
| 0 | 1 | 0 |

| *A* | *B* | *Y* |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

| *A* | *B* | *Y* |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

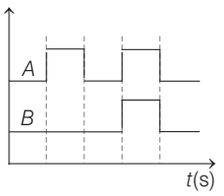
(d) None of these

***2*** For the given combination of gates, if the logic states of inputs $A$, $B$ and $C$ are as follows. $A = B = C = 0$ and $A = B = 1$, $C = 0$, then the logic states of output $D$ are

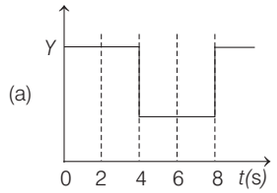


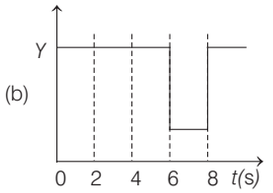

(a) 0, 0 (b) 0, 1 (c) 1, 0 (d) 1, 1

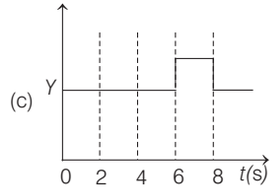
***3*** The real time variation of input signals $A$ and $B$ are as shown below.If the inputs are fed into NAND gate, then select the output signal from the following

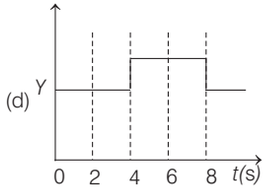




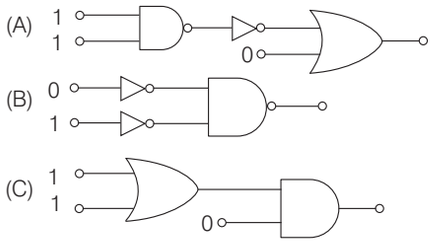


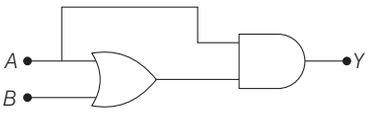




***4*** In the following combinations of logic gates, the outputs of $A$, $B$ and $C$ are respectively




(a) 0,1,1
(b) 0,1,0
(c) 1,1,0
(d) 1,0,1

***5*** The truth table of the following combination of gates is




(a)

| Inputs | | Outputs | |
|---|---|---|---|
| ***A*** | ***B*** | $A \cdot B$ | Y |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

(b)

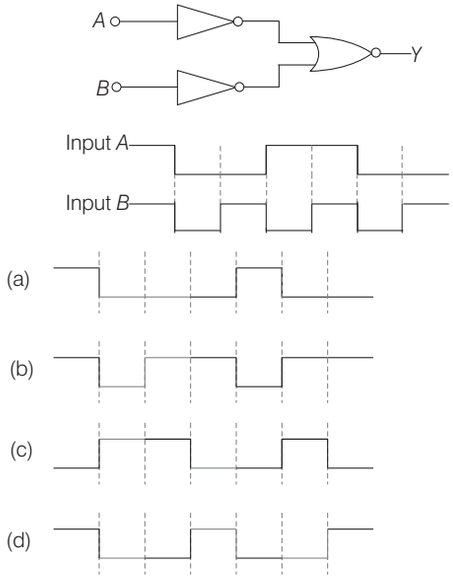
| Inputs | | Outputs | |
|---|---|---|---|
| ***A*** | ***B*** | $A \cdot B$ | ***Y*** |
| 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |

(c)

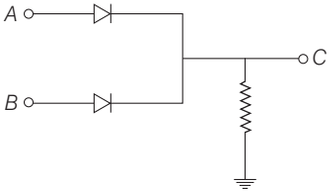
| Inputs | | Outputs | |
|---|---|---|---|
| ***A*** | ***B*** | $A + B$ | $Y = A \cdot (A + B)$ |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 |

(d) None of the above

**6** The logic circuit shown below has the input waveforms *A* and *B* as shown. Pick out the correct output waveform.




**7** In the adjacent circuit, A and B represent two inputs and C represents the output,




The circuit represents

(a) NOR gate (b) AND gate
(c) NAND gate (d) OR gate

**8** Which of the following circuits has given outputs?

| A | B | C |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

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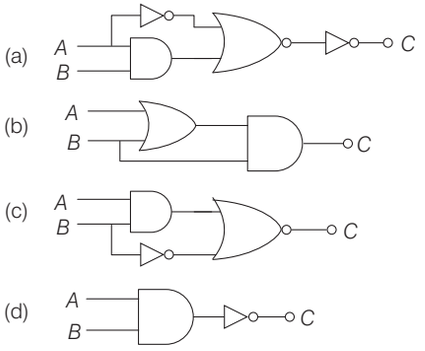
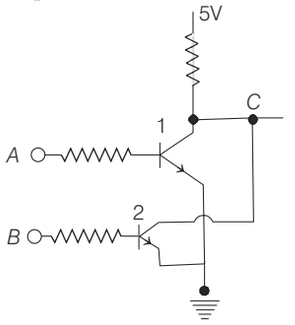



**9** Consider two n-p-n transistors as shown in figure. If 0 V corresponds to false and 5 V corresponds to true, then the output at C corresponds to




**→ JEE Main (Online) 2013**

(a) *A* NAND *B* (b) *A* OR *B*
(c) A AND *B* (d) *A* NOR *B*

**10** If *a, b, c* and *d* are inputs to a gate and *x* is its output every time, then as per the following time graph, the gate is

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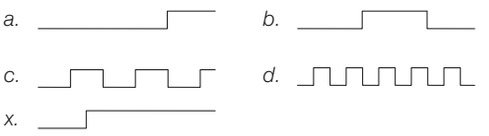



(a) NOT
(b) AND
(c) OR
(d) NAND

# ANSWERS

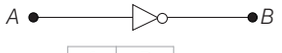
| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| SESSION 1 | **1** (c) | **2** (c) | **3** (a) | **4** (c) | **5** (d) | **6** (c) | **7** (a) | **8** (a) | **9** (a) | **10** (a) |
| | **11** (c) | **12** (c) | **13** (a) | **14** (a) | **15** (d) | **16** (c) | **17** (a) | **18** (b) | **19** (c) | **20** (a) |
| | **21** (a) | | | | | | | | | |
| SESSION 2 | **1** (b) | **2** (d) | **3** (b) | **4** (c) | **5** (c) | **6** (a) | **7** (d) | **8** (c) | **9** (a) | **10** (c) |

# Hints and Explanations

## SESSION 1

**1** The combination of OR and NOT gates is NOR gate.

**2** Truth table of NOT gate is




| A | B |
|---|---|
| 0 | 1 |
| 1 | 0 |

**3** OR gate output is high, if anyone or both input are high.

**4** The Boolean expression for the given combination is $Y = (A + B)\cdot C$
The truth table is

| A | B | C | A + B | Y = (A + B) C |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

Hence, $A = 1, B = 0$ and $C = 1$

**5** The repetitive use of NAND and NOR gate gives digital circuits.

**6** For option (c), it is a NAND gate, its output $= \overline{0.1} = \overline{0} = 1$

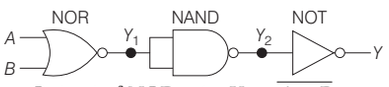
**7** For NAND gate, $Y = \overline{AB}$

**8** The output of the NAND gate is
$$Y = \overline{A\cdot A} = \overline{A} + \overline{A} = \overline{A}$$

**9** The output of NOR gate is made input for NOT gate.
$$Y = \overline{\overline{A + B}} = A + B$$

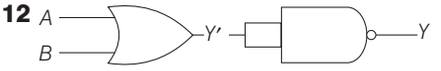
**10** The output of two NOT gate is input for NOR gate.
Hence, $Y = \overline{\overline{A} + \overline{B}} = \overline{\overline{A}}\cdot\overline{\overline{B}} = A\cdot B$
(AND gate)

**11** The gate circuit can be shown by given two points $A$ and $B$.




Output of NOR gate, $Y_1 = \overline{A + B}$
Output of NAND gate,
$Y_2 = \overline{Y_1\cdot Y_1} = \overline{\overline{A + B}\cdot\overline{A + B}}$
$= \overline{\overline{A + B}} + \overline{\overline{A + B}}$
$= (A + B) + (A + B) = A + B$
Output of NOT gate,
$Y = \overline{Y_2} = \overline{A + B}$
which is output of NOR gate.

**12**




$Y' = A + B$ and $Y = \overline{Y'} = \overline{A + B}$
i.e. output of a NOR gate.

**13** Boolean expression for the given circuit
$$Y = \overline{\overline{(A\cdot\overline{(A\cdot B)})}\cdot\overline{(B\cdot\overline{(A\cdot B)})}}$$
$$= \overline{(\overline{A} + A\cdot B)\cdot(\overline{B} + A\cdot B)}$$
$$= \overline{(\overline{A} + A\cdot B)} + \overline{(\overline{B} + (A\cdot B))}$$
$$= A\cdot\overline{(A\cdot B)} + B\cdot\overline{(A\cdot B)}$$
$$= A\cdot(\overline{A} + \overline{B}) + B\cdot(\overline{A} + \overline{B})$$
$$= A\cdot\overline{B} + B\cdot\overline{A}$$

| A | B | $\overline{A}$ | $\overline{B}$ | $A\cdot\overline{B}$ | $B\cdot\overline{A}$ | Y |
|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 |

So, option (a) is correct.

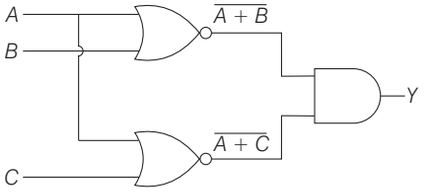
**14** Truth table for given combination is

| A | B | X |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

This comes out to be truth table of OR gate.

**15** The output $F = \overline{(\overline{W + X})\cdot(\overline{W + Y})}$
$$= \overline{\overline{(W + X)}} + \overline{\overline{(W + Y)}}$$
$$= W + X + W + Y$$
$$= W + X + Y$$

**16** The gate circuit is given as




$Y = \overline{(A+B)}\ \overline{(A+C)}$
For this circuit, output
$Y = (\overline{A + B})(\overline{A + C})$

**17** The given Boolean expression can be written as
$$Y = \overline{(A + B)}\cdot\overline{(AB)}$$
$$= (\overline{A}\cdot\overline{B})\cdot(\overline{A} + \overline{B})$$
$$= (\overline{A}\cdot\overline{A})\cdot\overline{B} + \overline{A}(\overline{B}\cdot\overline{B})$$
$$= \overline{A}\cdot\overline{B} + \overline{A}\cdot\overline{B}$$
$$= \overline{A}\cdot\overline{B}$$
So, the truth table is

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

**18** Here, $A\cdot\overline{A} = 0$ always when either $A = 0$ or 1.

**19** NOT gate inverts the signal applied to it. But in diode, the input and output are in same phase. Thus, NOT gate cannot be built using diode.

**20** NOT gate inverts the input signal i.e. if input is 1 then output will be zero or *vice-versa*. Therefore, it is called as invertor. NOT gate inverts the input order means that for low input, it gives high output or for high input, it gives low output.

**21** NAND or NOR gates are called universal (digital) building blocks because using these two types of gates we can produce all the basic gates namely OR, AND or other complex gates.

## SESSION 2

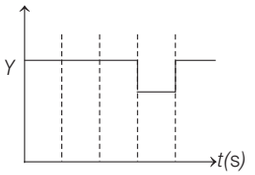
**1** When two inputs of a NAND gate are joined together, it works as a NOT gate. The OR gate connected to this NOT gate results is a NOR gate.

**2** The output $D$ for the given combination
$$D = \overline{(A + B)\cdot C} = \overline{(A + B)} + \overline{C}$$
If $A = B = C = 0$, then
$$D = \overline{(0 + 0)} + \overline{0}$$
$$= \overline{0} + \overline{0}$$
$$= 1 + 1 = 1$$
If $A = B = 1, C = 0$, then
$$D = \overline{(1 + 1)} + \overline{0}$$
$$= \overline{1} + \overline{0}$$
$$= 0 + 1 = 1$$

**3** From real time variation of input signals,we can from truth table for $A$ and $B$ and conclude output from NAND gate.

| Inputs | | Output |
|---|---|---|
| *A* | *B* | *Y* |
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 0 | 1 |
| 1 | 1 | 0 |
| 0 | 0 | 1 |

From output, we can show real time variation of output signal as below.




**4** A. NAND operation on (1, 1) = 0

NOT operation on (0) = 1

OR operation on (1, 0) = 1

B. NOT operation on (0, 1) = (1, 0)

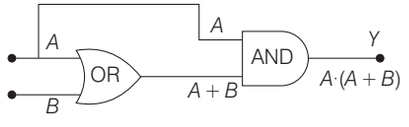
NAND operation on (1, 0) = 1

C. OR operation on (1, 1) = 1

AND operation on (1, 0) = 0

**5** Let us draw the given combination pointing out that the first gate is OR gate second gate is AND gate. The inputs of the OR gate, are $A$ and $B$, and its output is $A + B$ that is $A$ OR $B$.

The inputs of the AND gate are $A$ and $A + B$ and its output is $A \cdot (A + B)$ that is $A$ AND ($A$ or $B$). The truth table for the output is $Y = A.(A + B)$ is as follows




| Inputs | | Outputs | |
|---|---|---|---|
| *A* | *B* | *A + B* | *Y = A · (A + B)* |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 |

**6** Truth table

| *A* | *B* | *Y* |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |
| 0 | 0 | 0 |

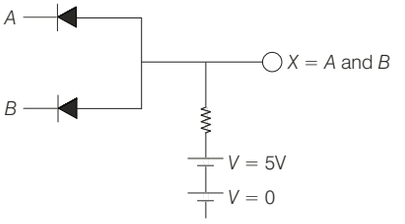
**7** If we give the following inputs to $A$ and $B$, then corresponding output is shows in table

| *A* | *B* | *C* |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

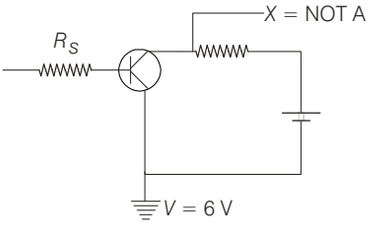
The above table is similar to OR gate.

**8** Observing the given gate we observe that gate would be same as given in option in which.
The values $A = 0, B = 0$ gives output 0
The values $A = 0, B = 1$ gives output 0
The values $A = 1, B = 0$ gives output 1
The value $A = 1$, and $B = 1$ gives output 0

**9** From the figure of AND gate




and NOT gate




Clearly, the function $X$ = NOT ($A$ AND $B$) of the logical variables $A$ AND $B$ is called NAND gate.

**10** Output of OR gate is 0 when all inputs are 0 and output is 1 when atleast one of the inputs is 1.

**Observing output *x*** It is 0 when all inputs are 0 and it is 1 when atleast one of the inputs is 1.

∴ The gate is OR.

**Alternative Method**

**OR Gate**

| a | b | c | d | x |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |