☆ Multi Vibrators using logic gates.

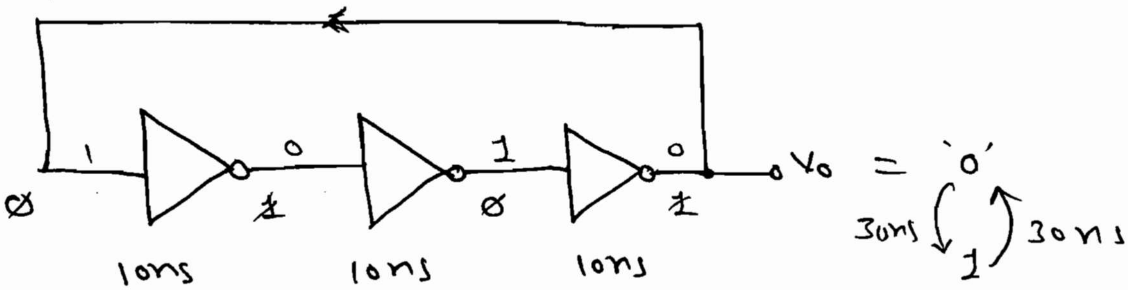
Applications

1. Astable Multivibrator → Square wave generator
(Free running mv)

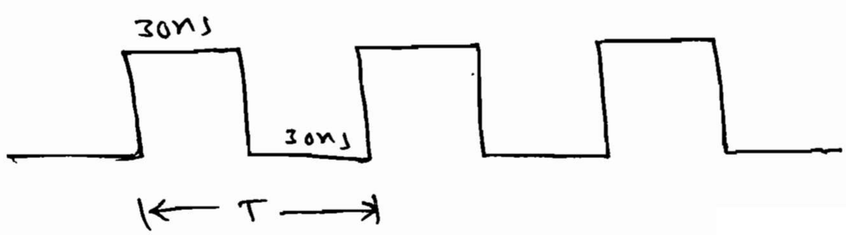
2. Monostable multivibrator → { (a) Pulse generator (b) Pulse stretcher.
(one shot mv)

3. Bistable multivibrator → 1-Bit memory.

* Astable Multivibrator Using logic gate.



'0', '1' = Unstable States.

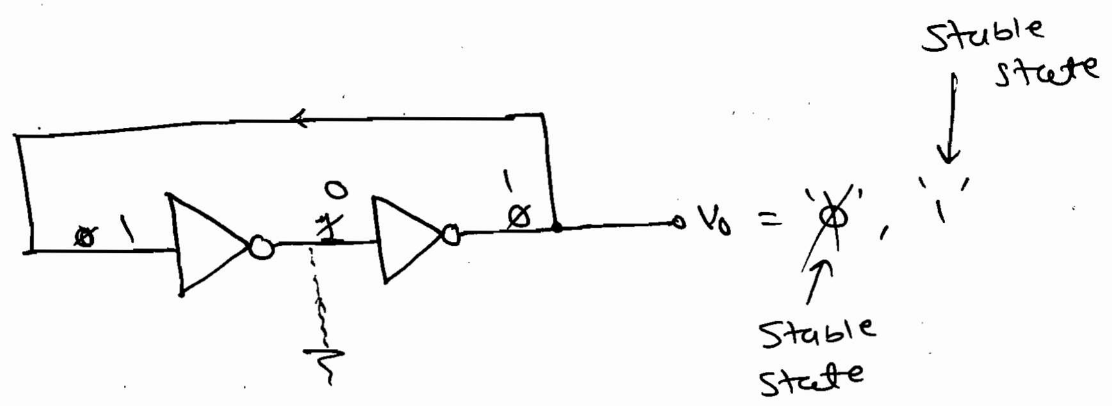


∴ $\boxed{T = 60\ ns}$

→ Time period of Square wave

$\boxed{T = 2 \times [\text{sum of Propagation Delays of all Inverters}]}$

* Bistable Multivibrators.

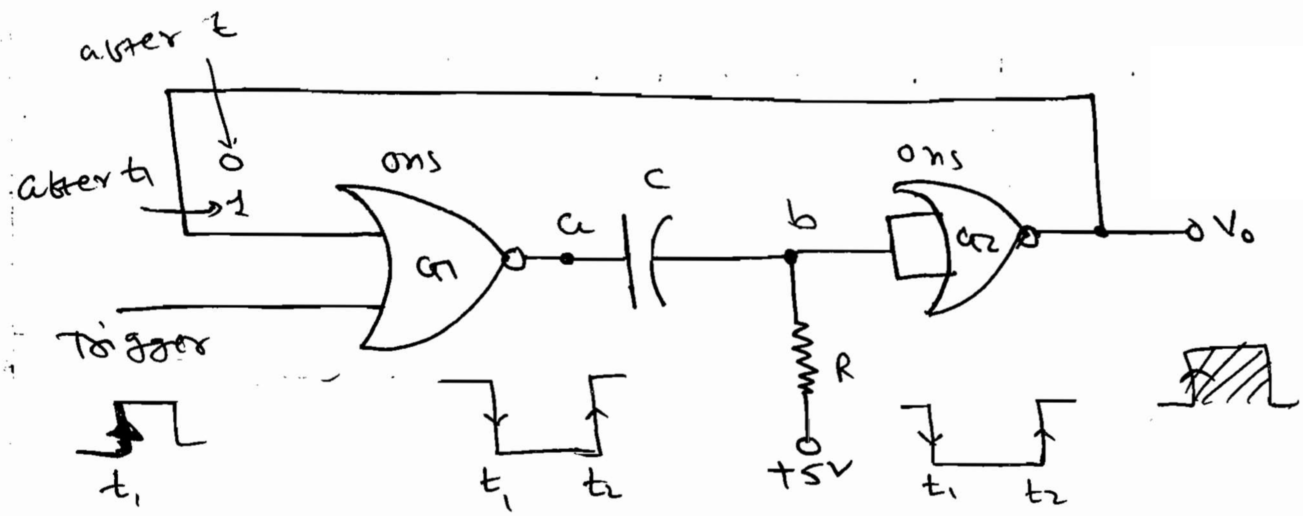


NOTE:

→ If odd no. of Inverter then ~~class~~ Astable MV.

→ If even no. of Inverter then Bistable MV.

* Monostable Multivibrator

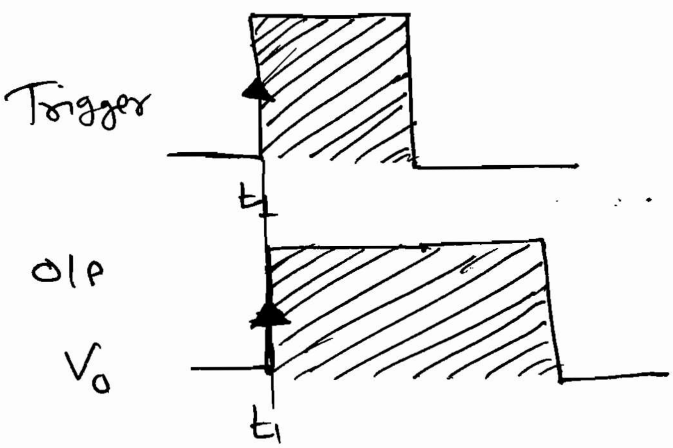


→ After T_1, the feedback came at gate-1 input is equal to '1' which means the $V_a = 0$. Capacitor charges to +5V with time constant RC.

→ Once capacitor charges to +5 Volts.

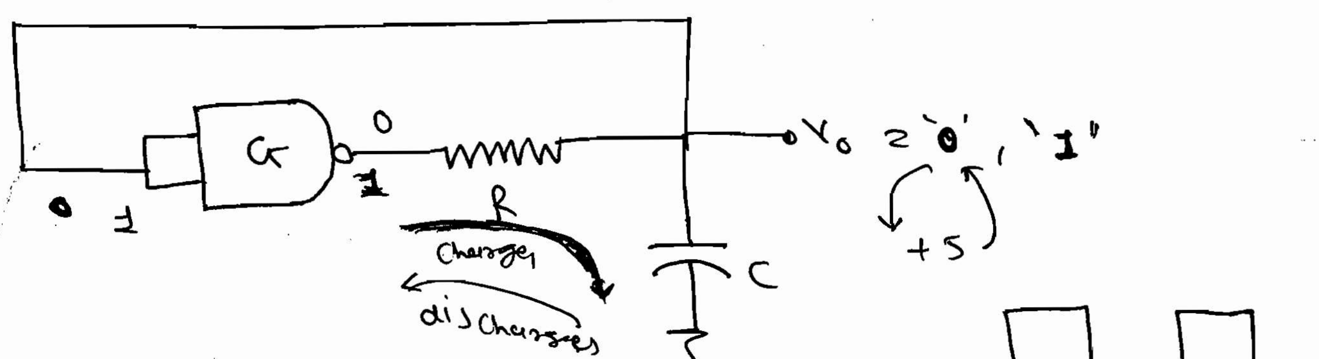
hence the capacitor discharges.

* **Pulse stretching.**



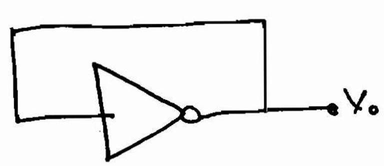
Ex- Determine the following multivibrators:

a)



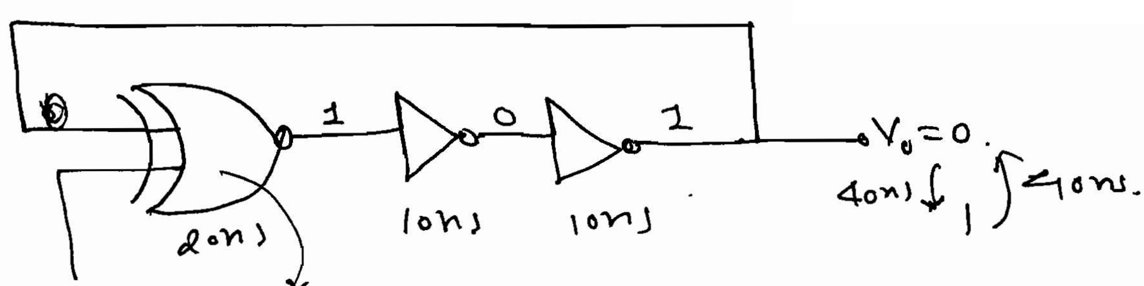
→ So, it is Astable mv.

b)

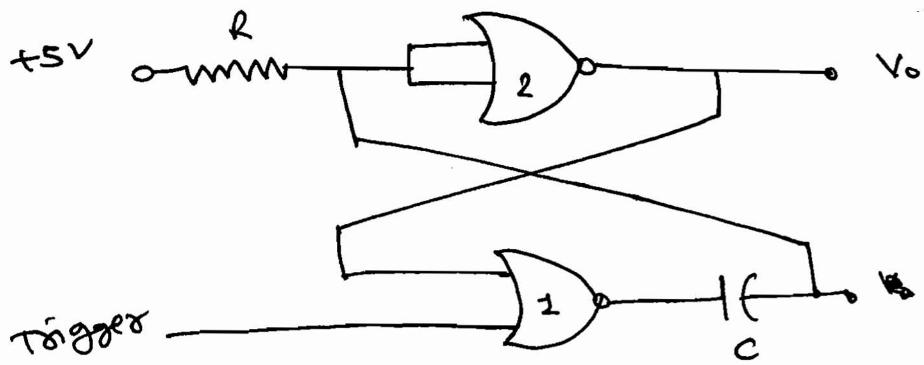


→ Astable mv.

c)

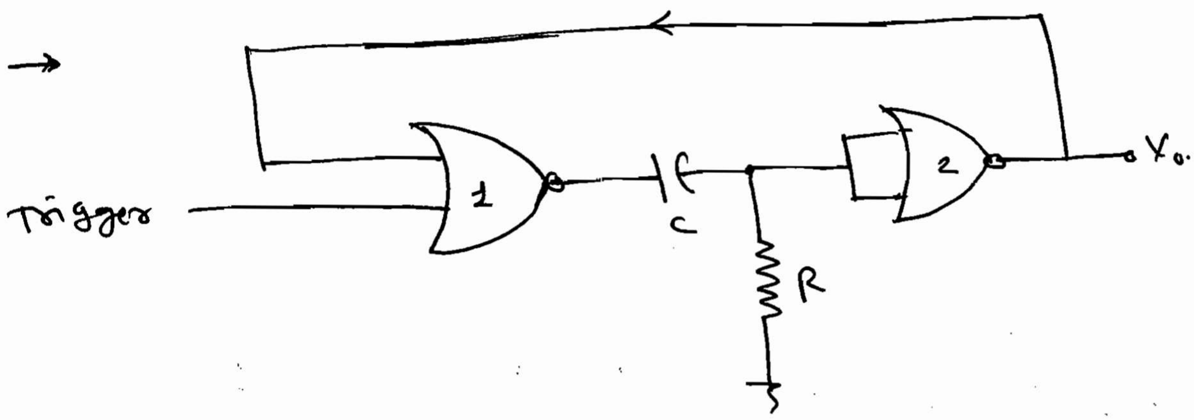


(4)



|||

→

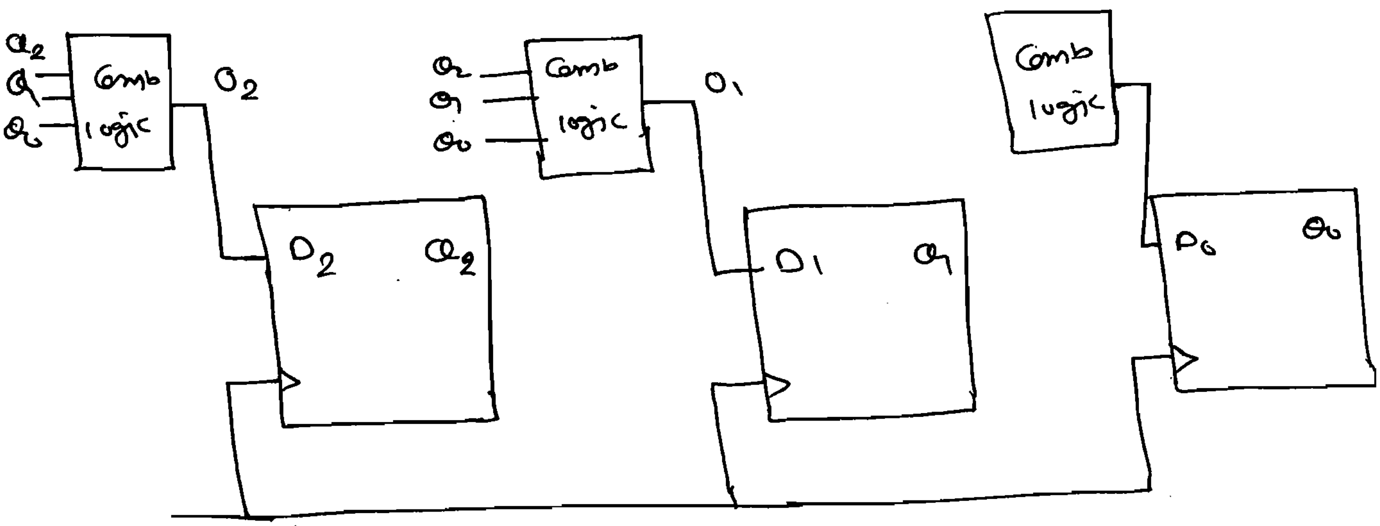


→ Now it is look like monostable mv.

so, given ckt is monostable mv.

Ex- In the following circuits determine the values of $O_2, O_1, O_0 = ?$ if it is counting the following sequence 101, 010, 110

→



→ This is nothing but design a sync counter using D-FF which counts through the states 5, 2, 6, 5, ...

→ at time of design use excitation table

→ at time of analysis use truth table.

→

P.S.			N.S			FF Inputs		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	D_2	D_1	D_0
1	0	1	0	1	0	0	1	0
0	1	0	1	1	0	1	1	0
1	1	0	1	0	1	1	0	1

(5)
(2)
(6)

→ $\boxed{D_2 = Q_1}$

$D_2 = \Sigma m(2,5) + d(0,3,1,4,7)$

→

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	X	X	X	1
1	X	1	X	0

$\therefore D_1 = \bar{Q}_2 + Q_0.$

$D_1 = \Sigma m(6) + d(0,1,3,4,7)$

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	X	X	X	0
1	X	0	X	1

$D_1 = \bar{Q}_0 Q_2$ (or) $Q_2 \cdot Q_1$